Threshold Voltage Temperature Dependence for a 1.2 kV SiC MOSFET with Non-Linear Gate Stack

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Abstract

The use of Silicon Carbide (SiC) power MOSFETs is becoming increasingly popular due to their unique properties, including a wide bandgap, higher critical electric field, and superior thermal conductivity compared to traditional Silicon (Si) MOSFETs. The reliability assessment of SiC power MOSFETs holds significant importance across various industries, such as automotive and aerospace, where these devices find numerous applications. One crucial aspect of their reliability is evaluating their performance during short-circuit (SC) events. To address this concern, this study employs TCAD simulations to analyze the behaviour of a SiC power MOSFET equipped with a gate insulator that consists of a stack of silicon dioxide (SiO_2) combined with a non-linear dielectric (NLD) material. This NLD exhibits a Curie-Weiss temperature dependence, characteristic of ferroelectric materials. During short-circuit events, failures are often associated with temperature rises. The study demonstrates the effectiveness of using an NLD with a temperature-dependent permittivity (ε) as a gate insulator. By doing so, the temperature increase is mitigated, and the MOSFET's ruggedness during short-circuit events is enhanced. This advancement in gate insulator technology could significantly improve the overall reliability and performance of SiC power MOSFETs in various applications.

Keywords: Silicon Carbide, Power MOSFET, TCAD Simulations, Ferroelectric Materials, Short-circuit Test.

INTRODUCTION

The use of Silicon Carbide (SiC) power MOSFETs is becoming increasingly popular due to their unique properties, including a wide bandgap, higher critical electric field, and superior thermal conductivity compared to traditional Silicon (Si) MOSFETs [1]. The reliability assessment of SiC power MOSFETs holds significant importance across various industries, such as automotive and aerospace, where these devices find numerous applications. A crucial validation test to assess reliability of SiC power MOSFETs is short-circuit (SC) [2]. Typical applications require a minimum short-circuit withstand time (SCWT) in the microsecond range. Typically, current devices are required to withstand the supply voltage for at least 5 µs. In this investigation, TCAD simulations are employed to gain insights into the behaviour of a 1.2 kV SiC power MOSFET, with a gate insulator that consists in a stack formed by silicon dioxide (SiO_2) and a non-linear dielectric (NLD) exhibiting a Curie-Weiss temperature dependence commonly found in ferroelectric materials [3,4]. During a short circuit event, the device experiences a sudden surge in current, which can lead to a significant increase in power dissipation. This sudden increase in power can cause localized heating, leading to hotspots within the device. This study illustrates how the implementation of an NLD, characterized by a temperature-dependent permittivity (ε), can effectively reduce the temperature rise. This advancement in gate insulator technology could significantly improve the overall reliability and performance of SiC power MOSFETs in various applications. A sketch of the proposed device, with a SiO_2/NLD stack as gate insulator, is reported in Fig.1.

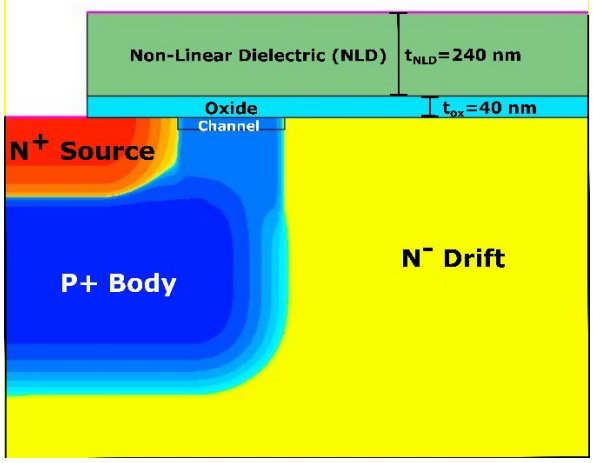

Fig. 1. Sketch of the proposed design, with an oxide/non-linear dielectric stack as gate insulator.

DEVICE MODELING

In the initial phase of the study, the non-linear dielectric (NLD) was implemented via the physical model interface of Sentaurus TCAD. The NLD was designed with the same properties of an oxide, except for its temperature-dependent permittivity. The latter was based on the ferroelectric material vinylidene fluoride trifluoroethylene P(VDF-TrFE) [5], whose permittivity has the behaviour described by Eq. 1.

$$\varepsilon = \lambda \frac{C_{CW}}{T - T_0} \; with \begin{cases} \lambda = -1/2 & for \quad T < T_0 \\ \lambda = 1 & for \quad T > T_0 \end{cases} \qquad (1)$$

P(VDF-TrFE) is characterized by a Curie Temperature (T_0) of 355 K, a Curie Weiss constant (C_{CW}) that is 3429 K, for the ferroelectric phase ($T<T_0$), and 11878 K for the paraelectric phase ($T>T_0$). The graphical representation of the resulted permittivity, varying the temperature, can be seen in Fig. 2.

Subsequently, the capacitance exhibited by the oxide/NLD stack was analyzed through AC simulations. Fig. 3 illustrates the variation of capacitance per unit area with temperature for anthe oxide/non-linear dielectric stack, featuring an oxide thickness (t_{OX}) of 40 nm and different NLD thicknesses (t_{NLD}). Below the Curie Temperature, as the temperature of the stack rises, the capacitance increases owing to the rising permittivity of the NLD. However, once the temperature surpasses the Curie Temperature, the permittivity of the NLD starts to decrease, resulting in a reduction of capacitance exhibited by the stack.

Next, the oxide/NLD stack replaced the standard gate oxide into the TCAD model of a commercial 1200 V SiC MOSFET, which had been previously calibrated using experimental data [6]. To match the transfer and output characteristics of the MOSFET with a standard gate oxide at the typical operating temperature of 340 K in automotive applications, the oxide thickness (t_{OX}) and the NLD thickness (t_{NLD}) were set at 40 nm and 240 nm, respectively. The performance of this proposed structure was compared to a reference structure with a gate oxide thickness of 50 nm, which is the typical thickness for 1.2 kV SiC MOSFETs. The comparative analysis of the two structures is presented in Figs. 4 and 5, witnessing a good agreement between the proposed and reference structure both sub-threshold and over-threshold.

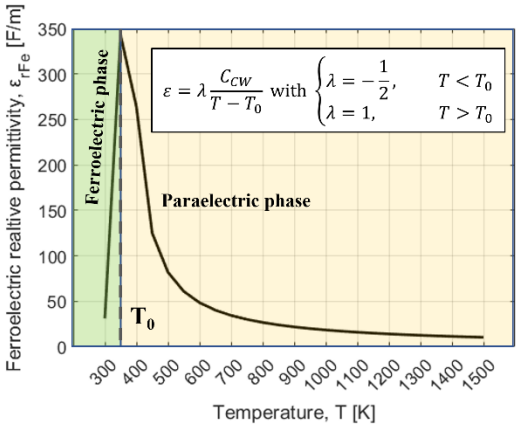

Fig. 2. Relative dielectric permittivity of the ferroelectric material P(VDF–Trifle), used to model the non-linear dielectric. Inset of the figure: general analytical model of the relative dielectric permittivity of a ferroelectric material.

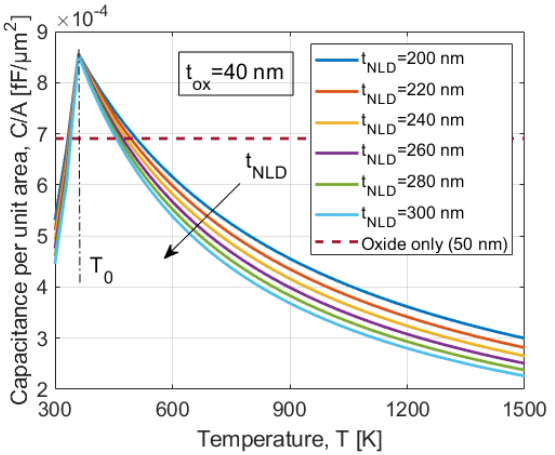

Fig. 3. Oxide/NLD stack capacitance keeping the oxide thickness (tox) fixed and varying both temperature and NLD thickness. As the temperature rises, the capacitance of the stack increases until it reaches the Curie temperature, T_0. Beyond T_0, the capacitance starts to decrease with further increases in temperature. Additionally, the capacitance decreases as the NLD thickness increases.

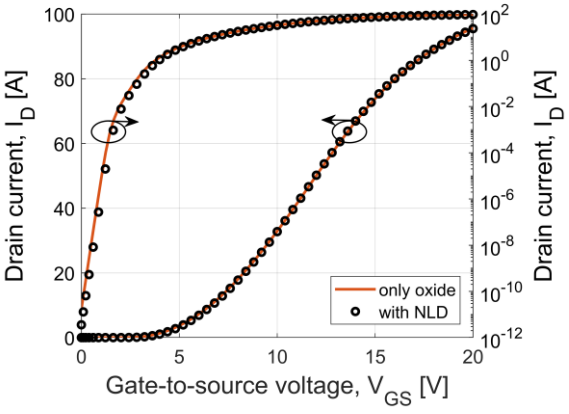

Fig. 4. Comparison between isothermal transfer characteristics of the reference MOSFET (with a 50 nm-thick oxide as gate insulator) and the proposed design (with the oxide/NLD stack, t_{ox}=40 nm and t_{NLD}=240 nm) at T=340 K (V_{DS}=20 V).

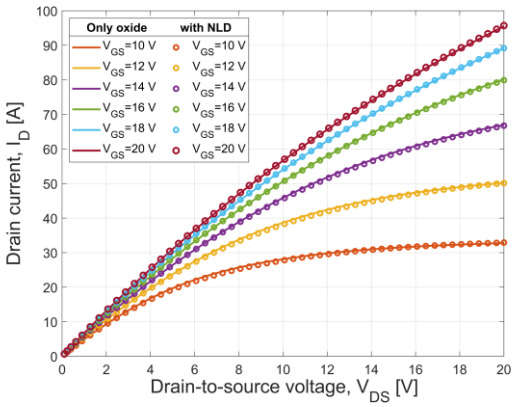

Fig. 5. Comparison between isothermal output characteristics of the standard MOSFET (with a 50 nm thick oxide as gate insulator) and the proposed design (with the oxide/NLD stack, t_{ox}=40 nm and t_{NLD}=240 nm) at T=340 K..

RESULTS AND DISCUSSION

Short-circuit behaviour

To evaluate the performance of the proposed design in short-circuit scenarios, mixed mode electrothermal simulations were conducted [7]. The circuit used for the short-circuit simulations is reported in Fig. 6. In this setup, a pulse source is connected to the gate terminal to allow the current flow into the device, while a constant supply voltage (V_{BUS}) is connected to the drain terminal. To account for thermal effects arising during the transient operation, a thermal resistance (R_{TH}) of 0.01 cm^^{2}K/W is connected to the drain terminal. Moreover, to address parasitic elements introduced by wires and connections, additional stray inductances of 7 nH and 40 nH are integrated into the circuit, connected to the source and drain terminals, respectively. The test was performed with a gate-to-source voltage (V_{GS}) of 18 V and a V_{BUS} of 800 V, with an on-state time (T_{ON}) of 5 µs. As shown in Fig. 7, the proposed structure demonstrates better short-circuit performance, with a maximum temperature 40% lower than that of the reference structure (1230 K instead of 2050 K). Furthermore, the proposed structure exhibits a notable absence of the change in slope at the end of the SC pulse, which is commonly observed in the standard structure [8]. This absence is attributed to the lower temperature reached in the proposed design. As a result, the risk of failure due to thermal runaway is mitigated significantly. These observations are corroborated by the current density of electron and hole, observed at 5.5 µs (i.e., at turn-off) and reported in Fig. 8. Regarding to the structure with the NLD stack, the hole current density distributions (Fig. 8(a, c)) witness a lower current conducted, while the electron current density distributions (Fig. 8(b, d)) show a decrese in the generations of the holes in the body body region, compared with the standard one.

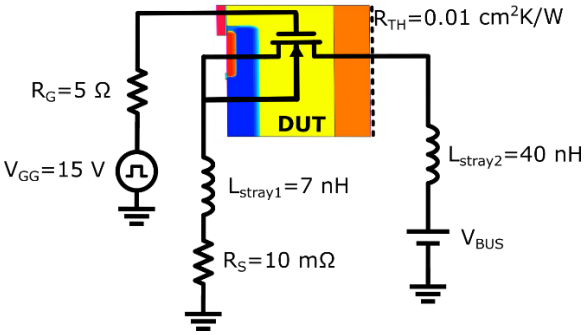

Fig. 6. Mixed-mode circuit for the electrothermal simulation of shortcircuit. RG=5 Ω, RS=10 mΩ, Lstray1=7 nH, Lstray2=40 nH. A thermal resistance (RTH) of 0.01 cm2K/W is set on the drain contact.

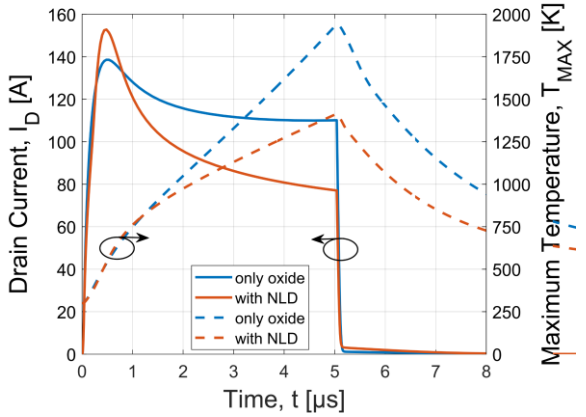

Fig. 7. Short-circuit waveforms for a supply voltage of 800 V applied for 5 µs. The proposed structure reaches a maximum temperature more than 500 K lower than the standard structure.

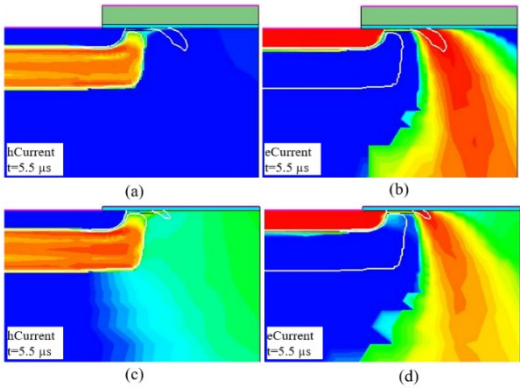

Fig. 8. Holes current density (a), (c), and electrons current density (b), (d) at t=5.5 µs for the proposed structure (top) and standard structure (bottom) for a SC test at 800 V.

Threshold voltage temperature dependence

In Fig.6, the temperature dependence of the threshold voltage of proposed structure and standard structure is shown. The threshold voltage was extracted as the voltage at which the electron density value in the channel reached the ionized acceptor concentration. The analysis was performed for a V_{DS} of 0 V, in order to eliminate two-dimensional effects. When the temperature reaches high

values (e.g., for T>600 K), V_{TH} of NLD-stack structure becomes lower than standard structure due to the increasing influence of the NLD. However, such a small discrepancy cannot be responsible for the short-circuit capability enhancement.

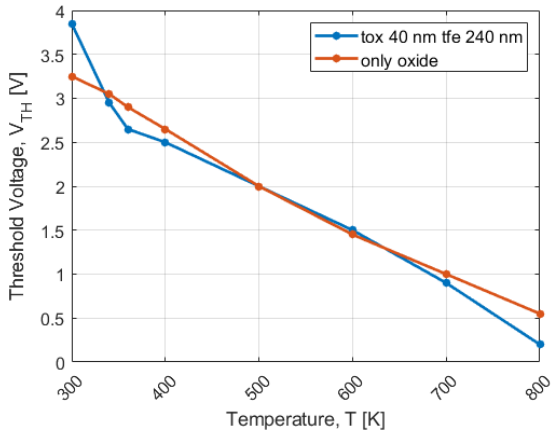

Fig. 9. Threshold voltage comparison varying temperature between proposed structure and reference

CONCLUSION

In this work, it has been shown how replacing the standard gate oxide of a 1.2 kV SiC MOSFET with a oxide/NLD stack would improve its short-circuit capability, since the temperature increase of the device is lowered of about 40% compared with a MOSFET with a standard gate oxide. Since the variation of the threshold voltage with temperature does not present substantial variation between standard and proposed structures, the improved behaviour is dominated by the variation of the capacitance on the current.

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