Annealing behavior of Pt and PtH defects in fully process 1.2kV Si diodes covering the whole substrate thickness

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Abstract

We present an annealing study of the platinum-hydrogen (PtH) defect complex on fast recovery silicon (Si) high voltage diodes. These specially processed test diodes were annealed in nitrogen ambient at three different annealing temperatures for 30 min, respectively. Before and after this annealing step the substitutional platinum (Pt) and platinum-hydrogen concentration within the entire space charge region (SCR) were characterized using high-voltage current deep level transient spectroscopy. The annealing impacts the investigated trap levels as previously found in bulk Si samples. For annealing temperatures above 250°C the PtH starts to dissociate partly and at 330°C almost no PtH can be found anywhere inside the entire SCR. For the annealing at 300°C additionally an increase of the PtH concentration in the proximity of the pn-junction is observed which is most likely due to the presence of a hydrogen source located at the front side of the diodes. Furthermore, a clear correlation between the leakage currents and the PtH depth profiles suggests strongly that the PtH is the major carrier generation center in the investigated samples.

Keywords: Silicon, diode, Platinum, Platinum-Hydrogen, lifetime control, high voltage, DLTS

INTRODUCTION

In modern silicon (Si) fast-switching power diodes minority carrier lifetime control is inevitable for an efficient switching performance [1, 2, 3]. For this, additional energy levels within the band gap of Si are deliberately introduced by either high-energy particle irradiation [4, 5] or doping with noble metals as platinum (Pt) [1, 6] or gold (Au) [7, 8]. These trap levels act as recombination centers and hence reduce the carrier lifetime. Additionally, they increase the forward voltage drop V_F as well as the leakage current I_R [1]. As an increased leakage current of the diode adds to switching losses in a freewheeling diode application (e.g. with a parallel IGBT [9]) the smallest possible I_R is desired. Au and electron irradiation both result into higher I_R compared to Pt [1, 2, 10] and regarding switching behavior Pt and Au are the better choice compared to electron irradiation [1]. Therefore, Pt is often the choice for life time adjustment [1] as the low reverse currents also enable the increase of the junction temperature. For substitutional Pt (Pt_{Si}) in Si three electrically active charge transition levels are reported in literature with (E_C – 0.23) eV, (E_V + 0.09) eV and (E_V + 0.33) eV [11]. So, for an optimized minority carrier lifetime a precise control of the Pt_{Si} distribution within the space charge region (SCR) is crucial. The platinum-hydrogen (PtH_{Si}) defect complex is often observed in Pt doped devices [3], as hydrogen (H) is present in many process steps during device fabrication. As the energy of the $PtH_{Si}^{-/0}$ charge transition level (E_C – 0.5) eV [12] is close to the middle of the bandgap of Si, it acts as an efficient generation center and thereby is a main source for leakage currents. Hence, a detailed understanding of the spatial distribution and the temperature dependency of this defect level is key to optimize modern Pt doped Si diodes. Sachse et al. [11] studied the annealing behavior of four different PtH related trap levels in n- and p-type Si with Deep Level Transient Spectroscopy (DLTS) measurements via a Schottky contact. Their studies give a detailed picture of the transitions between the different PtH complexes as well as the dissociation of these complexes in Pt doped Si wafer. Rasinger et al. [13] used fully processed Si diodes for the investigation of the temperature stability of the PtH. In contrast to their studies we investigated the $PtH_{Si}^{-/0}$ and $Pt_{Si}^{-/0}$ concentration within the entire SCR whereas former DLTS measurements where limited to the proximity of the pn-junction.

EXPERIMENTAL PROCEDURE

For this study specifically processed Si high-voltage (HV) test diodes without a field stop (FS) implantation [14] were fabricated. The as such processed devices have a deliberately high contamination with H from several different process steps after the Pt doping and thus impact the Pt defect complexes significantly. During device fabrication the Pt is diffused by an annealing step after the Pt doping. This diffusion step has a significantly higher temperature budget than the additional annealing steps which were executed on the fully processed diced devices. For the additional annealing steps the diodes were placed inside a furnace with N_2 ambient and annealed at 250°C, 300°C and 330°C for 30 min, respectively.

Before and after the annealing depth profiles of the concentration of the $Pt_{Si}^{-/0}$ and the $PtH_{Si}^{-/0}$ within the entire SCR were measured using HV-Current Deep Level Transient Spectroscopy (HV-IDLTS) [14, 15]. For IDLTS [16] three voltages pulses are applied consecuitevely: the first pulse V_R sets the width of the SCR during which all traps inside the SCR are discharged. The second pulse $|V_F| < |V_R|$ reduces the volume of the SCR and hence some of the previously emptied traps are filled. After this the voltage is switched back to V_R, the traps emit the captured charge carriers and the resulting current transient is measured. As this emission process is strongly dependent on temperature, this pulse sequence is repeated over a large temperature range to characterize trap levels with different activation energies (E_a) and capture cross sections.

Our measurement setup [15] uses a Keithley 2636B with a voltage range of 200 V and a cryogenic probe station. For the measurement the temperature is ramped starting from 20 K up to 300 K and the current transients are measured continuously. The filling and the reverse bias for every IDLTS measurement is chosen to obtain the same measurement volume for each voltage pair. The measurement volume closest to the pn-junction uses $V_F = 0$ V and $V_R = 3$ V and the highest voltage pair is $V_F = 88$ V and $V_R = 107$ V. For $V_F > 107$ V the electric field reaches the backside of the investigated diodes. With these IDLTS measurements we can identify all electrically active defects before and after the annealling steps on the fully processed devices as well as their concentration throughout the entire substrate thickness.

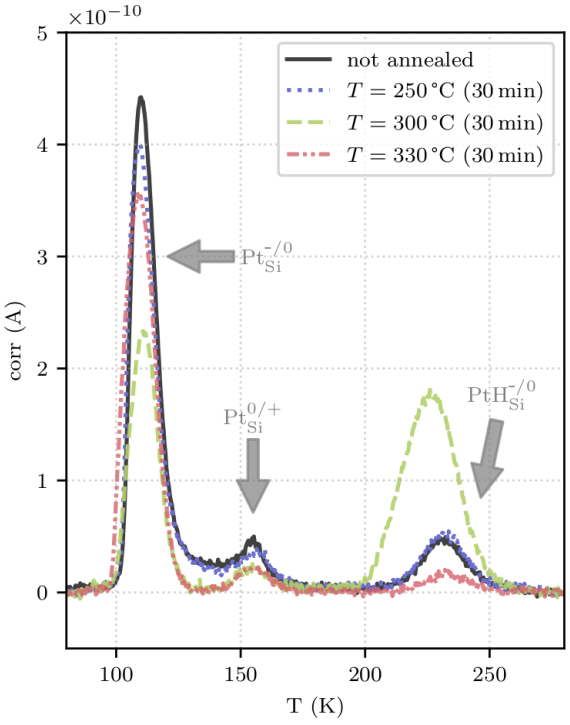

Figure 1: IDLTS of a not annealed sample and the samples annealed at T=250°C, 300°C and 330°C. All four IDLTS spectra show three peaks which are assigned to two different charge states of Pt_{Si} and one to PtH. The spectra were measured with $V_F = -3$ V and $V_R = -9$ V. The filling pulse was applied for $t_F = 100$ ms and the reverse pulse for $t_R = 500$ ms.

Assignment	E_a in eV	E_a in eV Literature values
$Pt_{Si}^{-/0}$	$E_C - 0.22 \pm 0.03$	$E_C - 0.23$ [11, 17]
$PtH_{Si}^{-/0}$	$E_C - 0.51 \pm 0.02$	$E_C - 0.5$ [11, 12]
$Pt_{Si}^{0/+}$	$E_V + 0.31 \pm 0.03$	$E_V + 0.33$ [11] $E_V + 0.314$ [17]

Table 1: Measured activation energies as determined by IDLTS measurment and literature values used for trap level identification.

EXPERIMENTAL RESULTS AND DISCUSSION

The IDLTS spectra close to the pn-junction show three different peaks which are assigned to the $Pt_{Si}^{-/0}$ (109 K), $Pt_{Si}^{0/+}$(157 K) and $PtH_{Si}^{-/0}$(243 K) as shown in Figure 1. The corresponding Arrhenius energies used for the trap level assignment are summarized in Table 1 together with the literature values. For the depth profile investigations, we focus on the majority carrier charge transition levels because the biasing is always in the reverse direction of the diode and hence this measurement procedure is not suited to investigate minority carrier trap levels.

In figure 2 the depth profiles before and after the annealing step at 330°C are shown. Before the annealing $Pt_{Si}^{-/0}$ is mainly located close to the pn-junction and especially in the middle of the SCR the $PtH_{Si}^{-/0}$concentration is highest. After the annealing at 330°C the $PtH_{Si}^{-/0}$ nearly vanishes while the $Pt_{Si}^{-/0}$ is now detectable in the entire SCR. The $Pt_{Si}^{-/0}$ and the $PtH_{Si}^{-/0}$ are the only majority carrier defect levels present in the investigated sample. Hence, the sum of $Pt_{Si}^{-/0}$+ $PtH_{Si}^{-/0}$before the annealing is compared to the depth profile of $Pt_{Si}^{-/0}$ after the annealing.

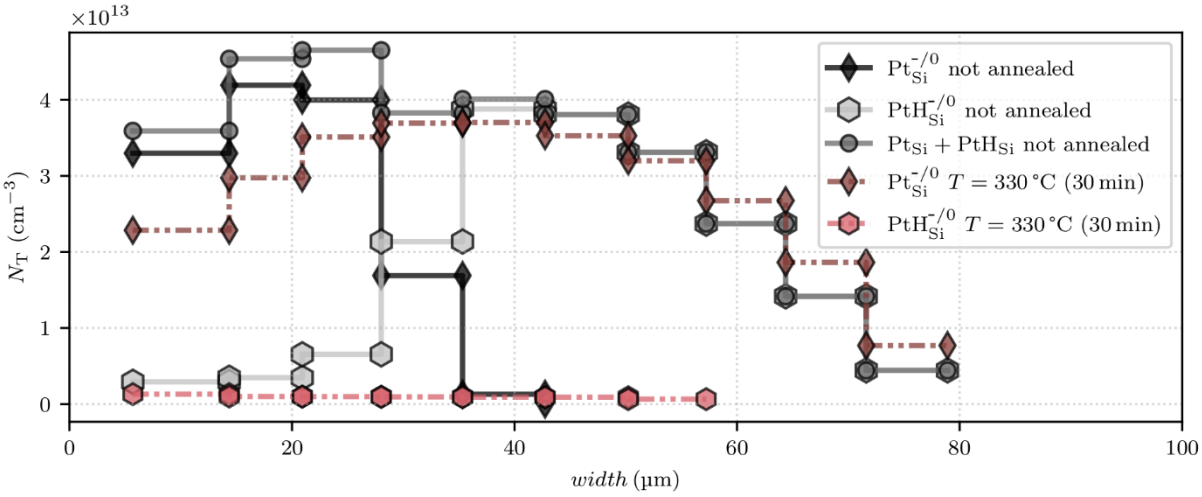

Figure 2: Depth profiles of the $Pt_{Si}^{-/0}$ and $PtH_{Si}^{-/0}$ before and after an annealing step at 330°C for 30 min using HV-IDLTS. For the not annealed sample also the sum of the two majority carrier traps is included. The depth profiles for the $Pt_{Si}^{-/0}$ as well as for the $PtH_{Si}^{-/0}$ change signifcantly by this anneal. After the anneal almost no $PtH_{Si}^{-/0}$ is detected and the $Pt_{Si}^{-/0}$ depth profile matches with the $Pt_{Si}^{-/0} + PtH_{Si}^{-/0}$ depth profile before the anneal.

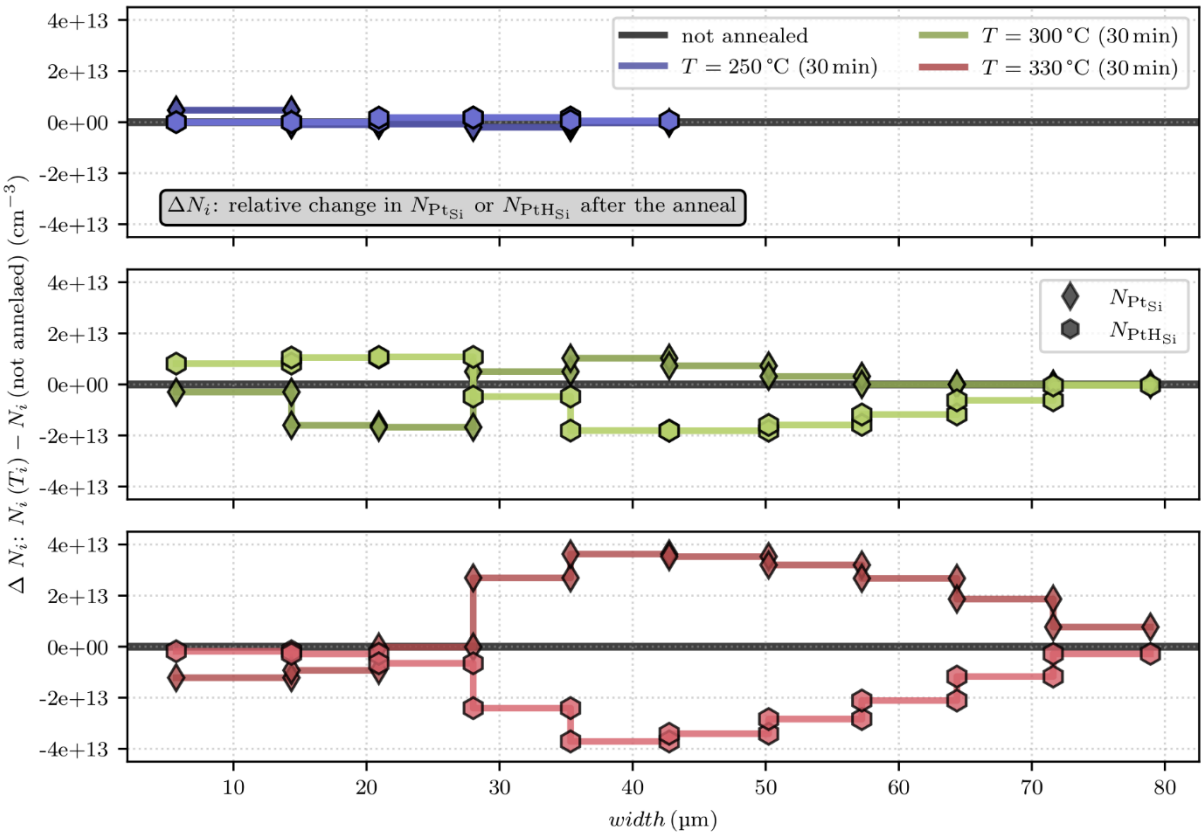

Figure 3: The difference of the $Pt_{Si}^{-/0}$(diamonds) and $PtH_{Si}^{-/0}$ concentration after the different anneals compared to the not annealed sample. A positive ΔN_i (eq. (1) and (2)) indicates a larger concentration of the defect level after the annealing step and vice versa for a negative ΔN_i. For the smallest annealing temperature of 250°C the concentration of both charge transition levels does not change. For the anneal at 300°C $N_{Pt_{Si}}$ decreases at the beginning of the SCR which is correlated to an increase of $N_{PtH_{Si}}$. In the middle of the SCR $N_{Pt_{Si}}$ is increased indicating a partial dissociation of the PtH. The increasing $PtH_{Si}^{-/0}$ concentration is suspected to be linked to a hydrogen source located at the frontside of the device. The annealing at T=330 °C clearly shows a dissociation of the $PtH_{Si}^{-/0}$ into $Pt_{Si}^{-/0}$ as the curves are almost symmetric around zero for a width > 27 µm. The decreased $Pt_{Si}^{-/0}$ concentration in the proximity of the pn-junction could possibly be linked to an out-diffusion of the Pt as described in [6, 18].

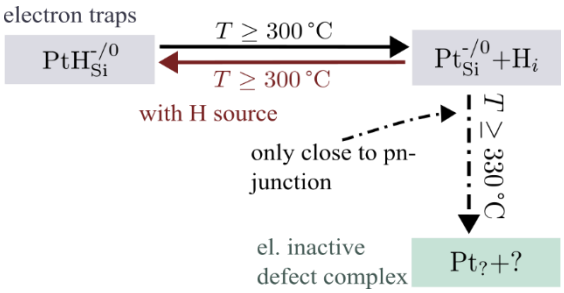

Figure 4: Summary of observed transitions of the $Pt_{Si}^{-/0}$ and the $PtH_{Si}^{-/0}$ for annealing temperatures $T \geq 300$ °C and $t = 30$ min. For smaller annealing temperatures no change of the $Pt_{Si}^{-/0}$ and the $PtH_{Si}^{-/0}$ defect concentration was observed. The reaction of $Pt_{Si}^{-/0}$ + H is only possible if H is available. In the investigated samples the frontside metallization is suspected to act as such a source for $T \geq 300$ °C. For the anneal at 330 °C the dissociation of $PtH_{Si}^{-/0}$ outweighs and $N_{PtH_{Si}}$ is significantly reduced within the entire SCR. A decrease of the $Pt_{Si}^{-/0}$ concentration is observed for $T = 330$ °C in the proximity of the pn-junction. This indicates a transformation of the electrically active Pt_{Si} into an electrically inactive defect complex which could be interstitial Pt_i.

These two depth profiles match almost perfectly indicating a dissociation of the $PtH_{Si}^{-/0}$ to $Pt_{Si}^{-/0}$ + H over the entire SCR width/substrate thickness which is in accordance with previous annealing experiments [11, 13].
For a more detailed analysis of the different annealing temperatures T_i on the $Pt_{Si}^{-/0}$ and the $PtH_{Si}^{-/0}$ concentrations the difference in trap concentration is plotted with the not annealed sample as reference:

$$\Delta N_{Pt_{Si}} = N_{Pt_{Si}}(T_i) - N_{Pt_{Si}}(\text{not annealed}), \quad (1)$$

$$\Delta N_{PtH_{Si}} = N_{PtH_{Si}}(T_i) - N_{PtH_{Si}}(\text{not annealed}). \quad (2)$$

The depth profile of $\Delta N_{Pt_{Si}}$ and $\Delta N_{PtH_{Si}}$ is shown in Figure 3 for each annealing temperature, respectively. The annealing temperature of 250°C seems to not affect the two charge transition levels $Pt_{Si}^{-/0}$ and $PtH_{Si}^{-/0}$ as $\Delta N_{Pt_{Si}}$ as well as $\Delta N_{PtH_{Si}}$ is close to zero within the entire measurement volume.
For the two higher annealing temperatures both $\Delta N_{Pt_{Si}}$ and $\Delta N_{PtH_{Si}}$ depth profiles change significantly. For $T = 300$ °C the $Pt_{Si}^{-/0}$ concentrations decrease for the first three measurement volumes and is increased in the middle of the SCR and vice versa for the $PtH_{Si}^{-/0}$. These two contrary trends could indicate a hydrogen source located at the frontside of the chip which becomes active for $T \geq 300$ °C leading to an increase of $PtH_{Si}^{-/0}$ close to the pn-junction. A possible hydrogen source could be the frontside metallization. The assumption of the hydrogen source located at the frontside is supported by the decrease of $PtH_{Si}^{-/0}$ further inside the device. This suggest a partly dissociation of the $PtH_{Si}^{-/0}$ into $Pt_{Si}^{-/0}$ + H which is at slightly lower temperatures than previously described with $T > 327$ °C for a 60 min anneal [11].
For the highest annealing temperature of 330 °C an almost complete dissociation of the $PtH_{Si}^{-/0}$ into $Pt_{Si}^{-/0}$ + H is observed as discussed previously in Figure 2. Apart from this mechanism a decrease of $N_{Pt_{Si}}$ is observed in the proximity of the pn-junction. Thus, an additional minority carrier transient spectroscopy (MCTS) measurement was performed covering the first two measurement volumes with $V_F = +1$ V and $V_R = -7$ V. This spectrum does not show additional minority carrier traps for the sample annealed at $T = 330$ °C. These experimental results indicate a transformation of

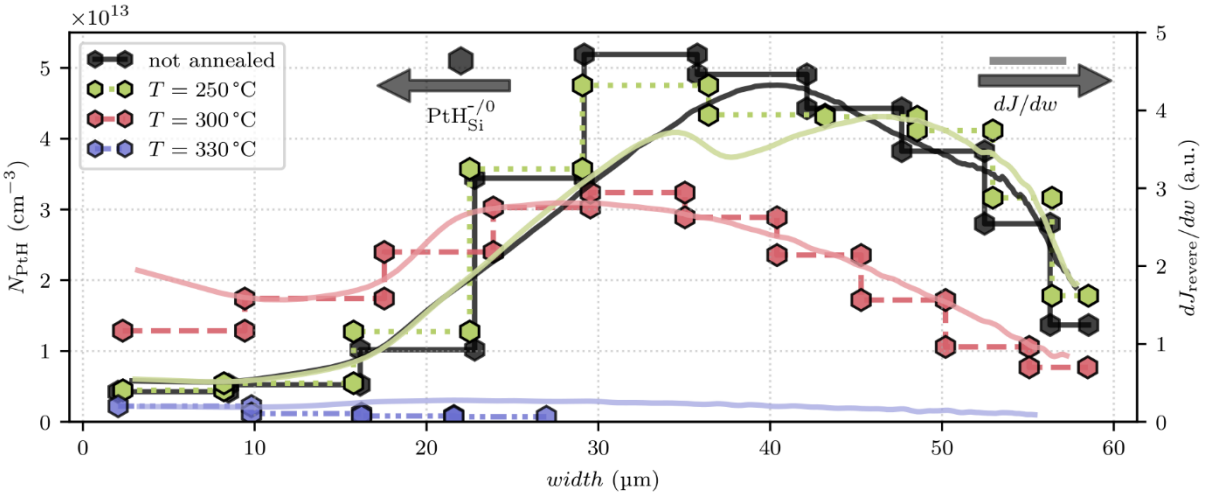

Figure 5: Depth profile of the $PtH_{Si}^{-/0}$ obtained from HV-IDLTS (hexagons and left hand-side y-axis) and the depth profile from the derivative dJ/dw from reverse IV measurements (solid lines and right hand-side y-axis). For each sample these two differently obtained depth profiles match almost perfectly which strongly suggest that the $PtH_{Si}^{-/0}$ charge transition level is the main source of leakage current in these devices. Furthermore, an increase of the $PtH_{Si}^{-/0}$ as well as for the leakage current close to the pn-junction is observed for the sample annealed at 300°C.

electrically active substitutional Pt_{Si} into an electrically inactive defect or defect complex during this anneal, as the temperature is well below the diffusion temperature of Pt [1]. In [6, 18] a reduction of the $Pt_{Si}^{-/0}$ concentration close to the pn-junction is described in dependence on the cool down rate of the Pt diffusion. They suggest an *out-diffusion* of the Pt due to a transition of substitutional Pt_{Si} into interstitial Pt_i (electrical inactive) by the reverse Frank-Turnbull and reverse kick-out mechanism. Even though the temperature budget of our annealing temperatures is significantly smaller we suspect a similar mechanism of the decreased $Pt_{Si}^{-/0}$ concentration.
A summary of the observed transitions for the different annealing steps is given in Figure 4.

Apart from the annealing behavior of the $PtH_{Si}^{-/0}$ we also investigated the correlation between the leakage current and the $PtH_{Si}^{-/0}$ depth profiles for each annealing step. For this we obtained the depth profile of the major generation center from reverse current voltage (IV) characteristic by calculating dJ/dw [9]. These two differently calculated depth profiles are both shown in Figure 5. For all different annealing temperatures, a strong correlation of these two differently obtained depth profiles is observed. This indicates that the $PtH_{Si}^{-/0}$ is the major generation center in all samples which is in accordance with previous reports on fully processed Pt doped HV-Si diodes [13, 19].

CONCLUSION

By using HV-IDLTS we could analyze the annealing behavior of the PtH on fully processed diodes throughout the complete substrate thickness. For the smallest annealing temperature of 250°C we did not see a change of the defect concentrations. For all higher annealing temperatures, we obtain different annealing results depending on the distance to the pn-junction as well as on the annealing temperature. For the anneal at 300°C we observe a partly dissociation of the $PtH_{Si}^{-/0}$ in the middle of the SCR and an increasing $PtH_{Si}^{-/0}$ concentration close to the pn-junction. This indicates a H source at the frontside of the fully processed diodes which becomes active during the anneal. For the highest annealing temperature of 330°C we obtain an almost complete dissociation of the $PtH_{Si}^{-/0}$ as the remaining $PtH_{Si}^{-/0}$ concentration is comparable small and the $Pt_{Si}^{-/0}$ depth profile after the anneal correlates strongly with the $Pt_{Si}^{-/0} + PtH_{Si}^{-/0}$ depth profile before the anneal. In the proximity of the pn-junction we observe a smaller $Pt_{Si}^{-/0}$ concentration after the anneal. We suspect a transformation of the electrically active substitutional Pt_{Si} into electrically inactive interstitial Pt_i as described in [6, 18]. Furthermore, the almost perfect match of the $PtH_{Si}^{-/0}$ depth profiles from HV-IDLTS with the depth profiles calculated from reverse IV measurements indicates strongly that the major generation center is the $PtH_{Si}^{-/0}$ in all samples.

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