Scalable Vertical GaN FETs (SV- GaN FETs) for Low Voltage Applications

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Abstract

This is the first report on a novel multi-polarization channel applied to realize normally-off and high-performance vertical GaN device devices for low voltage applications. This structure is made with 2DHG introduced to realize the enhancement mode channel instead of p-GaN as in conventional vertical GaN MOSFETs. As the 2DHG depends upon growth conditions, p-type doping activation issues can be overcome. The Mg-doped layer is only used to reduce the short-channel effects, as the 2DHG layer is too thin. Two more 2DEG layers are formed through AlGaN/GaN/AlGaN/GaN polarization structure, which minimizes the on-state resistance. Simulation analysis shows that this proposed structure can provide a large drain current at ~ $500\ mA/mm$ level. The calculation results show this novel vertical GaN MOSFET – termed as SV GaN FET - has the potential of breaking the GaN material limit in the trade-off between area-specific on-resistance ($R_{(on,sp)}$) and breakdown voltage at low voltages.

Keywords: 2DEG, 2DHG**,** Low Voltage, Scalable Vertical GaN FETs (SV- GaN FETs)

INTRODUCTION

Due to its capability for higher efficiency, Gallium Nitride (GaN) is widely considered as the next generation pervasive semiconductor that can help address global challenges of climate change, energy security, health, and connectivity. Replacing silicon with GaN has the potential to reduce power loss by 80%, chip size by 90% at 600V and meet the performance/cost parity demanded by Integrated Circuit (IC) industry. Moreover, GaN has great potential to reduce cost because GaN device can be fabricated on epitaxy grown substrate that is larger and less expensive than Silicon Carbide (SiC).

Polarization Super Junction (PSJ) technology has been recently introduced and applied on GaN HEMT devices. It breaks the trade-off between area-specific on-resistance ($R_{(on,sp)}$) and breakdown voltage in lateral formats [1, 2]. However, in most lateral GaN transistors, threshold voltage could not be increased to a high enough level (except through cascode approach) to satisfy the requirement of automotive applications [3]. For high-frequency applications, dynamic on-resistance in lateral GaN devices can degrade device/system efficiency due to increased conduction losses [4]. Besides, most lateral GaN devices are not as area-efficient as vertical GaN transistors since sufficient length between the gate and drain electrodes is necessary to achieve high blocking capability [5]. In vertical GaN MOSFET technology, p-type GaN is usually doped by magnesium (Mg) and the percentage activation of this impurity rarely exceeds 1%. Moreover, the fabrication and performance of high voltage GaN MOSFET structures are dependent on p-GaN doping techniques [6, 7]. To overcome such technical limitations, our innovative idea is to expand the PSJ concept to Scalable Vertical (SV) GaN FETs.

VERTICAL DEVICE STRUCTURE AND DEVICE SIMULATION

Silvaco TCAD is used for 2D device simulation of SV-GaN FETs. The models adopted for simulating I-V characteristics includes POLAR (spontaneous polarization), CALC.STRAIN (piezoelectric polarization) and FLDMOB (field-dependent mobility).

Fig. 1 shows a simplified SV- GaN FET with $10\text{nm} - Al_{0.05}Ga_{0.95}N$ / $5nm - GaN$ / $10\text{nm} - Al_{0.05}Ga_{0.95}N$ / $5nm - GaN$ channel. There are two 2DEG layers: the

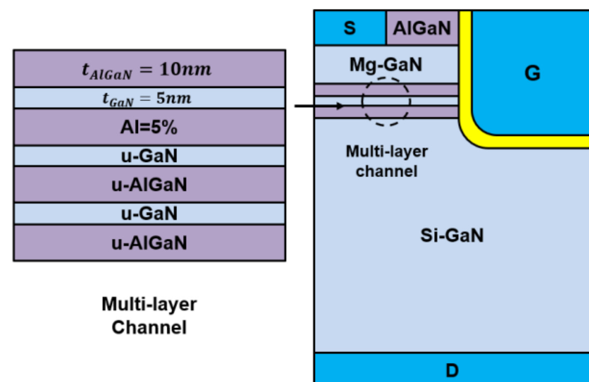

Fig. 1. Multi polarization channel vertical GaN device cross-section

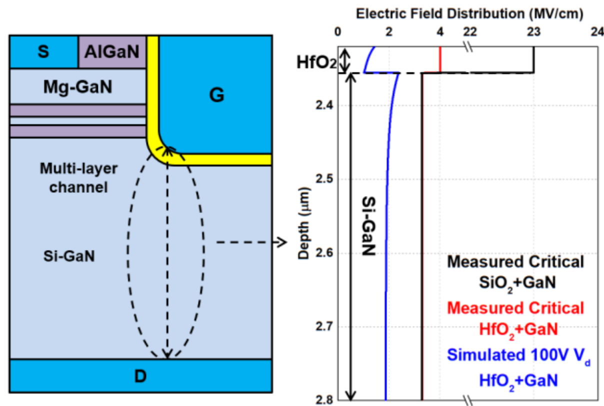

Fig. 2 Gate corner electric field distributions: simulated results vs. measurement material critical electric field [8, 9].

upper layer is connected to the source electrode while bottom 2DEG layer is connected to drain electrode. 2DHG presence in multi-layers is regarded as the channel with the function of realized normally off and controlled threshold voltage. 2DEG and 2DHG sheet carrier density can be controlled by adjusting AlGaN layer thickness and Al mole fraction.

The channel design of multi-layer stacks utilizes a charge compensation concept between the adjacent 2DEG and 2DHG layers to support voltage. The applied voltage is dropped across the stack as well as the Si-doped GaN drift region. BV can be scaled by increasing the number of multi-layer stacks or optimizing the thicknesses of the stacks. In trench gate vertical devices, corner design is an important issue that affects operation reliability. In this work, reported data of measured critical electric field strength of ~ $4MV/cm$ ($23MV/cm$) for HfO_2 (SiO_2) and $3.3MV/cm$ for Si-GaN is used as the reference values and U-shaped design is considered for the gate geometry to suppress corner effects [8, 9].

Fig. 2 shows that a SV- GaN FET device with $0.5\mu m$ Si-GaN drift region is simulated at 100V drain voltage, the peak electric field is the only 2/3rd of the reference value. Moreover, other techniques such as p-GaN underneath the gate can further electrically shield the gate corners. As shown in Fig. 3, an Mg-doped GaN region applied

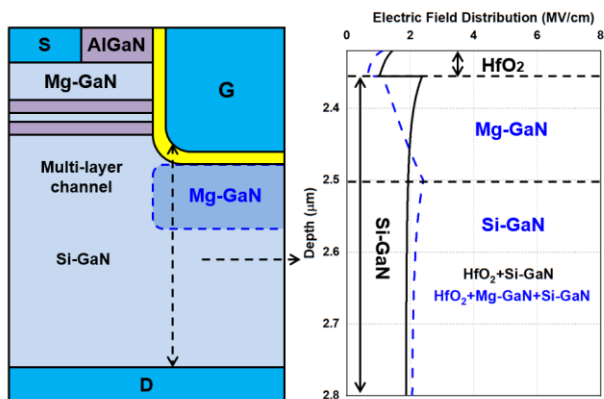

Fig. 3 Gate corner electric field distributions: Si-GaN vs. Mg-GaN+Si-GaN at $V_d = 100V$.

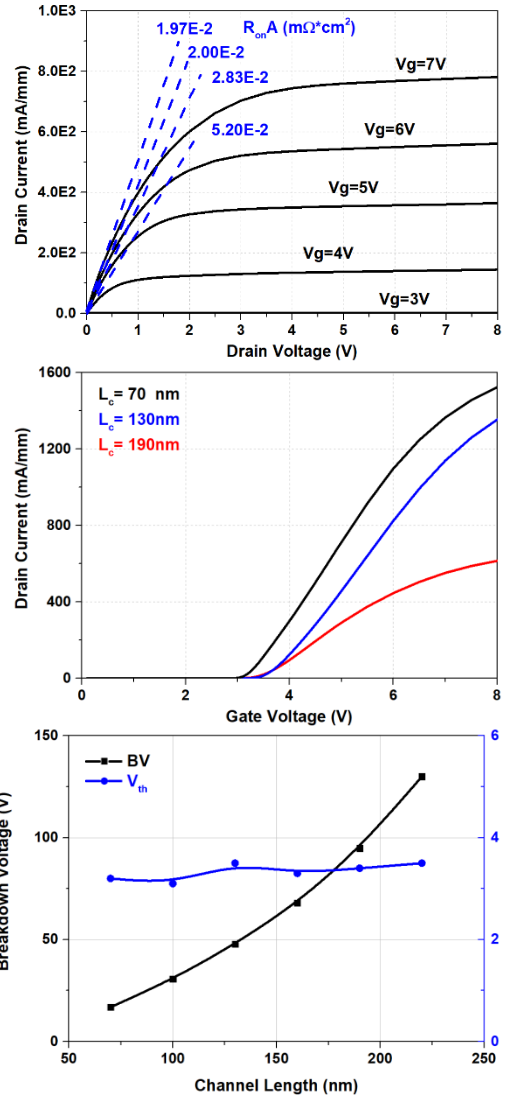

Fig. 4 Simulated (a) $160\mu m$ channel $I_d - V_d$ characteristics. (b) Transfer I-V characteristics. (c) Channel length vs BV and V_{th}

beneath the trench gate can further suppress the electric field crowding at the corner of the gate.

Fig. 4(a) shows the $I_d - V_d$ characteristics as a function of gate voltage. With the increasing number of multi-polarization junction stacks, device blocking capability can be improved without any significant increase in V_{th}, as shown in Fig. 4(c).

In Fig. 5, for comparison, 4H-SiC and GaN material theoretical limits are demonstrated as well as conventional GaN HEMT with $1\mu m$ channel length [10]. The calculation results show a performance beyond the material limit by assuming ideal channel mobility of $1000\ cm^2/Vs$. The simulation results for SV-GaN FETs predict significantly superior performance to conventional lateral GaN HEMT, albeit practical carrier mobility is utilized for calibration. Vertical GaN devices based on PSJ concept will be a promising candidate for the next generation of power electronics.

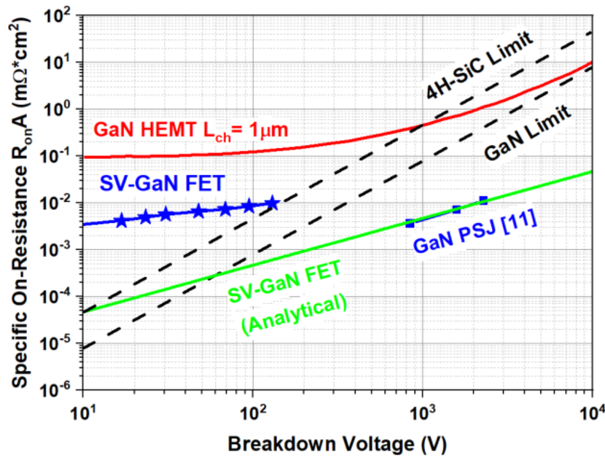

Fig. 5 Area-specific on-resistance vs. Breakdown trend in GaN and SiC; for reference vertical GaN PSJ technology [10] is shown as well as the predicted trend of SV-GaN FET.

CONCLUSIONS

A novel vertical GaN MOSFET technology, which can be scaled and suitable for low voltage applications, is presented herein. A 100V device can potentially achieve a $R_{(on,sp)}$ lower than $10^{-2} m\Omega \cdot cm^2$ as shown in this work. The device can be easily scaled, and the specific on-state resistance can be further optimized with more refined design rules. Based on the results presented, the multi-polarization channel vertical GaN device are predicted to offer immense potential in power electronic systems and high frequency integrated applications.

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