Commercial Sweet Spots for GaN and CMOS Integration by Micro-Transfer-Printing

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Abstract

Several approaches for close integration of power switches with CMOS logic are subject of technical evaluations and academic discussions. This paper identifies the commercially relevant processing steps of different integration methods (HV and SOI CMOS, monolithic integration in SOI and in GaN, Direct Wafer Bonding, micro-Transfer-Printing of GaN on CMOS and CMOS on GaN) and compares them on simple cost per wafer and cost per chip models. Four examples of real ICs verify the simple costs per chip model. Commercially attractive high voltage to logic partitionings are identified for the different integration approaches.

Keywords: heterogeneous integration, monolithic integration

MOTIVATION

The need for better efficiencies of power supplies and inverters with smaller footprints can be met with Wide Band Gap (WBG) power devices like Gallium-Nitride (GaN) High Electron Mobility Transistors (HEMTs) with lower on-state and dynamic losses capable to switch at higher frequencies. Several approaches for close-by integration of GaN power switches together with silicon based CMOS driver and controller logic are on the market or subject of technical evaluations and academic discussions.
The package parasitics, namely the package lead inductance, bond wire length related inductances and resistances, as well as the PCB trace inductances are a serious obstacle to the high-speed switching, which is necessary in order to reduce the switching power losses or reduce the size of power converters [1], [2], [3], [4].
While academic research is and has to be done in all fields further industrial development can only occur within commercially promising areas. Therefore commercial boundary conditions impose economic limits to the usability of the different integration approaches depending heavily on the potential applications.

INTEGRATION APPROACHES AND RELATED COSTS

Partitioning

The addition of power switches to a CMOS logic can be realized in many different process technologies ranging from silicon based CMOS technologies to monolithically integrated GaN or silicon solutions. But for most solutions in general the costs for substrate, epitaxy, manufacturing and wafer test are per wafer. The costs per chip additionally include the number of good dies defined by the chip size and yield figures. Both cost figures are independent from the aerial usage of dedicated process steps. This so called partitioning problem is shown in Figure 1 for the example of a monolithic GaN integration into a silicon based CMOS logic technology. The full processing expenses e.g. for the GaN Metal Organic Chemical Vapour Deposition, MOCVD, are incurred independent if the IC contains only small or large GaN areas.
With a small GaN area all the GaN related costs are for a very small functional area, with a very high GaN area the costs per logic functionality get very high. Similar problems occur for dedicated high voltage or low voltage CMOS processing steps or mask layers which are used only in small parts or in only a few devices in the IC – but of course with much smaller values compared to GaN MOCVD epitaxy.
So when looking at costs per functionality, this implies acceptable costs structures for many integration approaches only for evenly distributed area usage but, very high costs levels e.g. in the mentioned example when integrating only one very small GaN high voltage switch.

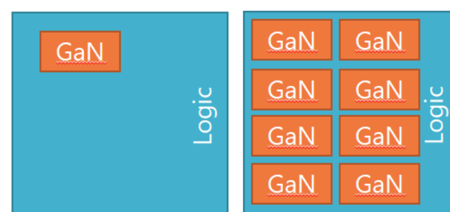

Figure 1: Partitioning problem for the example of monolithic GaN integration into a silicon CMOS chip, left: low GaN usage, right: low logic usage

Bulk CMOS

Already with standard CMOS technologies just by adding dedicated HV implants or gate oxides low side n- and p-channel enhancement and depletion transistors with operating voltages above 600V can be realized. With more specialized and dedicated CMOS or Bipolar CMOS DMOS (BCD) processes also high side configurations even above 600V can be manufactured.
Costs to be taken into account are the substrate material including the epitaxy and the processing costs depending on the complexity of the process. Both costs are area independent.

SOI CMOS

Replacing the bulk or epitaxial substrates by SOI wafers higher performance and high side capability can be achieved at the expense of higher wafer costs.
Costs to be taken into account are the SOI substrate material and the processing costs with both costs being area independent.

Monolithic integration in SOI

For the monolithic integration of GaN HEMTs on a silicon CMOS wafer several approaches have been discussed in the literature [5], [6], [7], [8]. A promising approach might be the use of Silicon-On-Insulator (SOI) wafers with (111) oriented handle wafer (the lower wafer in the SOI stack) with a (100) oriented upper device wafer. Etching a tub down to the handle wafer reveals an appropriate (111) oriented substrate for GaN epitaxial growth while the device wafer has the typical CMOS (100) crystal orientation, see Figure 2.

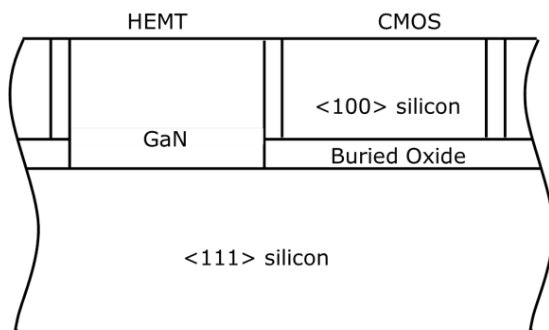

Figure 2: Schematic device cross section of the monolithic GaN in SOI approach [5]

Costs to be taken into account are for the SOI substrate material, the silicon and Buried Oxide (BOX) etch, the GaN MOCVD epitaxy and the CMOS and/or HEMT processing costs whereat not all processing layers allow for re-usage in the other domain.

Monolithic integration in GaN

In the GaN wafer process not only the single power switch can be manufactured, also further transistor(s) or diodes can be integrated to form e.g. a half bridge [9], [10]. With the integration of enhancement and depletion mode transistors NAND, NOR or NOT logic patterns can be built [11]. Just by design, mainly the gate to drain drift region spacing, transistors with different voltage rating can be realized e.g. for integrated gate drivers [12].
Today only n-channel devices are technically and commercially feasible while solutions for p-channel devices are complex and in an early state of research [13]. Additionally, the HV GaN devices will use photolithography nodes in the 180 nm to 1 µm range while for state of the art CMOS sub 180 nm geometry nodes are in use. So either the photolithography is not sufficient for CMOS logic or unnecessary small (and therefore expensive) for the GaN device. A CMOS like complexity won´t be achievable in GaN in foreseeable time.
A severe limitation of the monolithic integration in GaN will be the common silicon substrate. For operating voltages up to 200 V the common substrate is likely not an issue but it will negatively affect operation at higher voltages [14]. Overcoming this issue by the use of SOI substrates, consisting of a lower (100) handle wafer and a top (111) device or epi substrate wafer together with a trench isolation interrupting the (111) silicon substrate adds significantly to performance [15], [16], [17] but also to costs.
Costs to be taken into account are for the silicon (or SOI) substrate material, the MOCVD epitaxy and the processing including additional process step for e.g. trench etching and layers for additional devices.

Direct Wafer Bonding

Another potential integration method to combine GaN and silicon CMOS is wafer bonding [18], [19]. For the Direct Wafer Bonding, DWB, a demanding Chemical Mechanical Polishing, CMP, step is necessary to achieve the required planar surface with sub-1 nm surface topology [20], [21], [22]. The schematic complete flow is shown in Figure 3. Within a first wafer bonding step the GaN wafer is bonded to an oxidized temporary silicon carrier wafer and the (111) silicon substrate of the GaN wafer can be grinded away. After an oxide deposition onto the new surface the “GaN on temporary carrier wafer” is bonded in a second wafer bonding step onto the planarized CMOS wafer. Afterwards, the temporary carrier wafer is removed. Interconnects with sort of Through GaN Vias and a Re-Distribution Layer, RDL, connect the GaN HEMT with the CMOS.

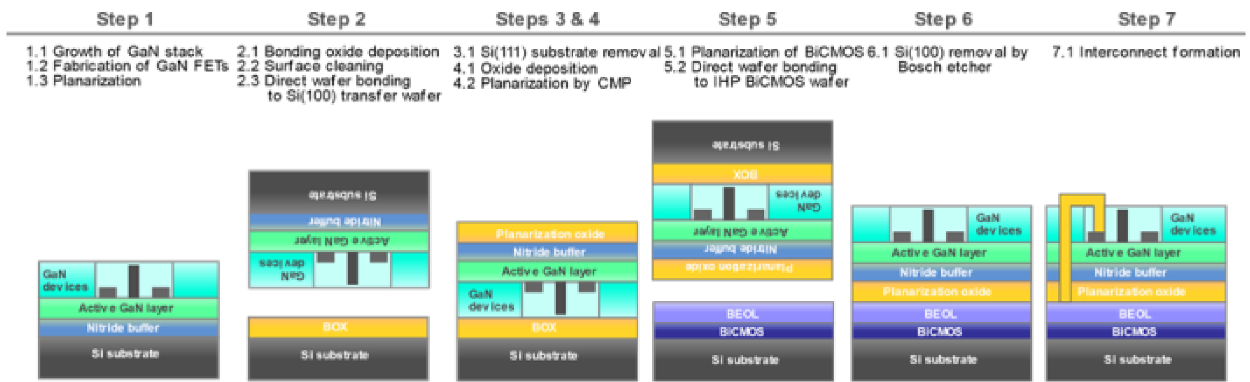

Figure 3: Schematic flow of the heterogeneous integration by Direct Wafer Bonding [20]

Costs to be taken into account are for the substrate materials, for CMOS and GaN MOCVD epitaxy, CMOS and GaN processing, additional processing layers for CMP planarization, two times the direct wafer bonding, grinding and the Through GaN Via and copper plating for the interconnects.

Micro-Transfer-Printing GaN on CMOS

For the micro-Transfer-Printing, µTP, [23] of GaN devices onto silicon CMOS the CMOS product wafer as well as the GaN source wafer are processed separately. Small GaN chiplets (e.g. consisting of a single HEMT or several HEMTs and diodes) or arrays of chiplets are picked from the source wafer with a stamp and printed on the product wafer. Final interconnect is done on wafer level by a thick RDL metal layer. This flow is shown in Figure 4. [24], [25], [26].

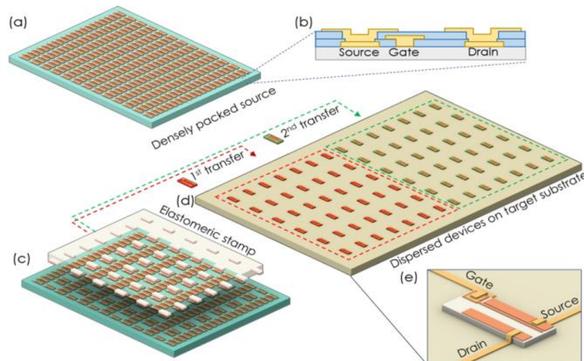

Figure 4: Schematic process flow of the micro-Transfer Printing [21]

Additional processing is needed for release, printing and interconnect. Schematic cross-sections to make the GaN HEMTs print-ready are shown in Figures 5a-c. A first trench etch step around the device removes the Inter-Metal-Dielectric, IMD, material in the Back End of Line, BEOL, layer stack. Silicon nitride is then deposited and patterned to form tethers connecting the HEMTs with an un-etched anchor region thus holding the chiplets in place when in a subsequent step the (111) silicon substrate is removed by an anisotropic wet etch. With help of an elastomeric stamp and velocity controlled adhesion the HEMTs are removed, tethers are broken, and an array of HEMTs is printed on a new substrate wafer and interconnected, Figure 5d.

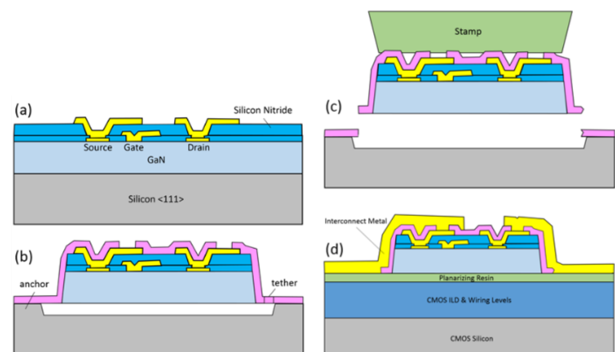

Figure 5. The process flow for heterogeneous integration of GaN HEMTs. (a) The transistors are fabricated on an <111> Si substrate. (b) The devices are isolated, passivated and then undercut. (c) The devices are retrieved with an elastomer stamp. (d) The devices are printed to a Si CMOS wafer and then interconnected using Cu RDL traces. [24]

Around the chiplets additional area is required in both x and y directions for the release trenches, typically these are designed with a width of 10microns. In one direction non under-etched area is used to form the anchor regions (Figure 5b). Figure 6 shows the dropping source wafer utilization rate at small chiplet sizes for anchor widths of 20 and 40microns versus standard 60microns scribe lane width. The wasted non-IC area is much larger for a standard scribe lane solution necessary for blade dicing than for the anchor and tether area of µTP

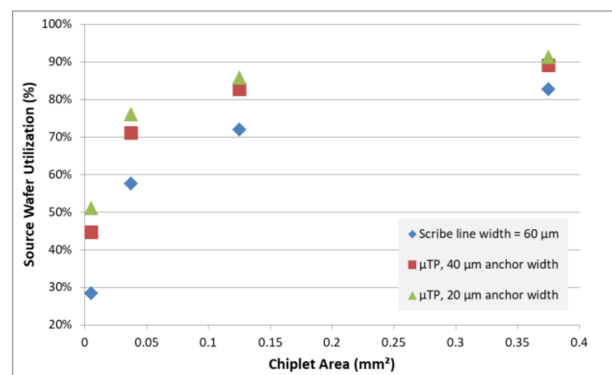

Figure 6: Source Wafer Utilization rate for scribe lane and anchor/tether chip separation

integration especially for small chip sizes.

Costs to be taken into account for the µTP process are the silicon substrates for CMOS and GaN epitaxy, the GaN MOCVD and likely CMOS epitaxy, CMOS and GaN processing, additional processing layers are required for release etch, tether formation, adhesive deposition and patterning. The costs for the micro-transfer printing are to be optimized between stamp size i.e. the number of required print steps to fully populate the product wafer and the source wafer utilization. The copper Re-Distribution Layer, RDL, needs a certain thickness to cross the chiplet height of some microns, this RDL layer potentially might substitute a CMOS via and metal layer – nevertheless full costs have been considered in the following.

A major costs advantage for micro-Transfer-Printing is that one source wafer is typically sufficient to populate several product wafers, thus the GaN source wafer costs are distributed on several product wafers and lower the costs per chip.

µTP CMOS on GaN

Using SOI technologies for the logic IC allows for release etching of CMOS chiplets, fabricated within the upper device wafer of the SOI material, vertically isolated by the BOX and laterally isolated by oxide filled trenches. The release requires a deep etch through the passivation and Inter-Metal-Dielectric, IMD, stacks as well as through the device wafer material. Either the BOX or the silicon handle wafer can then be etched away to release logic CMOS chiplets. Printing of these chiplets can be performed as shown above on top of large GaN HEMTs.

Costs to be taken into account are the silicon and SOI substrates, the GaN MOCVD epitaxy, CMOS and GaN processing, additional processing layers for release etch, adhesive deposition and patterning, the µTP and the RDL.

COST COMPARISON

An overview of the considered costs per integration approach is given in Figure 7. For all technologies 200mm wafer diameters are assumed. In detail the following costs are considered:

Silicon Substrate: Typical costs for 200mm polished substrates, (100) orientation for silicon epitaxy or (111) orientation for GaN MOCVD epitaxy.

SOI Substrate: Typical costs for bonded and etched back SOI wafer with a BOX thickness of about one micron and a device wafer layer several microns thick.

Silicon Epitaxy: Typical costs for about 10 microns thick silicon epitaxial layer.

CMOS process: A typical mask layer count of 20 layers was assumed for the basic CMOS process, additional layers for further metal layers and high voltage n- and p-channel devices are required, in total, processing costs for 30 mask layers were assumed.

GaN MOCVD: Assumed costs for a buffer and barrier GaN epitaxy suitable to manufacture HEMTs with operating voltages above 650V including p-GaN epitaxy for normally-on behaviour.

GaN process: Typical HEMT process with 15 mask layers including p-GaN gate patterning and several metal layers.

DWB: Costs for the planarization process(es), the substrate removal(s), the direct wafer bonding itself as well as the Through Silicon Via, TSV, process for interconnect via formations.

Through Silicon Via, TSV: Assumed processing costs for a sort of front side TSV process including deep di-electric and GaN etch, barrier deposition and copper plating.

µTP: Costs including the printing itself as well as costs for release steps and adhesive patterning

Copper RDL: Costs for a copper plating process, thick enough to cross the chiplet step height of several microns.

Figure 7 also mentions efforts for test and yield. In both heterogeneous integration methods (DWB and µTP) the yield of the CMOS wafer multiplies with the yield of the GaN wafer as well as with the yield of the integration process itself. For the µTP process also the

Bulk CMOS	SOI CMOS	Monolithic integration in SOI	Monolithic Integration in GaN	Direct Wafer Bonding	µTP GaN on CMOS	µTP CMOS on GaN
Yield loss	Yield loss	Yield loss	Yield loss	Yield loss[3]	Yield loss[3]	Yield loss[3]
Test	Test	Test	Test	Test	2x Test	2x Test
					Copper RDL	Copper RDL
					µ-Transfer-Printing	µ-Transfer-Printing
				TSV		
				Wafer Bonding		
			GaN Process	GaN Process	GaN Process	GaN Process
		GaN MOCVD	GaN MOCVD	GaN MOCVD	GaN MOCVD	GaN MOCVD
			Silicon Substrate	Silicon Substrate	Silicon Substrate	Silicon Substrate
CMOS process	CMOS process	CMOS process		CMOS process	CMOS process	CMOS process
Silicon Epitaxy				Silicon Epitaxy	Silicon Epitaxy	
	SOI Substrate	SOI Substrate				SOI Substrate
Silicon Substrate				Silicon Substrate	Silicon Substrate	

Figure 7: Cost components considered for different integration approaches

number of printed chiplets per IC needs to be taken into account since they lower the final yield.

Table 1 shows estimated final yield numbers for µTP of GaN chiplets onto CMOS ICs for typical chiplet and IC areas. The CMOS and GaN yield numbers Y were calculated using the simple Poisson model

$$Y=e^{(-A*D)}$$

defect density D assumed with 0.3 defects/cm² for the CMOS IC and 0.5 defects/cm² for the released GaN chiplet. Even with eight printed chiplets per IC and a low print yield of 90% as a worst case estimation, the calculated final yield numbers are still above 80%.

1 Chiplet / IC							
	GaN area [cm²]	0.0004	0.0008	0.0012	0.0016	0.002	
	GaN yield	99.98%	99.96%	99.94%	99.92%	99.90%	Print
CMOS area [cm²]	CMOS yield	Final yield					Yield
0.04	98.8%	97.8%	97.8%	97.8%	97.7%	97.7%	99%
0.08	97.6%	96.6%	96.6%	96.6%	96.6%	96.6%	99%
0.12	96.5%	95.5%	95.5%	95.4%	95.4%	95.4%	99%
0.16	95.3%	94.3%	94.3%	94.3%	94.3%	94.3%	99%
0.2	94.2%	93.2%	93.2%	93.2%	93.2%	93.1%	99%
0.24	93.1%	92.1%	92.1%	92.1%	92.0%	92.0%	99%
0.28	91.9%	91.0%	91.0%	91.0%	91.0%	90.9%	99%

8 chiplets / IC							
	GaN area [cm²]	0.0004	0.0008	0.0012	0.0016	0.002	
	Source GaN chiplet yield	99.98%	99.96%	99.94%	99.92%	99.90%	Print
CMOS area [cm²]	CMOS yield	Final yield					Yield
0.04	98.8%	88.8%	88.6%	88.5%	88.4%	88.2%	90%
0.08	97.6%	87.7%	87.6%	87.4%	87.3%	87.2%	90%
0.12	96.5%	86.7%	86.5%	86.4%	86.3%	86.1%	90%
0.16	95.3%	85.6%	85.5%	85.4%	85.2%	85.1%	90%
0.2	94.2%	84.6%	84.5%	84.4%	84.2%	84.1%	90%
0.24	93.1%	83.6%	83.5%	83.3%	83.2%	83.1%	90%
0.28	91.9%	82.6%	82.5%	82.4%	82.2%	82.1%	90%

Table 1: Final yield estimation for µTP of GaN chiplets on CMOS ICs for different areas, fixed print yields of 99% (top) and 90% (bottom) and one (top) or eight (bottom) chiplets per IC

The above described cost components with assumed values were then used for cost per wafer estimations of the different integration approaches for varied logic to HV or GaN switch area ratios, see Figure 8. For pure silicon solutions a hypothetical conservative factor of only ten in area was used to compare silicon and GaN high voltage transistors even when Baliga's figure of merit differs by three orders of magnitude between both materials [27], [28]. In this costs per wafer estimation only the µTP integration methods have an area ratio dependence.

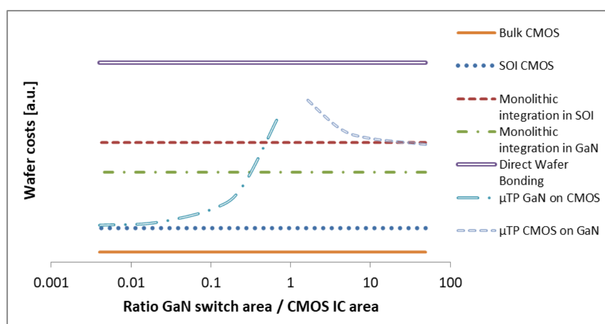

Figure 8: Different integration schemes and their costs per wafer versus area ratio CMOS IC / GaN Switch (equivalent Si HV area for bulk CMOS and SOI CMOS assumed)

Figure 9 gives the results of cost per chip estimations. Base of the estimation is a hypothetical IC with varied logic and HV or GaN switch areas. The standard CMOS solutions, SOI as well as bulk CMOS, reveal costs per chip which are growing significantly with higher switch area. The monolithic integrated solutions, in SOI as well as in GaN, have chip costs independent from the used area ratio. The integration by DWB has a cost minimum at a GaN to CMOS IC ratio of one. The µTP approaches have lightly growing costs per chip with larger GaN switch ratios.

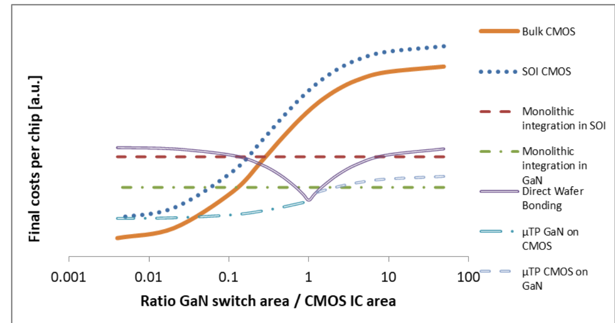

Figure 9: Different integration schemes and their costs per theoretical IC versus area ratio CMOS IC / GaN Switch

COMPARISON µTP – SOI CMOS

The commercial comparison done so far was on a pure cost per wafer base not taking functional requirements i.e. costs per performance and real application requirements, into account. To check the above cost estimation and to add also a functional comparison a cost estimation was done for different dedicated application examples requiring several high voltage switches. The replacement of (large) silicon power switches consuming a lot of IC area by (smaller) printed GaN switches with similar Rds(on) on top of the IC saves area and costs on the CMOS site but adds costs for the GaN device and the printing process.

The comparison, results are shown in Figure 10, was done for the following ICs:

A **30W DC-DC-converter.** This IC is manufactured in a 0.18µm high voltage SOI technology requiring a few 40V and 60V transistors with 0.01Ω and 0.1Ω respectively. The high voltage transistor area is more than 80% of the whole chip area in the silicon variant i.e. HV transistors and logic are placed next to each other, both requiring chip area. The printed GaN transistors on top of the logic lead to a huge chip size reduction with the GaN switches now on top of the logic. The printed switches now need 70% of a much smaller IC.

The cost adder for the release etch, printing and RDL interconnect adds about 50% additional costs. Final cost improvement is about 30%.

A **65W AC-DC-converter.** This IC is manufactured in the same 0.18µm HV SOI technology but it requires several 290V and 375V transistors with 1Ω each. The high voltage transistor area totals to about 35% of the

whole SOI chip area. The printed GaN switches consume only 5% of the IC area in the printed version. Taking into account the additional µTP and GaN costs versus the reduced HV SOI IC area the final cost reduction is almost 20%.

A **three phase Brush-Less DC (BLDC) motor driver**. This IC with on chip charge pump for floating supply generation was designed for a 1µm, 650V trench isolated SOI process. It contains six blocks of several 600V IGBTs and freewheeling diodes with a DC current capability of 4A. The 650V silicon devices to be replaced by printed GaN cover more than 50% of the total IC area in the original layout. Adding the IC area reduction to the additional µTP costs leads to a final costs reduction of more than 10%.

Eight channel controller IC. This IC was already designed for a 0.35µm bulk CMOS process with eight printed 100V, 1.1Ω HEMTs as power switches. The printed GaN needs only about 2% of the IC area. The µTP printing allows for high side configuration even on the bulk CMOS process. Replacing, theoretically, the printed HEMTs by silicon CMOS devices with similar voltage rating and on-resistance would increase the total chip area by only a few percent, cost improvement of the µTP variant is only about 2%. (But, it should be noted, high side capability as for the printed HEMT controller is not possible in this bulk CMOS technology).

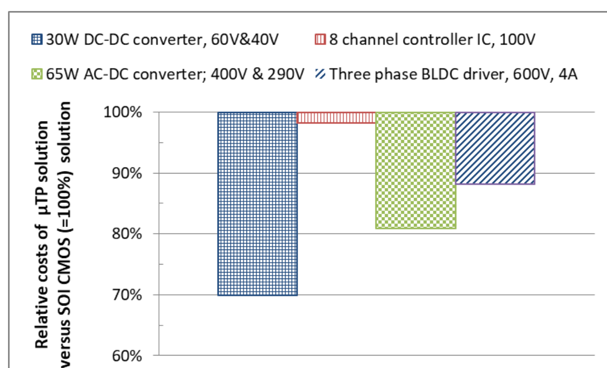

Figure 10: Costs comparison of micro-transfer-printed solution versus SOI CMOS (100%) approach

DISCUSSION

Several conclusions can be already drawn out of the more general costs estimations from Figures 8 and 9 without taking device or IC performance into account. The bulk and SOI silicon CMOS approaches have constant cost levels per wafer. On wafer level the processing effort is not affected by the ratio of high voltage switch to low voltage logic area. On chip level a large GaN switch to CMOS IC ratio as shown in Figure 9 leads to a very high area requirement for the silicon HV transistors (assumed factor of ten between GaN and silicon transistor Rdson) leading to very large IC areas and unfavourable costs when the switch area gets too large.

For both monolithic integration variants, GaN in silicon as well as logic integration in GaN, constant costs are observed per wafer as well as per chip. In both integration approaches costs are defined by substrate and processing costs and the total chip size. The difference in cost levels in Figures 8 and 9 is due to the difference of a factor of two in the assumed processing layers and the GaN MOCVD cost adder versus the SOI substrate. In both monolithic integration variants substrate and processing costs are independent from the ratio of GaN switch to CMOS IC leading to constant chip costs versus ratio in Figures 8 and 9.

Also with the Direct Wafer Bonding, DWB, constant costs can be observed when looking at pure wafer costs, i.e. the costs for two substrates and two times the processing. The costs per wafer appear very high when looking into costs per wafer. This situation changes when looking into costs per chip. Cost advantages for the DWB exist for an area ratio of about one i.e. logic IC and power switch area are about equal, due to the stacking the chip size is only half and material is used very efficiently.

The Micro-Transfer-Printing, µTP, of GaN on CMOS has its commercial sweet spot for low partitioning ratios i.e. the printed GaN switch is much smaller than the CMOS IC. Looking closer into the details it reveals that the main reason for the lower costs is due to the spreading of the quite large GaN MOCVD epitaxy costs of the source wafers over many product wafers. But for very small ratios a sort of saturation can be observed. This cost saturation is due to the required additional area for anchors in one direction and release trenches in both directions so that for very small chiplet edge lengths below 100microns the anchor and release trench area define the chiplet size, therefore the source wafer usage and therefore the costs for the printed chiplets do not further decrease.

Additionally, for small GaN chiplet areas the expected yield figures for the GaN and the release process are pretty high so that reasonable final yield numbers of above 80% can be achieved even when printing several chiplets per IC. The used defect density of 0.3 defect/cm² consider a mature CMOS process plus additional processing steps for the target wafer, the assumed defect density of 0.5 defects/cm² take into account a more complex epitaxial process, typically much less mask layers in the GaN process as well as the additional processing for the release of the chiplets. Based on these estimations potential applications and targets for further developments can be defined.

For µTP of CMOS on GaN a slight cost increase can be seen with higher GaN switch ratios. This is because here the (slightly) cheaper material is printed so that “only” the costs of the cheaper source wafer are distributed among several product wafers. Generally, µTP can lead to commercially attractive solutions when an expensive source wafer can be distributed over many cheaper product wafers.

The pure area related comparison described so far does not consider functional capabilities. Several performance limits like the poor logic functionality of

the monolithic GaN approach without complex digital logic or integrated NVM or the missing high side capability of a bulk CMOS technology might be misleading.
To check the cost per chip model four real IC designs were used to extend the basic costs per wafer and cost per chip comparison to more realistic application driven ICs. The results of these real examples can then be compared to the general cost per chip model, results are given in Figure 11.

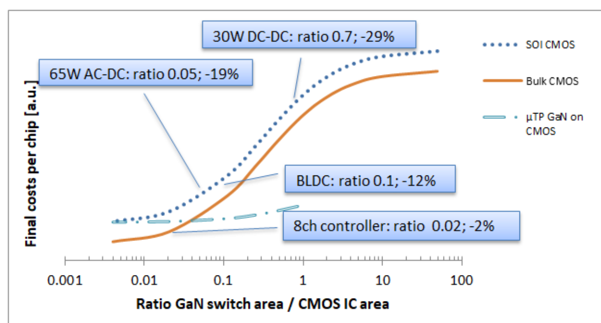

Figure 11: Adding the cost savings from Figure 11 into the expected cost model from Figure 9

The 30W DC-DC-converter is designed in a silicon SOI technology with very low ohmic 40V and 60V transistors. Due to the required low resistance the high voltage transistor area is therefore quite large and requires more than 80% of the whole chip area. Using GaN instead of the silicon HV devices reduces the HV area significantly leading to a printed GaN switch to CMOS IC area ratio of 0.7. The estimated costs savings of 30% fit very well into the general cost per chip model.
The 65W AC-DC-converter requires higher operating voltages (290V and 375V) but much smaller on-resistances and therefore a smaller area for the original silicon based HV transistors which need about 46% of the total IC area. Replacing the silicon HV transistors with printed GaN ones leads to a reduction of required HV GaN area to about 5%. The final cost reduction is almost 20% while the model also predicted cost savings lower than the previous DC-DC-converter.
The three phase Brush-Less DC (BLDC) motor driver originally needs 50% of the IC area for the HV IGBTs. In the printed GaN version the GaN transistors require only 10% of the chip area. With the estimated cost savings of 12% the real costs savings are slightly smaller than what the model would predict for a ratio of 0.1. Likely due to the better on-state resistance of the IGBT the area (and cost) saving effects of the replacement with GaN switches is slightly smaller in the real chip than what the model prediction.
The Eight channel controller IC was already designed for a bulk CMOS process with printed GaN power switches requiring only 2% of the IC area. The cost per chip model predicts a small cost increase of the µTP solution versus the bulk CMOS variant. The cost estimation of the real chip leads to a 2% cost saving. Both deviations from cost parity are rather small so that the model still gives the correct ball park number. Taking into account that all input costs are just estimations with a certain error the predicted behaviour fits very well to the real examples.

CONCLUSION

After having to a certain extend confirmed the rough cost per chip model with four examples one could use now Figure 9 to identify the commercial sweet spots for the considered integration technologies.
HV Bulk and SOI CMOS technologies are commercially competitive for small GaN switch areas. A GaN to IC area ratio of a few percent has to be "translated" into a few tens of tens of percent area ratio in these pure silicon processes which fits to the described partitioning problem.
Monolithic integration in SOI seems to be, from a pure estimated commercial point of view, less attractive. Of course technical performance or ease of handling might justify such a technology.
Especially for a large GaN area ratio **monolithic integration in GaN** has its benefits. So for applications requiring large driver areas with just some logic such a process is commercially attractive.
DWB has its commercial sweet spot for equal GaN and CMOS areas. For unequal chip sizes the unused and wasted area quickly leads to a big increase in costs.
µTP of GaN on CMOS is commercially attractive for small GaN area ratios. On the one hand side, for GaN chiplets getting too small the necessary area for anchors and tethers saturate the printable chiplet size. On the other hand the required underetch of the release process inhibits chiplet sizes getting too big.
µTP of CMOS on GaN is commercially comparable to a monolithic integration in GaN or slightly worse. The much better logic performance of a printed CMOS chiplet versus integrated GaN logic might be a big benefit.

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REFERENCES

[1] A. Elbanhawy: Effects of Parasitic Inductances on Switching Performance, Proc. PCIM Europe 2003, 251–255.

[2] K. Kostov, J. K. Lim, Y. F. Zhang, M. Bakowski: Impact of Package Parasitics on Switching Performance, Materials Science Forum 858, 2016, 1057–1060.

[3] C. Wang et al: Parasitic Effects Analysis of Bonding Wires Bonding Parameter of Intelligent Power Modules for Three-Phase Motor Control Applications; J. Phys.: Conf. Ser. 2020, 1607 012036

[4] M. Pavier et al: High frequency DC:DC power conversion: The influence of package parasitics, APEC 2003 vol.2, 699-704

[5] G. Kittler, R. Lerner: Method for producing silicon semiconductor wafers comprising a layer for integrating III-V semiconductor components; US 8,759,169 B2

[6] T. E. Kazior et al, High Performance Mixed Signal and RF Circuits Enabled by the Direct Monolithic Heterogeneous Integration of GaN HEMTs and Si CMOS on a Silicon Substrate, IEEE Symposium on Compound Semiconductor Integrated Circuit (CSICS), Oct 2011, 1-4

[7] R. Lerner et al, Alternative level shifting devices for 900V gate drivers; Proc. 13th Int. Seminar on Power Semiconductors ISPS'16; 171-176

[8] Maurizio Di Paolo Emilio, III-V semiconductors-based Chips for 5G mobile; https://www.eetimes.com/document.asp?doc_id=1335227

[9] B. Weiss et al., Soft-switching 3 MHz converter based on monolithically integrated half-bridge GaN-chip, IEEE 4th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), 2016, 215-219

[10] G. Tang et al., High-Speed, High Reliability GaN Power Device with Integrated Gate Driver; 30th International Symposium Seminar on Power Semiconductor Devices and ICs, Chicago, 2018, 76-79

[11] M. Zhu and E. Matioli: Monolithic Integration of GaN-Based NMOS Digital Logic Gate Circuits with E-Mode Power GaN MOSHEMTs; 30th International Symposium on Power Semiconductor Devices and ICs, Chicago, 2018, 236-239

[12] Richard Reiner et al., Monolithically-Integrated Power Circuits in High-Voltage GaN-on-Si Heterojunction Technology; 13th International Seminar on Power Semiconductors, Prague, 2016, 29-38

[13] A. Nakajima et al.; Monolithic Integration of GaN-based Normally-off P- and N-channel MOSFETs; 13th International Seminar on Power Semiconductors, Prague, 2016, 127-136

[14] B. Weiss et al: Substrate Biasing Effects in a High-Voltage, IEEE 5th Workshop on Wide Bandgap Power Devices and Applications (WiPDA); 2017, 265 - 272

[15] K. Geen, M. Van Hove and S. Decoutere.; The Monolithic Integration Of GaN; Compound Semiconductor Vol. 23, Issue 6, August / September 2017, 40-43

[16] X. Li et al.: 200 V Enhancement-Mode p-GaN HEMTs Fabricated on 200 mm GaN-on-SOI With Trench Isolation for Monolithic Integration," in IEEE Electron Device Letters, vol. 38, no. 7, July 2017, 918-921

[17] X. Li: Reliability and Integration of GaN Power Devices and Circuits on GaN-On-SOI, PhD thesis KU Leuven, November 2020

[18] K. H. Lee et al.: Monolithic Integration of Si-CMOS and III-V-on-Si through Direct Wafer Bonding Process," IEEE Journal of the Electron Devices Society, vol. 6, 2018, 571-578

[19] D. Caimi et al: "Heterogeneous Integration of III–V Materials by Direct Wafer Bonding for High-Performance Electronics and Optoelectronics," in IEEE Transactions on Electron Devices, vol. 68, no. 7, July 2021, 3149-3156,

[20] C. Zota: communication during GaNonCMOS project

[21] https://ganoncmos.eu/ganoncmos-results-systems/

[22] C. Zota: Direct Wafer Bonding for 3D Integration of Si CMOS and GaN, in https://ganoncmos.eu/wp-content/uploads/2021/04/GaNonCMOS_Webinar_2020-06-18_final.pdf , 37-52

[23] M. A. Meitl et al: Transfer printing by kinetic control of adhesion to an elastomeric stamp." Nature materials, 5.1, 2006, 33-38.

[24] R. Lerner et al: Heterogeneous Integration of Microscale Gallium Nitride Transistors by Micro-Transfer-Printing," 2016 IEEE 66th Electronic Components and Technology Conference (ECTC), Las Vegas, NV, USA, 2016, 1186-1189

[25] R. Lerner et al: Integration of GaN-HEMTs onto Silicon CMOS by micro Transfer Printing, 28th International Symposium on Power Semiconductor Devices and ICs (ISPSD), Prague, 2016, 451-454.

[26] R. Lerner et al: Flexible and Scalable Heterogeneous Integration of GaN-HEMTs on Si-CMOS by Micro-Transfer-Printing." Physica Status Solidi A 215, No 8, 2018,

[27] B.J. Baliga: Semiconductors for high-voltage, vertical channel field-effect transistors. J. Appl. Phys. 53, Vol 53, Issue 3, 1982,

[28] B. J. Baliga: Power semiconductor device figure of merit for high-frequency applications, IEEE Electron Dev. Lett. Vol 10, Issue 10, 1989, 455-457

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