

A Simulation study of 6.5kV Gate Controlled Diode

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Abstract

Gate Controlled Diode (GCD) with micro-pattern trench structure, allows charge carrier modulation at the anode region by gate control. This is utilized to operate the diode at low saturation mode and desaturate the diode before IGBT turn-on, to achieve a better trade-off. The paper demonstrates the concept of a silicon bi-polar power diode with micro-pattern trench gate, for 6.5 kV applications. Thereby, a detailed study of switching behaviour and the switching pattern were conducted, so as to reduce the overall switching loss and improve the efficiency. The efficiency also depends on the robustness of the diode, several issues concerning the reverse recovery robustness of the Gate controlled diode were investigated.

Keywords: Gate Controlled Diode, micro-pattern trench, 'tdsat', desaturation

Introduction

The advancement in the processing technology has led to the development of micro-pattern trench (MPT) cell structures. The capability to achieve low on-state voltage and a better dynamic performance of MPT IGBT's [1, 2], has increased the speed and efficiency of high voltage power converters. To comprehend such fast-switching applications and increase the power quality of the overall system, a robust high performance controllable diode is necessary.

Several controllable silicon power diodes have been published, such as MOS controlled diode (MCD) [3], diode with controlled emitter efficiency [4], Anode controlled diode (ACD) [5]. However, they require pre-triggering to avoid short circuit or have turn-off robustness issues due to possible electron injection during open nchannel operation. In this paper a silicon high voltage diode based on the micro-pattern trench gate cell structure, is proposed.

The aim is to realize a diode for 6.5 kV HVDC and traction applications, with good controllability, and which has a low conduction loss and low switching loss. A numerical device level simulation of Gate controlled diode (GCD) is demonstrated in this paper, using Sentaurus TCAD.

Gate Controlled Diode Structure and Principle

The concept of the Gate controlled diode with MPT cell structures, is to use the high carrier confinement of the MPT cell design to achieve a low on-state voltage drop [1]. The vertical charge carrier profile realized by MPT cell design, enables highly controlled stored charge removal during diode turnoff [2], leading to low switching loss and better trade-off behaviour.

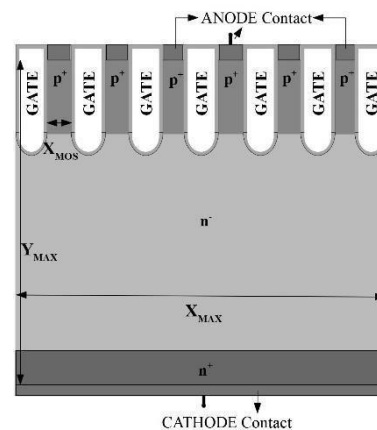


Fig. 1. Schematic cross-section of Gate controlled diode (GCD), with micro-pattern trench gate structures.

A schematic cross section of the Gate controlled diode (GCD) is shown in Fig. 1. The diode is based on PiN configuration with MPT cell structure on the anode side. The MPT cell structure and gate for the

diode were realized based on literature [2]. A $6\ \mu\text{m}$ (X_{MAX}) wide MPT structure was designed with a mesa width of $0.4\ \mu\text{m}$ (X_{MOS}) and a carefully selected mesa width to cell pitch ratio [6]. A $2.5\ \mu\text{m}$ thick p^+ anode region with a doping concentration of $5 \times 10^{16}\ \text{cm}^{-3}$ was realised into the sub- μm mesas between the trench gate. A very thin highly doped p^+ layer was formed near the anode contact to make the region low ohmic. A $0.5\ \mu\text{m}$ n^+ cathode layer of doping density $5 \times 10^{17}\ \text{cm}^{-3}$ was diffused into the n^- intrinsic base region. The thickness (Y_{MAX}) of the model and doping concentration of the base region was designed to handle a reverse blocking voltage of $6.5\ \text{kV}$.

Depending on the operation of GCD, a high injection of charge carriers can be achieved to lower conduction loss or have a controlled plasma density reduction, to lower the switching loss. This is possible by charge carrier modulation at the anode region, achieved from varying gate potential. When negative potential is applied, strong injection of holes leads to high plasma density. When a positive voltage is applied, an electron channel is developed around the oxide region which reduces the hole density from the anode side.

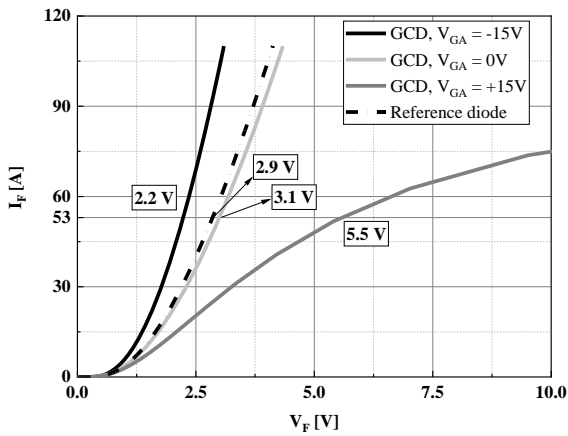


Fig. 2. Static I-V characteristics of GCD compared with reference diode. $I_{\text{nom}} = 53\ \text{A}$, $T = 150\ ^\circ\text{C}$.

Static I-V characteristics of GCD is shown in Fig.2, where the diode is simulated for a nominal current (I_{nom}) of $53\ \text{A}$ at $150\ ^\circ\text{C}$. The simulation model is designed to have active gate control over all the MPT gate structures and they are driven with respect to anode potential (V_{GA}). Compared to the I-V characteristics of the reference diode in Fig. 2, GCD operating with $V_{\text{GA}} = -15\ \text{V}$ has a low on-state voltage drop ($2.2\ \text{V}$ at nominal current) due to high plasma density on the anode side, achieved by strong hole injection. The strong hole density during $V_{\text{GA}} = -15\ \text{V}$ is reduced, when the biasing to the gate is removed and the diode behaves as a simple PiN

diode with reduced charge carriers at the anode side. This behaviour of plasma distribution when $V_{\text{GA}} = 0\ \text{V}$ is shown in Fig.3, along with plasma density curves from $V_{\text{GA}} = -15\ \text{V}$, $+15\ \text{V}$, $+5\ \text{V}$, $+30\ \text{V}$. Furthermore, positive gate voltages reduce the plasma density on the anode side further down. This reduced plasma at $V_{\text{GA}} = +15\ \text{V}$, results in a higher voltage drop across the diode ($5.6\ \text{V}$ at nominal current).

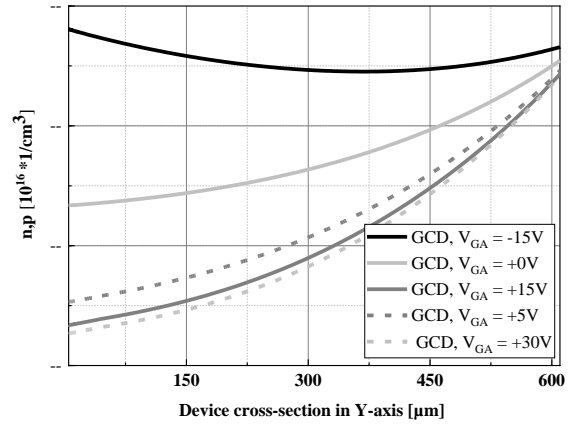


Fig. 3. Plasma density across the cross-section of GCD for corresponding Gate potentials from Fig. 2. under static condition. $I_{\text{nom}} = 53\ \text{A}$, $T = 150\ ^\circ\text{C}$.

Switching control and Trade-off

It is observed from Fig. 2 and 3 that the operating point of the device changes with gate bias. The effect of changing plasma density due to change in applied gate potential can be used to desaturate the plasma density during GCD's turn-off. This reduces reverse recovery charge and switching losses, improving the overall efficiency of the system.

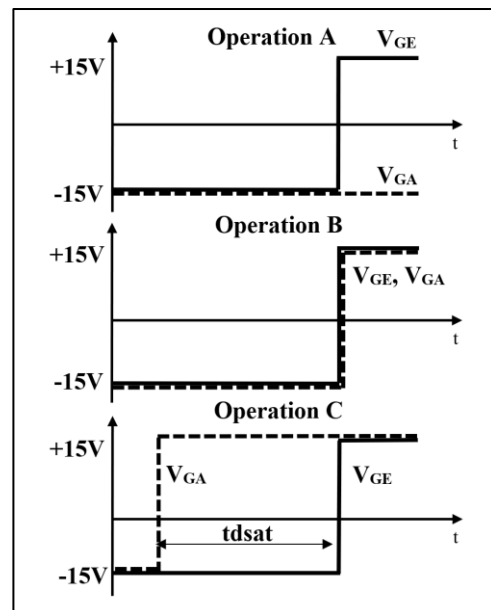


Fig. 4. GCD and IGBT, gate drive operations.

In order to understand the control that can be achieved by the gate, three driving conditions of V_{GA} are considered, as in Fig. 4. Operation A describes a constant V_{GA} of -15V on the GCD. Operation B, simultaneous switching of both the diode and the IGBT from -15V to +15V. Operation C shows switching of GCD ($V_{GA} = -15V$ to +15V) before the IGBT, with a time difference ‘ t_{dsat} ’. The simulations were performed for a nominal current of 53 A, a DC-link voltage of 3.6 kV and at a temperature of 150 °C. A 6.5 kV MPT-IGBT, similar to a model scaled from [2], with half the current density as of the diode is considered. For the traction application standards, the simulations were performed with a boundary condition of reverse recovery peak power (P_{RR}) 150 kW and the circuit inductance (L_S) of 1.6 μ H in accordance with $L_{stray} * I_{nom}$.

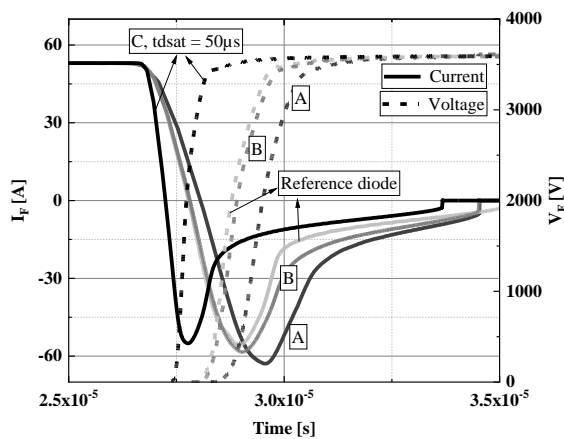


Fig. 5. Transient I-V characteristics of GCD during switching operations described by A, B, C. $V_{DC} = 3.6$ kV, $I_{nom} = 53$ A, $T = 150$ °C, $L_S = 1.6\mu$ H, $P_{RR} = 150$ kW.

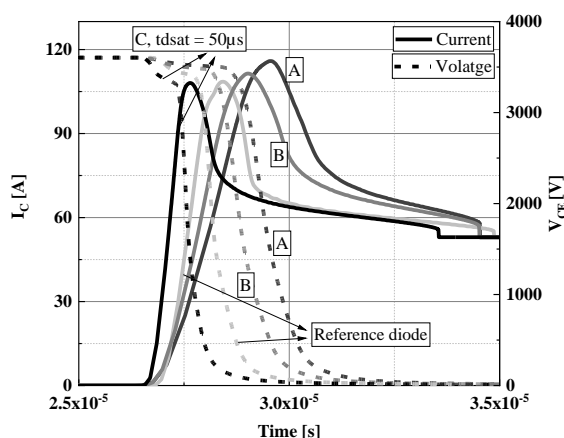


Fig. 6. Transient I-V characteristics of MPT-IGBT during switching operations described by A, B, C. $V_{DC} = 3.6$ kV, $I_{nom} = 53$ A, $T = 150$ °C, $L_S = 1.6\mu$ H, $P_{RR} = 150$ kW.

Fig. 5 and 6 show the transient I-V behaviour of GCD and IGBT switching during the above described operations A, B and C with ‘ t_{dsat} ’ = 50 μ s.

Operation A, with a constant $V_{GA} = -15V$ has the slowest dI_F/dt and highest switching loss, because of high stored charge in the diode. Only a small amount of charge reduction takes place by simultaneous switching of GCD and IGBT during Operation B. GCD has slightly high reverse recovery charge than the reference diode, because of high plasma density of GCD at $V_{GA} = -15V$. Due to fixed peak P_{RR} , the additional charge carriers left in the diode slows the dI/dt of IGBT during Operation B, when compared with the reference diode.

‘ t_{dsat} ’, the switching time between upper side IGBT and lower side GCD, has a great influence on switching loss. In this paper, different diode ‘ t_{dsat} ’ times 5 μ s, 20 μ s, 50 μ s and 100 μ s are investigated. From Operation B, it is noted that simultaneous switching is not advantageous so the IGBT is switched after GCD as in Operation C. Since changing V_{GA} from -15 V to +15 V reduces device plasma, GCD utilises the time ‘ t_{dsat} ’ to desaturate plasma [3, 7, 8]. Rate of desaturation varies in accordance with stored charge.

Fig. 7 shows the removal of charge carriers from GCD during Operation C, with a ‘ t_{dsat} ’ of 50 μ s. As observed, the total switching time to completely remove the charge carriers of the GCD is 60 μ s. For the first 50 μ s, the GCD desaturates and is driven into reduced plasma state by $V_{GA} = +15V$ while the IGBT is still in the blocking mode. The IGBT is turned on at 50 μ s and the GCD starts taking up the voltage. Due to the reduced plasma after 50 μ s the reverse recovery charge that needs to be removed becomes low. For a fixed peak P_{RR} and $L_{stray} * I_{nom}$ of the diode, steep dI_F/dt is observed with I_{RRM} remaining similar to I_{RRM} of the reference diode.

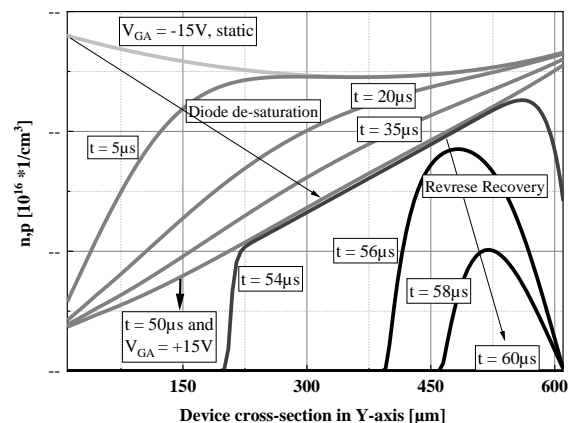


Fig. 7. Plasma density distribution across the cross-section of GCD, during the transient Operation C, with ‘ t_{dsat} ’ of 50 μ s. $V_{DC} = 3.6$ kV, $I_{nom} = 53$ A, $T = 150$ °C, $L_S = 1.6\mu$ H, $P_{RR} = 150$ kW.

Fig. 8 compares the influence of different ‘tdsat’ (0 to 100 μ s) to turn-on switching loss, distinguishing the GCD’s reverse recovery loss (E_{RR}), IGBT’s turn-on loss (E_{ON}) and the desaturation loss occurred during ‘tdsat’ (E_{dsat}). In addition, total switching loss of the reference diode is also shown at the specified nominal current density. It is observed for a longer ‘tdsat’, the reverse recovery loss and the IGBT turn-on loss reduces, reducing the total turn-on loss. Although a small amount of desaturation loss exists with 50 μ s and 100 μ s, when compared to the total reduction it is a small number.

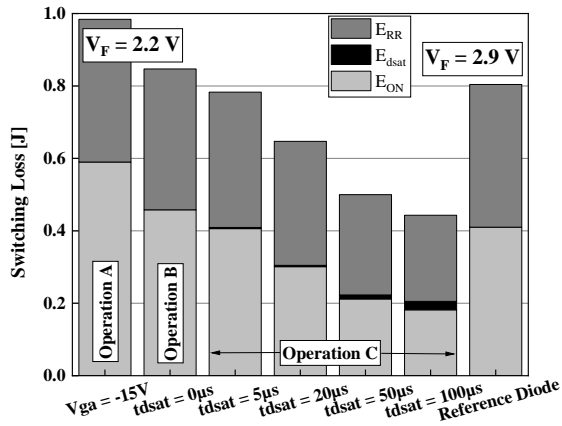


Fig. 8. Overall switching Energy loss comparison, distinguishing GCD’s E_{RR} , E_{dsat} and E_{ON} for Operations A, B and C for ‘tdsat’= 5 μ s, 20 μ s, 50 μ s, 100 μ s. V_{DC} = 3.6 kV, I_{nom} = 53A, T = 150 $^{\circ}$ C, L_S = 1.6 μ H, P_{RR} = 150 kW.

Table 1 shows the comparison of loss reduction achieved by influence of ‘tdsat’ in Operation B and C, when compared with Operation A i.e., GCD at a constant V_{GA} = -15V during switching. In case of ‘tdsat’ 50 μ s and 100 μ s respectively, a 50% and 55% of overall turn-on loss reduction is observed for a given peak reverse recovery power.

tdsat [μ s]	$R_{GON-IGBT}$ [Ω]	% Reduction in E_{RR}	% Reduction in E_{ON}	% Reduction in E_{TOTAL}
0	25	1.3	22.4	13.9
5	23	5.1	31.2	20.4
20	17	13.1	49.0	34.2
50	12	29.7	64.1	49.2
100	9	39.6	69.2	55.0

Table 1. Percentage energy loss reduction of Operations B and C when compared with Operation A.

A 50 % loss reduction obtained from longer ‘tdsat’ promises a significant improvement in the efficiency of the converter. For traction applications with 400 Hz switching frequency or HVDC application with 150 Hz switching frequency, the

100 μ s ‘tdsat’ lies well within the limit. As long as the ‘tdsat’ time is no longer than the applied pulse width, the PWM rectifiers and inverters should be capable of driving such a switching sequence.

The influence of ‘tdsat’ and changing diode current are investigated in order to understand the GCD’s behaviour in different operating conditions. Fig. 9 gives a total turn-on energy loss comparison of GCD during Operation C for varying ‘tdsat’, I_F , temperature. It is to be noted that, for a low current range, diode reverse recovery loss dominates the total turn-on loss from Fig. 9 a. Fig. 9 b, for I_F of 2 I_{nom} the energy loss distribution indicates that GCD with ‘tdsat’ of 50 μ s gives the best loss reduction. Even though the reverse recovery loss of GCD reduces with 100 μ s, the desaturation loss increases significantly. This is due to the high voltage drop (55 V) across the GCD at V_{GA} = +15V with 2 I_{nom} . The diode operates at a high saturation phase because of very high minority carriers at cathode side for such high current densities. Fig. 9 c, gives the variation in switching energy loss at 25 $^{\circ}$ C and 150 $^{\circ}$ C, it is observed for decreasing temperature the diode reverse loss decreases and IGBT loss increases.

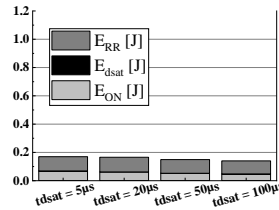


Fig. 9 a. I_F = 0.1 I_{nom} , T = 150 $^{\circ}$ C

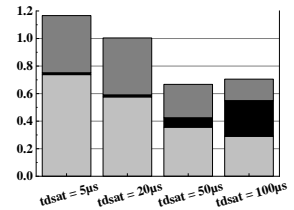


Fig. 9 b. I_F = 2 I_{nom} , T = 150 $^{\circ}$ C

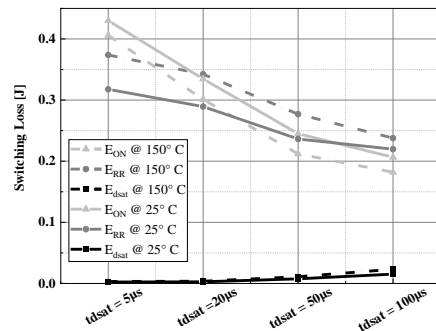


Fig. 9 c. I_F = 1 I_{nom} , T = 25 $^{\circ}$ C and 150 $^{\circ}$ C

Fig. 9. Overall switching Energy loss comparison, distinguishing GCD’s E_{RR} , E_{dsat} and E_{ON} for changing, ‘tdsat’= 5 μ s, 20 μ s, 50 μ s, 100 μ s, I_F = 5A, 53A, 106A and T = 25 $^{\circ}$ C and 150 $^{\circ}$ C. V_{DC} = 3.6 kV, L_S = 1.6 μ H.

Fig. 10 and 11 compares dI_F/dt of GCD with reverse recovery charge, Q_{RR} and turn-on loss, E_{ON} of the IGBT for varying ‘tdsat’ and currents. For different ‘tdsat’, $R_{GON-IGBT}$ are varied as in the Table 1. With

increasing 'tdsat' it is observed the dI_F/dt gets steeper and the turn-on loss of IGBT and reverse recovery GCD gets smaller. The effect of I_{nom} and $2I_{nom}$ on Q_{RR} appears to be minimal, whereas the IGBT turn-on loss increase is significant with changing I_F .

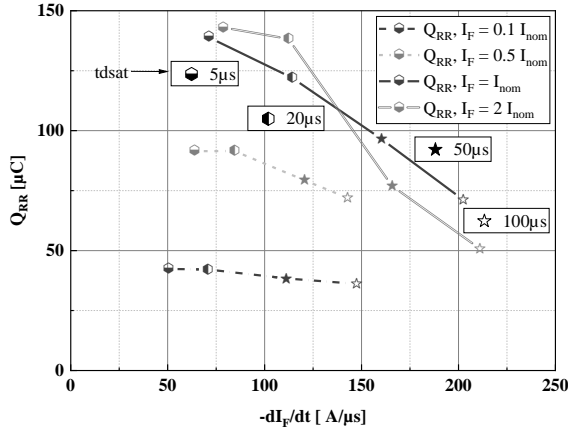


Fig. 10. Comparison of change in slope of diode current - dI_F/dt to the reverse recovery charge Q_{RR} of GCD for changing, 'tdsat' = $5\mu s$, $20\mu s$, $50\mu s$, $100\mu s$, $I_F = 5A$, $26A$, $53A$, $106A$, $V_{DC} = 3.6 kV$, $T = 150^\circ C$, $L_S = 1.6\mu H$.

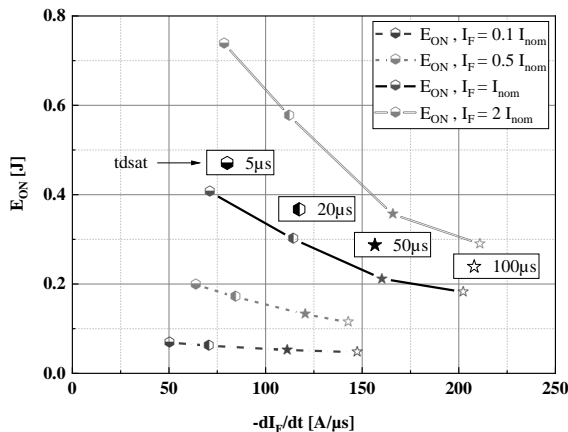


Fig. 11. Comparison of change in slope of diode current - dI_F/dt to the MPT-IGBT turn-on loss E_{ON} of GCD, for changing 'tdsat' = $5\mu s$, $20\mu s$, $50\mu s$, $100\mu s$ and changing diode current, $I_F = 5A$, $26A$, $53A$, $106A$, $V_{DC} = 3.6 kV$, $T = 150^\circ C$, $L_S = 1.6\mu H$.

Reverse Recovery Robustness

The Blocking Voltage. The GCD was designed to block a reverse voltage of 6.5 kV. Fig. 12 shows the simulation of static blocking condition of the diode at $V_{GA} = -15V$ and $V_{GA} = +15V$ at $150^\circ C$. In both the cases, the device shows a blocking capability up to 6.5 kV. At negative gate voltage, the leakage current appears to be low; during positive gate potential, the device shows marginally higher leakage current. To achieve a low on-state voltage, a higher n^+ cathode doping concentration was used

for the GCD. To reduce the leakage current, the cathode efficiency may be optimised.

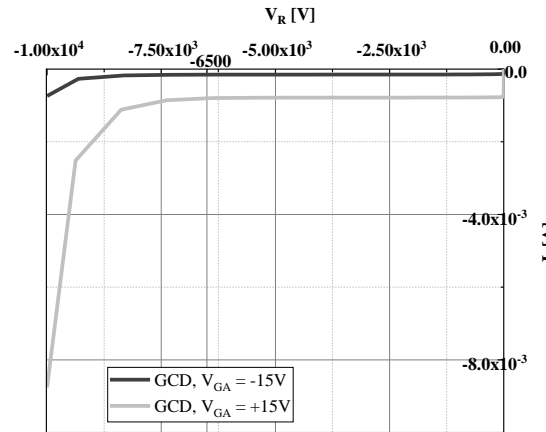


Fig. 12. Static blocking simulation, 6.5kV GCD, $T = 150^\circ C$.

Investigation of possible electron injection. The punch through of the device must be investigated at high reverse current densities to study the possible electron injection from the anode contact, when the electron channel is active at $V_{GA} = +15V$. The influence of electric field upon reaching the contact may induce an electron current from anode into the substrate which is an undesired effect. To simulate such an induced scenario, a work-around structure was designed as shown in Fig. 13. The main design modifications were highly doped p^+ layer fused at the cathode alongside the n^+ cathode. Two separate contact terminals provided for the p^+ and n^+ layer to bias the p-n junction. Anode ohmic contact was changed to Schottky contact. A high reverse blocking voltage of 50 kV was applied to the work-around structure under static condition, with a positive voltage to bias the p-n junction and the avalanche parameter was de-activated

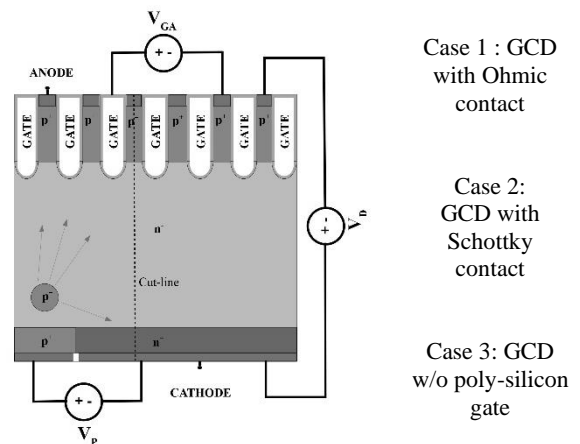


Fig. 13. Work-around structure of GCD to simulate possible electron injection. $V_{GA} = +15V$, $V_D = 50 kV$, $V_P = 1.7V$, de-activated avalanche parameter.

Three different cases of work around GCD structures were simulated. Case 1, GCD with normal anode ohmic contact. Case 2, GCD with Schottky anode contact. Case 3, the same structure with Schottky anode contact and micro-pattern trenches filled only with oxide to de-activate gate control. It is observed from Fig. 14, that the electric field doesn't reach the anode contact in case 1 and 2, with active MPT gate structures. Whereas in case 3, electric field reaches the anode contact and punch through is observed at a voltage of 1 kV as shown in Fig. 15, with increase in electron current (I_{eR}) and hole current (I_{pR}).

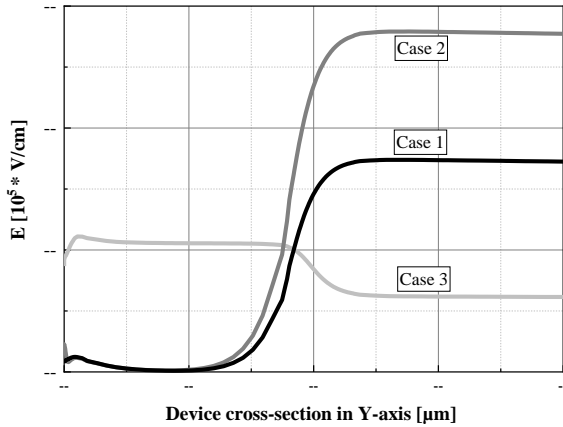


Fig. 14. Electric field distribution across the cross-section of the device (partial cross-section of the structure is shown). $V_{GA} = +15V$, $V_D = 50 kV$, $V_P = 1.7V$, de-activated avalanche parameter.

Fig. 15 shows the simulation of static I-V behaviour of the work around structures in case 1, 2, 3. As seen, a high hole current (I_{pR}) is flowing to the anode contact due to additional injection from p^+ layer at high reverse blocking voltage of 50 kV and a V_{GA} of +15V, without the avalanche generation. During cases 1 and 2, punch through of device is not observed due to field shielding effect provided by micro-pattern trench structure and device shows negligible electron current. This shows no electron injection from the anode contact and demonstrates a robust anode side of GCD structure.

Investigation of Cathode side Dynamic Avalanche and Softness. Typically, soft reverse recovery behaviour is observed from Fig. 5, at nominal current 53 A and DC link voltage of 3.6 kV, during Operation C. When GCD (at $V_{GA} = -15V$) is at high plasma density state, a short-circuit type IV leads to high carrier concentration on both sides of the diode. Specifically, the minority charge carriers at the back side of the diode leads to a high electric field and a cathode side avalanche. This may lead to double side fed current filaments on both sides of

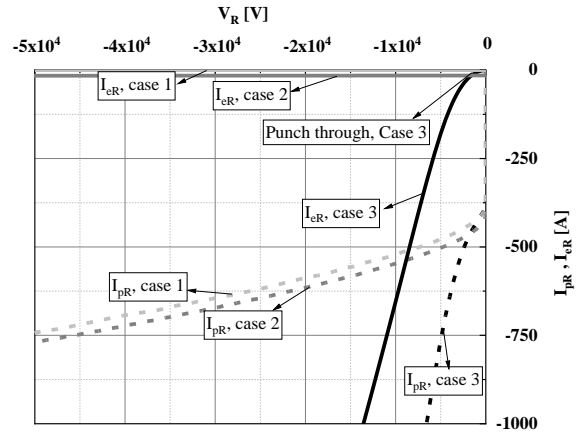


Fig. 15. Static reverse I-V simulation of GCD at high blocking voltage from Fig. 12. $V_D = 50 kV$, $V_P = 1.7V$, de-activated avalanche parameter.

the GCD. Furthermore, at 0.1 I_{nom} and lower temperature, the diode shows a snappy reverse recovery behaviour.

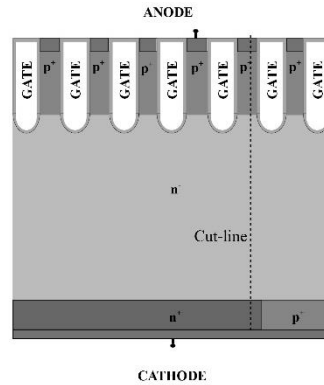


Fig. 16. GCD w/ p^+ shorts at cathode.

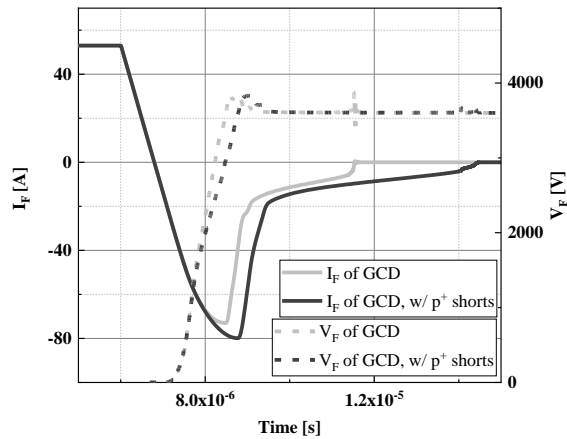


Fig. 17. Transient I-V characteristics of GCD and GCD w/ p^+ short, during short-circuit type IV. $L_{sc} = 52 \mu H$, $L_s = 1.6 \mu H$, $V_{DC} = 3.6 kV$, $I_{nom} = 53A$, $T = 150 ^\circ C$.

To avoid snappy recovery and cathode side dynamic avalanche, an addition of high doped p^+ short at cathode terminal is considered, similar to Field Charge Extraction (FCE) diode [9]. Fig. 16, depicts

a GCD with p^+ shorts at the cathode side. The n^+ cathode and p^+ short is electrically connected to each other. Simulations were based on wide (large X_{MAX}) model, to obtain inhomogeneous plasma distribution across the width of the diode. The short-circuit type IV simulations were performed at 3.6 kV DC-link voltage and I_F of 53A at 150 °C. The short-circuit inductance (L_{SC}) of 52 μ H, was chosen to have a similar dI_F/dt as during a normal switching.

The p^+ short provides an additional injection of holes, which delays the removal of minority carriers in the region. This slows down the depletion and avoiding a huge space charge region being formed, reducing the electric field and hence the dynamic avalanche on the cathode side. Additional hole current from p^+ short adds to the reverse recovery current and softens the tail current which can be observed from Fig. 17.

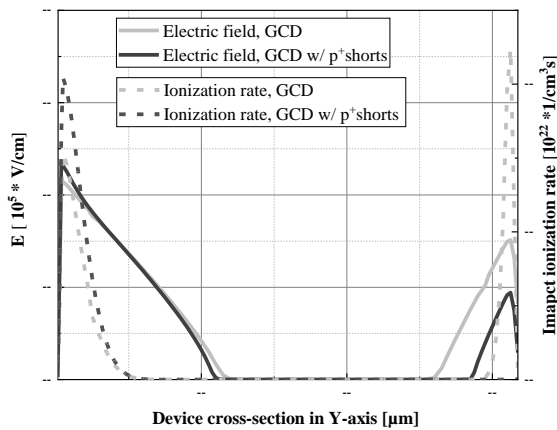


Fig. 18. Electric field distribution and Impact ionization rate distributed across the cross-section of the GCD and GCD w/ p^+ short. $L_{SC} = 52 \mu H$, $L_s = 1.6 \mu H$, $V_{DC} = 3.6 kV$, $I_{nom} = 53A$, $T = 150 \text{ }^\circ C$.

Fig. 18. shows the distribution of Electric field and Impact ionization rate, during short-circuit type IV. High electric field is observed on both sides, in the case of GCD. The GCD with p^+ shorts show decreased electric field on cathode side. The impact ionization shown in the figure depicts, no dynamic avalanche on the cathode side of GCD with p^+ short. The disadvantage of this modified structure would be additional reverse recovery charge which increases the losses, and also increased front side dynamic avalanche.

Conclusion

A Gate controllable diode concept is proposed based on the micro-pattern trench gate design. The simulation results of GCD MPT diode with an

efficient control allows two operating points of the GCD, a low on-state voltage mode ($V_{GA} = -15V$) for diode conduction and a moderately high saturation mode ($V_{GA} = +15V$), used to de-saturate the diode during switching. The GCD showed a significant improvement over the reference diode of same class, with 25% reduction in conduction loss and 40% to 60% reduction in switching loss after an effective desaturation achieved by gate control.

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