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CONTENTS

VISUAL PRESENTATIONS

INVITED LECTURES

Energy Harvesting Using Thermoelectric Microgenerators: Realistic Perspective or Utopian Idea? A Critical Analysis

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Abstract

Microstructured cell-arrayed thermoelectric power generators, which are able to convert (waste) heat into a few milliwatts or even watts of electrical energy, seem to be particularly attractive for the autonomous power supply of microelectronic circuitry and electronic or micromechatronic appliances without the use of batteries. However, the conversion efficiencies achieved so far are very small. A critical analysis shows that there is still a certain potential for improvements toward the theoretical limits, but that some expectations seem to be rather unrealistic and questionable in view of the physical and technological limitations.

INTRODUCTION

The need for regenerative decentralized small electric power sources comes along with the progress in microsystems technology in its various widespread application fields as, for example, wireless telecommunication and wearable appliances. Miniaturized thermoelectric power generators, which are able to convert waste heat into a few milliwatts or even watts of electrical energy, seem to be particularly attractive for the autonomous power supply of microelectronic or micromechatronic gadgets without the use of batteries. Microstructured (even CMOS-integrated) micro-thermoelectric generators (μ-TEGs) have been successfully demonstrated and are commercially available. However, the conversion efficiencies achieved so far are very small (less or much less than a few percent). But fortunately this is not decisive for many practical applications, where a heat source delivers the input heat for free (as waste heat) from an available heat reservoir at high temperature. Instead, other figures of merit have to be considered to assess the performance of μ-TEGs properly as discussed in the following.

Basic theoretical considerations

Thermodynamic efficiency

A thermoelectric generator (TEG) is a device through which heat is flowing from a heat source at high temperature T_{in} to a heat sink at low(er) temperature T_{out} (Fig.1). In an idealized view, it is assumed that the electric power P delivered by the TEG is the difference between the inflow and the outflow of heat, dQ_{in}/dt and dQ_{out}/dt . The energy conversion efficiency is defined as

$$\eta = \frac{P}{\left(\frac{dQ_{in}}{dt}\right)} \qquad (1)$$

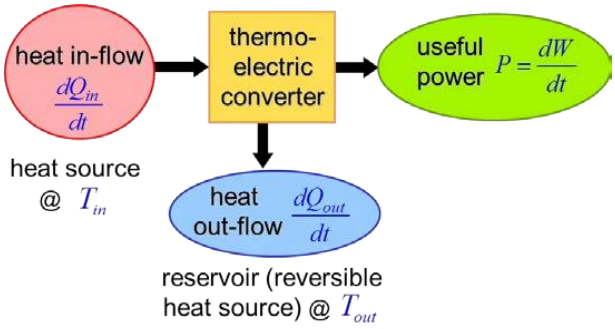

Fig. 1: Energy flow in an ideal thermoelectric generator.

By the second fundamental law of thermodynamics, η is limited by the Carnot efficiency η_C; this means

$$\eta \le \eta_c = T_{out}\left(\frac{1}{T_{out}} - \frac{1}{T_{in}}\right) = 100\% - T_{out}/T_{in} \qquad (2)$$

Typical values of the maximum attainable efficiency at room temperature $T_{out} = 300K$ for different temperature drops $\Delta T = T_{in} - T_{out}$ are

ΔT	$5K$	$10K$	$20K$	$100K$
η_C	1.6%	3.2 %	9.1%	25%

Unfortunately, due to effects inherent in thermoelectricity and design limitations, the converter efficiency attained in real µ-TEGs is drastically smaller (even by orders of magnitude) than η_C. On the other hand, even if the converter efficiency is very small, a µ-TEG may harvest a specified amount of electric output power, if the device area exposed to the heat flow is sufficiently large to collect the required inflow of waste heat (Fig. 2). As the latter comes for free, the crucial quantity determining the performance is the output power per active device area (see section 2.4), while the converter efficiency becomes quite questionable as measure of the device performance.

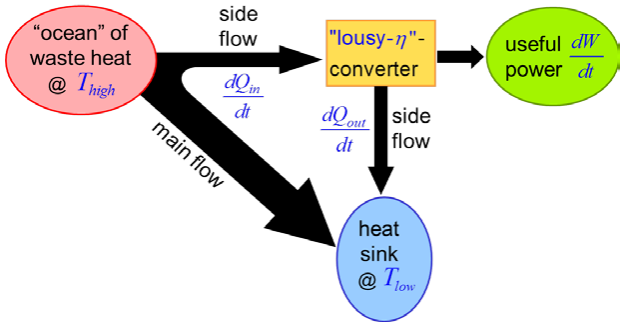

Fig. 2: Energy flow in a real "waste-heat-to-power" converter. The side flow of waste heat is proportional to the active area of the converter.

Figure of merit ZT

A common approach to assessing the performance of TEGs is based on the transport equations governing the flows of heat and electric current in a thermoelectric material. It is assumed that the maximum deliverable electric power flux is determined by the electronic contribution $J_{Q,el}$ to the total heat flux $J_{Q,tot}$ according to the relation

$$\vec{J}_{Q,el} \approx (L + S^2)\frac{\sigma T}{\kappa}\vec{J}_{Q,tot} \qquad (3)$$

where L is the Lorenz number, S the (absolute) thermopower, σ the electric conductivity, and κ the thermal conductivity. This relation suggests that the dimensionless quantity

$$ZT := \frac{S^2\sigma}{\kappa}T \qquad (4)$$

κ may serve as a proper "figure of merit" for the thermoelectric performance. Measured values of ZT vary over a wide range from $ZT \approx 10^{-3}$ for homogeneous bulk semiconductors to $ZT \approx 0.5\ldots1$ for commonly used high-efficiency thermoelectric materials like alloys based on bismuth in combinations with tellurium, antimony or selenium [2]. Current research focussing on nanostructured materials (superlattice, quantum dots etc.) has shown that ZT values up to 4 are feasible. However, the relevance of high ZT must be revisited in the light of the next section.

Thermoelectric generator efficiency

A more detailed theory including the internal Joule and Peltier heating [1] shows that in a TEG the maximum attainable energy conversion efficiency η is limited by the Carnot efficiency η_C multiplied by a factor $\eta_{TE} < 1$, the so-called thermoelectric generator efficiency:

$$\eta = \frac{P_{el}}{dQ_{in}/dt} \le \underbrace{\frac{T_{in} - T_{out}}{T_{in}}}_{\eta_c} \cdot \underbrace{\frac{\left[(1 + ZT_{av})^{\frac{1}{2}} - 1\right]}{(1 + ZT_{av})^{1/2} + 1 - \eta_c}}_{\eta_{TE}} \qquad (5)$$

with

$$T_{av} = (T_{in} + T_{out})/2$$

The variation of η_{TE} with the figure of merit ZT is displayed in Fig. 3. Only for small $ZT << 1$ the generator efficiency is approximately a linear function of ZT, while it saturates for large values of ZT. Consequently, striving for ever higher ZT is not rewarded by a proportional gain in efficiency, while other aspects in the optimization of real-world TEGs may have a much larger impact.

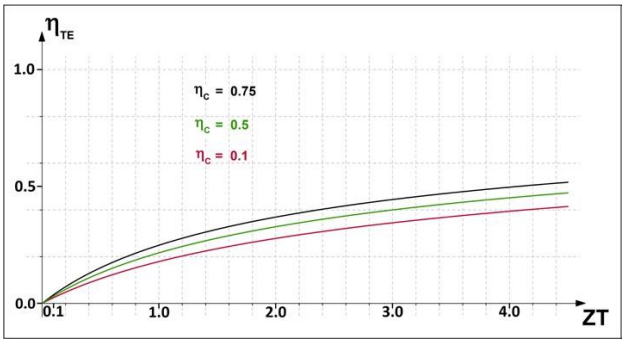

Fig. 3: Thermoelectric generator efficiency vs. figure of merit ZT

Thermoelectric power factor

In the situation sketched in Fig. 2 the electric output power can be factorized as

$$P = A_{heat} * \Pi * (\Delta T_{ext})^2$$

with (6)

$$\Delta T_{ext} = T_{high} - T_{low}$$

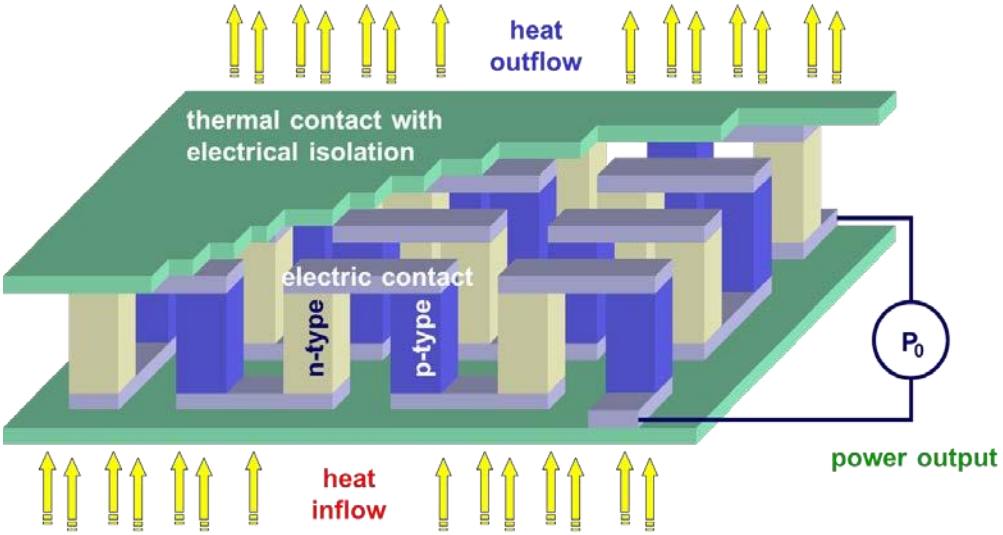

Fig. 4: Schematic view of a microstructured vertical thermopile.

Here A_{heat} is the cross-sectional area of the TEG passed by the heat flow and ΔT_{ext} is the externally controlled (given) temperature difference between waste heat source and ambient heat sink. The thermoelectric power factor Π depends on the details of device geometry and package and involves the respective physical material properties S, σ, and κ. Hence, Π is the proper figure of merit for optimizing the performance of realistic TEGs including the effects of electrical and thermal contacts, thermal leakage, package etc.

Optimized design of a microstructured thermopile

As an illustrative example, we derived the power factor for the model of a vertical thermopile consisting of a large number of microstructured thermocouples connected electrically in series and thermally in parallel. We include a thermal series resistance K_S of the package, but neglect any electrical contact resistances. The crucial parameter is the length of the thermocouples l_{TC}. We find the asymptotic expressions:

For small l_{TC}:

$$\Pi = \frac{1}{16}\frac{A_{TEG}}{A} \cdot \frac{S_{TC}^2 \sigma}{\kappa^2} \cdot \frac{l_{TC}}{(A_{TEG} \cdot K_S)^2} \qquad (7)$$

For large l_{TC}:

$$\Pi = \frac{1}{16}\frac{A_{TEG}}{A} \cdot S_{TC}^2 \sigma \cdot \frac{1}{l_{TC}}$$

where A_{TEG} and A denote the thermoelectrically active and total chip areas, respectively, S_{TC} the relative thermopower of one thermocouple, and σ and κ their respective electrical and thermal conductivity. As Π rises linearly with l_{TC} for small values and falls with $1/l_{TC}$ for large values, Π shows a maximum value in between. For "real-world" design parameters, as encountered in an industrial CMOS-process, we find l_{TC} in the range of some 10-100µm.

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Understanding Power Semiconductor Technology Platforms for Building a Viable and Sustainable Product Roadmap

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Abstract

In this paper, key technical pillars for a power device technology and product development roadmap are discussed. First, the main performance requirements of power semiconductors are outlined to establish modern development trends that can lead to a viable power device development roadmap. The basic principles of power semiconductor "Technology Platforms" will be presented in relation to well- defined "Device Sections". In addition, device classification and technology complexity aspects will be reviewed as important technical pillars in the roadmap building process. Understanding the above can help map out future development tasks targeting next generation products with improved performance over cost ratios.

Keywords: Power Electronics, Power Semiconductors, Technology Platforms.

INTRODUCTION

Power electronics applications are the foundation for driving the electrification mega-trend by providing efficient, sustainable, and reliable energy for the urban, industrial and transportation sectors. At the heart of this trend lies the power semiconductor device [1] which is responsible for modulating and controlling the electrical energy flow between the energy source and the application load. Therefore, power semiconductors are today present in all parts of the electrical energy chain, starting with low power applications such as computers and mobile phone chargers up to very high-power applications such as for grid systems (see Figure 1).

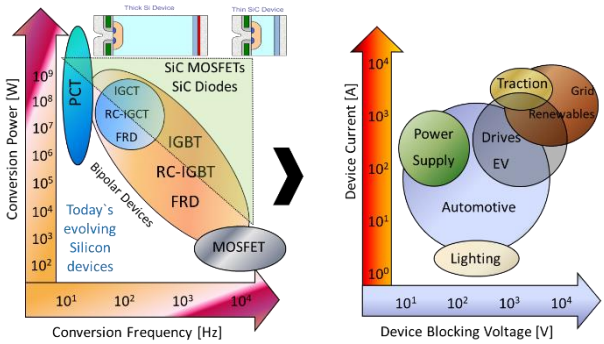

Fig. 1. Power semiconductors and applications.

For decades, Silicon based power semiconductors have dominated the power electronics market. They have maintained pole position through tremendous advancements in materials, process fabrication and the design and architecture of different device concepts. The prominent market position of Silicon power devices will be maintained due to the mature technologies and the continuous advancements in electrical characteristics, ratings, and reliability [2]. However, power devices based on wide bandgap materials such as Silicon Carbide (SiC) and Gallium Nitride (GaN) are currently employed in many applications due to their superior properties and potentially near ideal electrical performance. Such attributes are welcomed today by system designers as they enable higher power densities with increased operating efficiencies. For example, recent design and process breakthroughs resulted in a wide range of SiC MOSFET product platforms. This led to substantial growth in market adoption for key applications such as in automotive drivetrains.

The continuous drive for improved performance for both Silicon and SiC based power devices will be based on developing more advanced technologies. In this paper, the basic principles of power semiconductor "Technology Platforms" [3] will be presented and in relation to the main power semiconductor component sections at both chip and package levels. To build a viable and sustainable technology and product roadmap aligned with an established industrial business strategy, understanding some key roadmap technical pillars is important as shown in Figure 2 and discussed in this paper.

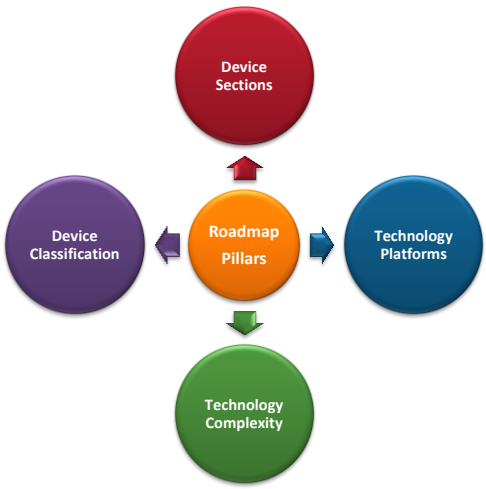

Fig. 2. Power semiconductors roadmap technical pillars.

These four technical pillars can aid research and development teams in industry and academia to devise future power device development projects targeting new technologies and products with improved overall performance over cost ratios. It can also assist with recent development trends addressing different application requirements with respect to device optimisation and customization (see Figure 3). Generally, the paper will focus on vertical devices targeting high power levels compared to lateral devices in the low power segment.

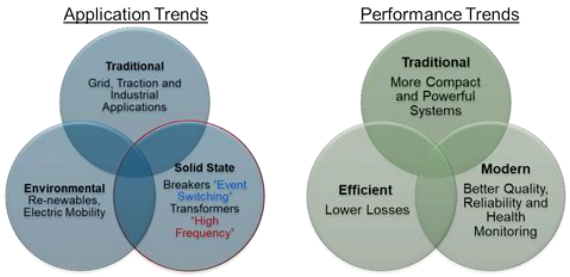

Fig. 3. Power electronics application and performance trends.

As an example, it is worth noting that more applications are emerging (e.g., renewables, EV and solid-state breakers or transformers) with different performance requirements. Advanced solid-state solutions requiring power electronics platforms, such as DC breakers, necessitate the power semiconductor to be optimized for so-called "Event Switching" operational mode as opposed to typical switching patterns in inverters. On the other end of the scale, HV devices need to be optimized for higher operating frequencies (>5kHz) required in resonance topologies employed in DC/DC conversion.

DEVICE REQUIREMENTS AND DEVELOPMENT

There exists a long list of electrical and reliability performance requirements for power semiconductor components [4]. However, the primary considerations can be divided into three categories as shown in Figure 4 and listed below:

1. **Power:** power density capability (electrical losses and thermal management)
2. **Control:** controllable switching (gate response, gate charge, turn-off softness, and EMI)
3. **Margins:** safe-operating-area, fault-handling capability, and reliability

Devices targeting high power densities aim for low conduction and switching losses, low thermal resistance, and high operating junction temperature. For the second category, there needs to be controllable turn-on, low gate charge, soft turn-off transients with low over-shoot voltages and minimal EMI levels. The last category, with regards to margins, includes a wide Safe-Operating-Area (SOA) associated with the turn-off current capability, fault-withstand capability such as short-circuit for IGBTs and MOSFETs or Surge Current for IGCTs and Diodes. In addition, the device (not the package) reliability requirements are associated with current and voltage sharing for devices arranged in parallel or series; stable conduction and stable blocking with no short to long term parameter drift or degradation and very low failure rates (FITs) due to cosmic rays.

When considering all the above issues, design engineers must also evaluate the attributes of the package. There is a continuous trend towards more compact and powerful packages, which combine a higher device packaging density with optimized chip and electrical layout designs for improved thermal properties and low parasitic elements. Improved joining technologies are crucial to achieve low thermal resistance and increased temperature and power cycling capabilities. The package role for device protection from harsh environmental conditions such as humidity is also a critical subject today.

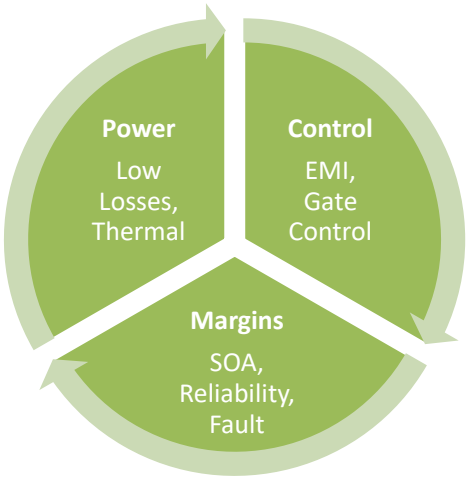

Fig. 4. Power semiconductor component requirements.

For power devices in general [5], the main technology drivers for providing higher power are always approached on two principal levels as illustrated in Figure 5 and listed below:

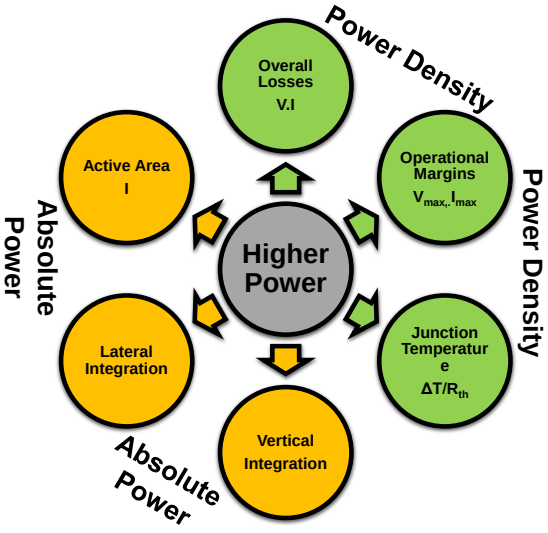

Fig. 5. Power Device technology drivers for higher power.

POWER DEVICE COMPONENT SECTIONS

To better understand the power semiconductor component, the chip and package structures can be each divided into different and distinctive sections as shown in Figure 6. These sections are defined by having clear functional targets and can be interchangeable with other different section concepts. Hence, a good understanding of each section building blocks, evolution and development trends is necessary for creating a viable power semiconductor product roadmap. In the following, we will outline the chip and package sections separately.

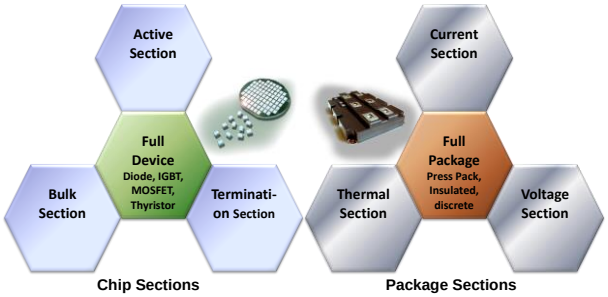

Fig. 6. Power semiconductor component sections.

Chip Sections

At chip level, the structure can be divided into three sections; namely the Bulk Section, the Termination Section, and the Active Section as shown in Figure 7 below with more detail:

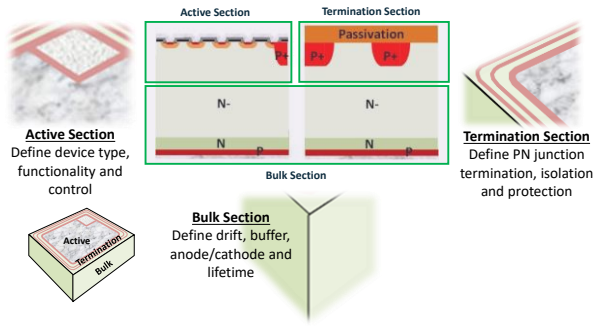

Fig. 7. Power semiconductor chip sections (e.g., IGBT).

The Bulk Section: is key for defining the device blocking capability while strongly affecting the device overall losses and operational mode (e.g., Unipolar or Bipolar). The bulk region also defines the bipolar gain levels for bipolar switching devices such as IGBTs and IGCTs which plays a critical role for the device performance under different operating conditions. The Bulk Section consists mainly of

- Lightly doped N- drift region which is the main design feature that distinguishes power devices from their low power counterparts. The N-drift region parameters (doping and thickness) mainly define the device blocking capability and voltage class. Other advanced bulk designs include lowly doped N-type and P-type pillars for providing super junction device concepts such as those in high voltage MOSFETs.
- Higher doped N-type buffer region is required for Punch-Through (PT) or Field-Stop (FS) type devices. When omitting the N-buffer region, a Non-Punch-Through (NPT) structure is obtained. Reverse blocking NPT type devices are also feasible as mentioned in the following sections.
- The bulk also incorporates higher doped P collector / anode regions (for IGBT and IGCT) or N cathode / drain regions (for Diode and MOSFET). For example, the difference between the Unipolar MOSFET and Bipolar IGBT is in principle a change from a highly doped N-type Drain to P-type Collector which enables bipolar mode behaviour of the IGBT.
- Shorted N-type regions (collector shorts) to realise a Reverse Conducting RC-IGBT or other special designs.
- Lifetime control in the bulk plays also an important role for excess carrier profiling (plasma engineering) for bipolar devices.
- Metallization layers for low ohmic contact and packaging.

The Termination Section: is positioned on the edge of the device for shaping and controlling the electric field distribution "in the semiconductor" AND "at the surface" to obtain maximum voltage withstand capability with low leakage currents and stable blocking especially at high temperatures. The Termination Section consists of

- PN Junction Termination (JT) which can be based on different design concepts. For chips/die (IGBT, MOSFET), planar designs are employed including Guard Rings (GR) with or without Field Plates or Junction Termination Extension (JTE) (e.g., Variable Lateral Doping (VLD)). For larger circular wafer devices (IGCT, Thyristor, Diode) employed in hermetic press-packs, positive or negative angle edge bevelling or mesa type designs are ideal.
- Termination Passivation which incorporates several different passivation and protection layers depending on the junction termination design requirements. In principle, there are three levels of passivation layers. The first is the layer that is in direct contact to the semiconductor materials and therefore has a strong influence on the surface charge levels and electric field distribution (can be a semi-conducting layer). The second is a thin protection layer against flashovers, mechanical damage, and humidity. The third top layer is relatively thick and consists of an organic material such as polyimide to provide further protection.
- For reverse blocking or bidirectional devices, the termination section is present on both sides of a vertical device.

The Active Section: defines the device type, functionality, and controllability. Therefore, it strongly

impacts the device over-all power ratings and performance. The Bipolar Diode, Schottky Diode, Thyristor, GTO/IGCT, Bipolar Transistor, MOSFET/IGBT are all different device concepts which are based on different active section design concepts. In general, the active section consists of

- The main active area which is responsible for the current conduction, voltage blocking and switching modes of operation. For example, the active area of MOSFETs and IGBTs consists of emitter MOS cells based on planar or trench gate structures having different layouts such as cellular or linear type designs.
- The Gate control terminal and distribution for switching devices. This design differs for gate current-controlled devices such as Thyristor or Transistors than those for voltage-controlled devices such as MOSFETs and IGBTs.
- The active to termination transition region (i.e., edge of active section). This design is key to maintain robust switching along with high voltage blocking capability especially for diode designs.
- Local lifetime control in the active section plays an important role for excess carrier profiling (plasma engineering) such as for Fast Recovery Diodes.
- Frontside metallization layers for low ohmic contact and packaging.
- For bidirectional type devices, the active section is present on both sides of a vertical device.

Package Sections

Similar section definitions can be applied to the power semiconductor package as shown in Figure 8. Without going into a detailed description, the package sections can be listed as follows:

The Thermal Section: is mainly related to the thermal path of the power semiconductor package. This includes the semiconductor chip, a substrate which can consist of an insulating layer (e.g., Direct Copper Bonding DCB substrate), a Copper heat spreading layer or base-plate if present. The joining layers of the above elements such as the soldering films are also key to the thermal characteristics of the component. Optimum layout designs and materials are required to achieve the minimum thermal resistance and thermal stability during device operation.

The Voltage Section: constitute the package encapsulation materials which is key to the module mechanical robustness and to chip protection from external harsh conditions. The filling materials can range from hermetic, Silicone Gel or Transfer molding. The latter is very common for discrete package as well as modern modules employed in automotive or consumer type applications. The package substrates, terminals, frame, and cover are also important when considering the design and related dimensions to withstand and insulate very high voltages (e.g., creepage distances).

The Current Section: relates to the main current flow in the package. For insulated type modules (i.e., chip needs to be insulated from cooling system), the current flows laterally while for press-pack modules (cooling plate is electrically active), the current flow is vertical. The current path includes the chip, wire-bonds, substrate, main terminals, and base-plate (for press-pack). The gate distribution and layout design are also part of the current section and an optimum design is required for uniform gate signal propagation and switching behaviour.

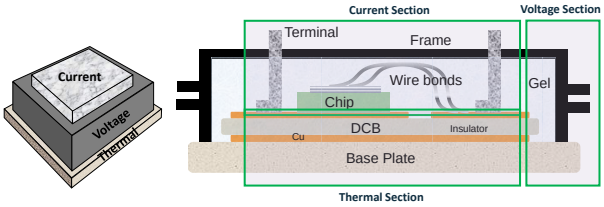

Fig. 8. Power semiconductor package sections.

The previously mentioned component (chip and package) sections can only be realised by developing the associated so-called “Technology Platforms” which will be described in the following paragraphs. It is important to outline first that the main and final target for the power semiconductor device technology development is to establish a range of product platforms or product portfolio with well-defined performance specifications and targeted applications.

POWER DEVICE TECHNOLOGY PLATFORMS

In industrial terms, “Product Platforms” are a set of products which utilizes qualified “Technology Platforms” for providing a wide range of ratings, configurations, and performance specifications. A given product platform can also constitute variants with minor modifications to achieve a range of optimised performance levels for specific applications. The “Technology Platforms” shown in Figure 9 are the main manufacturing pillars for realizing different device sections which the associated product platforms are based on. The technology platforms can be expressed as three distinctive categories or groups; namely the Process Platforms, the Design Platforms, and the Integration Platforms as follows:

- **Process Platforms:** a single or a sequence of processes with the target to realize an independent device building block and functionality for a given device section. A process platform can be as simple as depositing multilayer metals for a backside contact with no photolithography masks required, to more complex multi-mask processes to establish for example an IGBT MOS cell.

- **Design Platforms:** a single or set of design rules or guidelines for a given process platform (within the process capability) to modify or adjust a targeted performance. It also includes design layouts and starting material specification which are associated

with a given device section. Hence, adjusting mask dimensions, implant parameters, diffusion rates, layer thicknesses … etc, are all considered to be design platforms. When the design platforms are finalised, the targeted performance specification is normally reached.

- **Integration Platforms:** a set of process sequences and design features that when combined, the final device and functionalities are realised. The integration platforms can be represented as an overall process router and device structure. In addition, to develop, upgrade or deviate from an existing finalised device structure, new sets of process and design platforms need to be developed and inserted into the original process flow in the form of a single process step or set of processes (sub-router) to provide a new integration platform.

Fig. 9. Technology Platforms leading to Product Platforms.

In general terms, research and development of power devices runs through a technology development phase which requires successful technology verification followed by a product development phase which requires product qualification. Preferably, both process and integration platforms should be established and verified during technology development while some adjustments of the design platforms can still be performed during product development.

DEVICE CLASSIFICATION AND TECHNOLOGY COMPLEXITY

Device classification and customisation trends are shown in Figure 10. Many device/package footprint and performance standards have been developed to satisfy the demand of the power electronics market with respect to high level performance and multi-sourcing of components. However, customisation trends have been developed to further optimise the system performance by providing more enhanced products in terms of applicability and performance. This is justified since the power semiconductor is a key component in the power electronics system and it`s performance defines to a large degree the performance specification and competitiveness of the system. The customisation can range from simple variations to fine-tune the device losses (e.g., adjust the device technology point in terms of static versus dynamic losses), to providing alternative solutions to standard offerings (e.g., IGCT or RC-IGBT) which require more development efforts or to provide completely new and unique solutions for a specific application (e.g., press pack IGBT modules for HVDC). Some of the customised solutions can become popular due to their high-performance levels and could eventually establish themselves as a standard when adopted by different manufacturers while considering that no Intellectual Property issues are present. As mentioned previously, the high growth and expansion of power electronics applications with high performance expectations is a strong driving factor for more customisation development trends of power semiconductors devices.

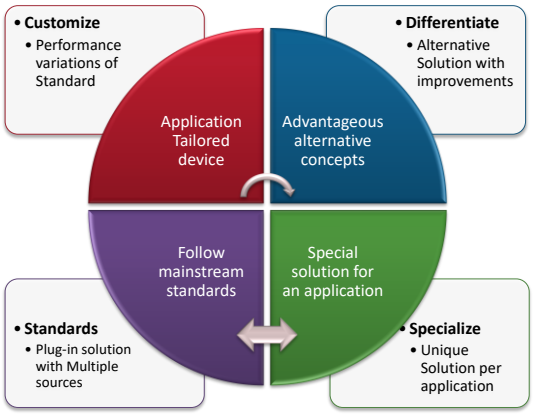

Fig. 10. Power device classification and customization trends.

Addressing technology development trends targeting higher power levels as described previously and the customisation trends listed above will require a detailed assessment of the technology complexity faced by the development teams. Figure 11 below illustrates the different complexity levels which range from developing completely new technology platforms to simple variant of existing platforms.

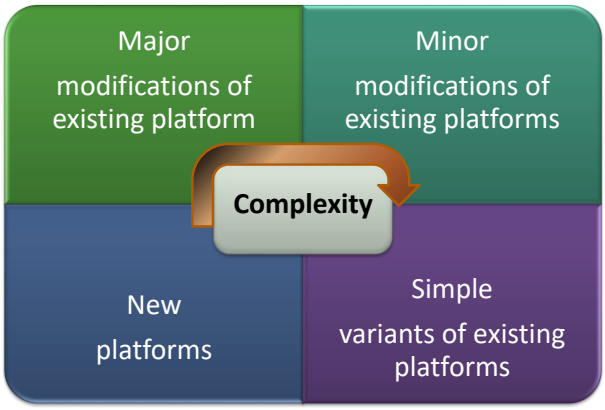

Fig. 11. Complexity levels for power device technologies.

Typically, new platforms or major modifications to existing platforms might require new process and integration platforms while minor to simple modifications can be achieved with changes to the design platforms only. In addition to the technical pillars, the other two important roadmap enablers in terms of financial and resource (skills and equipment) pillars can be planned accordingly based on the above principles.

DISCUSSION

To understand better the previous discussion, we present an example for the development of a reverse conducting RC-IGBT which combines both the switch and diode mode functionalities in a single chip as shown in Figure 12. Based on the development trends shown in Figure 5, this technology can lead to the increase of the absolute power levels by replacing the diode space with RC-IGBT chips. A reduction in the package footprint while keeping the same current rating is also possible. However, the target performance specification must ensure that other power density related factors such as losses, SOA / Reliability margins and high operating temperatures remain unaffected or preferably improved when possible. The RC-IGBT technology development is normally based on established IGBT technology platforms while carrying out the required modifications to enable reverse conducting functionality. This task becomes more challenging if the targeted RC-IGBT aims to fully replace the standard two-chip (i.e., IGBT and fast diode) component in mainstream hard switching applications. In otherwards, the RC-IGBT can be classed as a differentiating technology to mainstream IGBTs. This has been the case in recent years with RC-IGBTs employed in HVDC (e.g., the BIGT [6]) and automotive applications.

The RC-IGBT faces many development challenges to ensure that (a) no snap-back characteristics are present during on-state, (b) optimised trade-off between diode and switch mode losses, (c) good current uniformity and high SOA and (d) controlled switching behaviour.

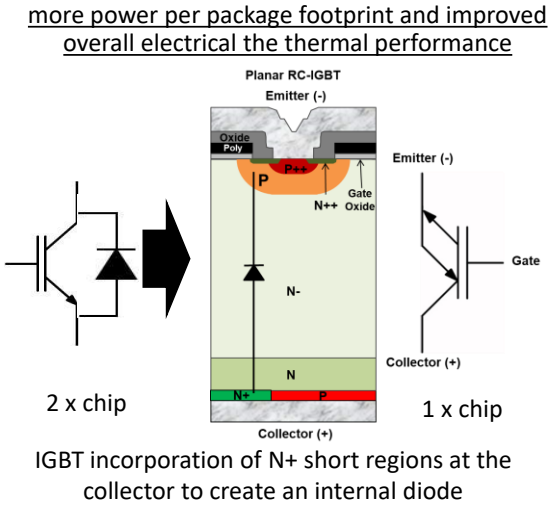

Fig. 12. From IGBT / Diode to RC-IGBT.

Overall, the RC-IGBT technology requires major modifications to an existing IGBT technology platform. The main IGBT sections where modifications are necessary are the bulk and active sections. The bulk section will require collector N+ type short regions to provide an internal diode structure while lifetime control might also be needed for plasma engineering to enable fast reverse recovery switching in diode mode operation. Hence, new process and integration platforms are developed while at the same time some of the original IGBT design platforms are adjusted to achieve the required RC-IGBT performance specification. Furthermore, the RC-IGBT could potentially require package improvements in terms of new footprint and layout designs to ensure that higher electrical and thermal performance levels are obtained due to the new integrated solution.

CONCLUSIONS

The paper introduced the growing power electronics market in relation to both modern application and performance trends. The power device requirements per application determines future development trends with focus on increased power levels, margins, and controllability. To help establish a viable technology and product roadmap, key “roadmap technical pillars” have been identified and discussed in this paper including the principles of “Technology Platforms” when related to different “Device Sections”.

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SiC Power Device Processing with special regard to Ion Implantation

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Abstract

For power device fabrication distinct challenges have to be addressed. In many fields they are identical to the needs in the CMOS world. However, some features of power device technologies require customized processes. Power devices in general are facing the main demand to lower dissipation losses caused by increasing current densities at decreasing structure sizes and optimized performance of device switching behavior at the same time. Hence, advanced manufacturing processes of wafer frontside and backside as well as for engineering of bulk properties are necessary.

Whereas MOSFETs used in CMOS IC switches typically operate at a parameter range of some µA at voltages of <5V, power devices utilize up to kA currents at voltages of up to kV range. Therefore chip areas are much larger to cope with these requirements. Also, 3D device structuring is required in order to enable current flow from the chip frontside to the backside.

In general technology requirements in combination with given raw material properties drive manufacturing challenges. That in turn puts pressure on advancing both single unit process steps as well as novel integration concepts, also incorporating feed forward run to run systems and new computational capabilities towards AI. The overall equipment effectiveness in terms of availability, performance and quality is key for an economic production environment. Machine learning based concepts are developed both for the prediction of individual equipment behavior as well as to manage complexity in the overall manufacturing process line. Furthermore ML-assisted root cause analysis is developed to identify important "hidden" parameters in production equipment as well as to help revealing and understanding complex correlations.

Keywords: SiC, Ion Implantation

As of today, Silicon is still the dominant mainstream material system with IGBTs and various kinds of Power MOSFETs still being optimized for upcoming applications. Due to their decade-long history and the maturity of the involved manufacturing processes it becomes increasingly difficult to find ways to enhance their efficiency at reasonable costs. Prominent examples are the increasingly stringent requirements towards total thickness variation of low voltage power MOSFETs as well as balancing the active dopant concentration on sub-percentage level for advanced super junction concepts.

In recent years Wide Band Gap materials like SiC and GaN gained momentum and market share. Their application range partially reaches into the one of the Silicon technology portfolio. Products based on WBG technologies are currently more expensive compared to their Silicon equivalents, yet with decreasing complexity and cost of the overall system solution for the customer they achieve the break-even point for an increasing number of applications. However, advanced processes especially in terms of efficient and high-quality epitaxial layer growth, advanced doping processes by ion implantation and subsequent annealing as well as challenges in wafer thinning bare a significant amount of innovation that to a large part still has to be exploited.

Epitaxial layer growth of high quality 4H-SiC is not only an art by itself, the productivity of currently available equipment also bottlenecks fast fab extensions in the field of SiC device processing. Significant equipment competition and process innovation is driven in that field.

Thinning of SiC wafers from their original 350µm thickness to the final device target (typically around 100µm for 1200V devices) is difficult and costly. SiC belongs to the hardest material systems and can only by grinded by diamond – the economic pain is obvious.

Besides epitaxy and wafer thinning ion implantation certainly plays a key role in SiC device processing. Due the negligible amount of diffusion in SiC all dopant profiles have to be placed exactly and in its final form via implantation processes. Whereas the principal design of ion implanter equipment still stays the same as for

silicon, distinct adaptions have to be made in terms of ion source technology and end station design.

Dedicated ion sources are required to create efficient amounts of Al ion beams. Currently competition between vaporizer and sputter source designs can be observed – both with their advantages and disadvantages. Vaporizer sources are a known technology since decades for usage of Sb implantations in silicon-based technologies, however, transition times from Al operation to other implantation species like N or P are significant and therefore reducing production efficiency. Sputter sources are a relatively new technology in volume production, therefore still an active field of research in order to maximize ion source lifetimes as well as operational efficiency.

In terms of end station adaptions especially the capability of processing hot implants is desperately needed especially for high dose contact applications. In-situ annealing of crystal damage prevents 4H-SiC from being transformed into other polymorph types of SiC and therefore harming device operation. 500°C are established as industry standard for hot implantation, however, research suggests that even more elevated temperatures might further benefit specific applications.
Since SiC is a quite dense material (3,21g/cm^{-3}) with hardly any diffusion of doping elements at practicable temperatures, dopant profiles have to be placed exactly to its final position by ion implantation. This implies that implantation energies are quite high for deep layers. One possible way of overcoming this obstacle is the usage of channeling implantation for the creation of deep extended dopant profiles. Due to the low probability of large energy transfer collisions ion stopping is dominated by the electronic drag, allowing for an extended tail of the implantation profile. That can result in plateau-like profiles instead of gaussian peaks and results in less surface near damage creation. Depending on the combination of crystal channel used as well as implantation parameters like element, implant energy and dose along with substrate temperature critical angles will differ significantly. Independently of the exact value, enhanced effort for tool and wafer material control will be required.

Overall, basic implantation knowledge for SiC application exists, however, there is significant room for further innovation as well as process optimization in the years to come.

As known from the silicon world also implantation in SiC have to be followed by thermal anneals in order to remove implantation damage and to activate dopants. In 4H-SiC temperatures in the range of 1600 – 1900°C are required, giving raise to the development of dedicated furnace systems. From a process point of view the usage of graphitic carbon capping layers is advised to stabilize the wafer surface and to avoid step-bunching.
Number footnotes separately in superscripts. Place the actual footnote at the bottom of the column in which is cited. Do not put footnotes in the reference list.

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GaN HEMT Device Model Development for Implementation of Different Circuit Designs

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Abstract

GaN HEMT devices (with different dimensions) have been investigated using 16- and 22-element small-signal equivalent circuit Model. The percentage error is estimated to show the difference in extracted parameters using 16- and 22-element small-signal equivalent circuit model which assist in choosing the accurate small-signal model for large gate periphery GaN HEMTs. For device's low power operation linear models are sufficient. In order to achieve higher certainty for high power applications, the non-linear behaviour of the device must be considered. While generating the large-signal device model, the nonlinear capacitances C_{gs} and C_{gd}, as well as the current source I_{ds} are primarily considered to capture the non-linear behavior of the device. The capacitances, C_{gs} and C_{gd}, are dependent on applied bias i. e. V_{gs} and V_{ds}. The Angelov model for I_{ds} is used to generate the non-linear model parameters which uses the multi-bias small-signal equivalent circuit parameters.

Keywords: HEMT, I-V Characteristc, S-Parameter, 16- and 22-Element Equivalent Circuit Model, Large-Signal Model.

INTRODUCTION

Gallium nitride-based HEMTs (high-electron mobility transistor) provides higher cut-off frequency and higher breakdown voltage and shows outstanding power and frequency performance over the past decade [1] [2]. GaN HEMTs are now the most promising devices for RF switches, low noise amplifiers and power amplifiers, which are essential components of transceiver systems. The need for an accurate device model becomes paramount for the design and analysis of any active circuit. Small-signal equivalent circuit models are adequate for low power operation devices. The non-linear behaviour of the device must be considered in order to obtain high accuracy for high power applications. GaN device modeling has been the subject of numerous reported works. There have been claimed to be several ways to simulate GaN HEMTs, each with advantages and disadvantages [3] [4] [5] [6] [7]. Several large-signal HEMT models (empirical equation based), including the ASM HEMT model [8], Curtice model [9] and Angelov (Chalmers) model [10], have previously been created and integrated with several commercial computer-aided design (CAD) programs. Different formulas are used by these models, based on the I-V characteristics between the subthreshold and saturation area, to fit the electrical behavior of the device.

In this work, the 16- and 22-element small signal model were used for parameters extraction. GaN HEMT devices with Different dimensions have been investigated using these techniques. The device's Stability Factor, K-factor, Maximum Gain and Delta Factor were simulated. The 16- and 22-element small signal equivalent circuit models are compared and the percentage error were estimated to depict the preciseness of 16- and 22-element small signal model to be chosen for large gate perphery devices.
The small model should be accurate, easy to apply in commercial simulators and relatively quick to extract. In this work, the multi-bias small-signal equivalent circuit parameters are extracted which is beneficial in generating the non-linear model of the device.

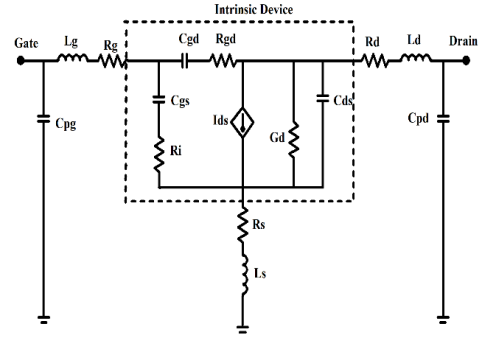
EXTRACTION METHODOLOGY

Small-signal model of the microwave transistor has been the subject of much debate and is still debated [20-22], due to the interests and challenges this area of research.

The small-signal models often act as the basis of large-signal and noise modelling which provides the main reason for such a great interest. The small-signal equivalent circuits used for the parameter extraction are shown in figure 2 (a) and (b). Figure 2 (a) shows the 16-element circuit consisting of 8 intrinsic and 8 extrinsic parameters and figure 2 (b) shows the 22-element circuit consisting of 10 intrinsic and 12 extrinsic elements. The intrinsic elements are surrounded by the dash lines in

figure 2(a) and (b). These models consider the the parasitic resistances (R_s, R_g and R_d); contact inductances (L_g, L_s and L_d); the gate and drain pad capacitances (C_{pg} and C_{pd}). The C_{gd}, C_{gs} and C_{ds} are the intrinsic capacitances between different contacts (such as gate-drain, gate-source and drain-source). g_d and g_m represents the output and intrinsic transconductances. The channel resistance associated are R_i and R_{gd}. The τ is the time delay i.e. the change of gate voltage w. r. t. drain current. The parasitic pad capacitances were differentiated as 6 different capacitances in 22-element model: C_{pdi}, C_{pgi}, C_{gdi}, C_{pda}, C_{pga} and C_{gda}. G_{gsf} and G_{gdf} models the conduction current through the gate-source and gate-drain terminals. The conventional approach has been considered for extraction of parameters and has been depicted as a flow chart in figure 3. First, the experimental [19] S-parameter at V_{gs}=-5 V and V_{ds}=0 V (cold pinch off condition) is used to estimate the pad capacitances. When determining the parasitic inductances and resistances, V_{gs} and V_{ds} in a cold HEMT measurement, i.e., 0 V. The curve fitting method is then applied to quantify the resistances and inductances. Additionally, the parasitic capacitances and resistance under the gate are considered [12], the extrinsic parameters' fidelity is increased, and this is crucial for the intrinsic parameters to be accurate.

The measured s-parameters are transformed into Z- and Y-parameters at V_{gs}=-3 V and V_{ds} = 10 V, followed by the extrinsic parameters de-embedding, to obtain the intrinsic parameters. These extrinsic and intrinsic parameters are the initial values for the circuit simulation.



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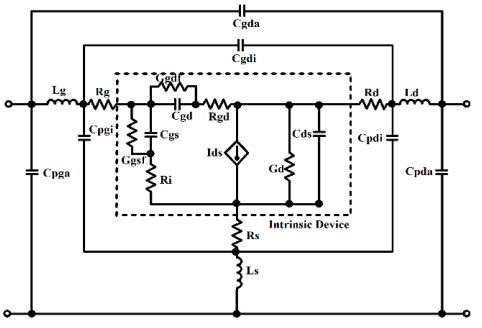


(b)

Fig. 2. (a) 16-Element Small-Signal Equivalent Circuit Model and (b) 22-Element Small-Signal Equivalent Circuit Model.

Subsequent to the extraction small-signal equivalent circuit is designed in ADS software using these parameter initial values followed by the optimization and tuning the parameters to get good congruency between the measured and simulated s-parameters.

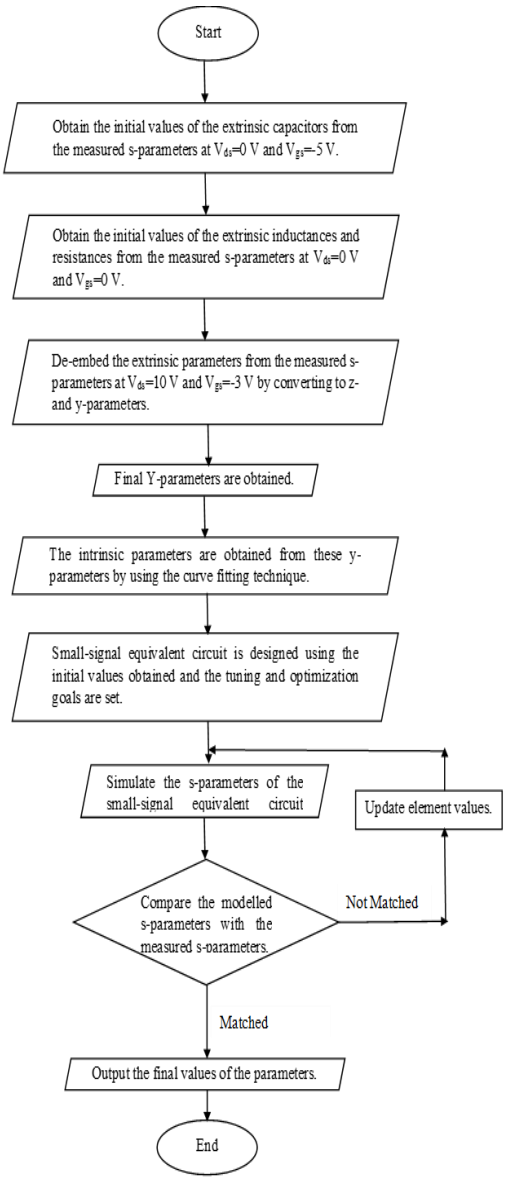
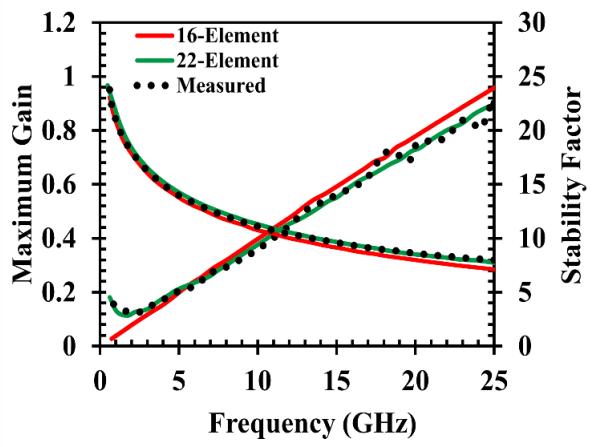


Fig. 3. Flow chart representaton of parameter extracton technque.



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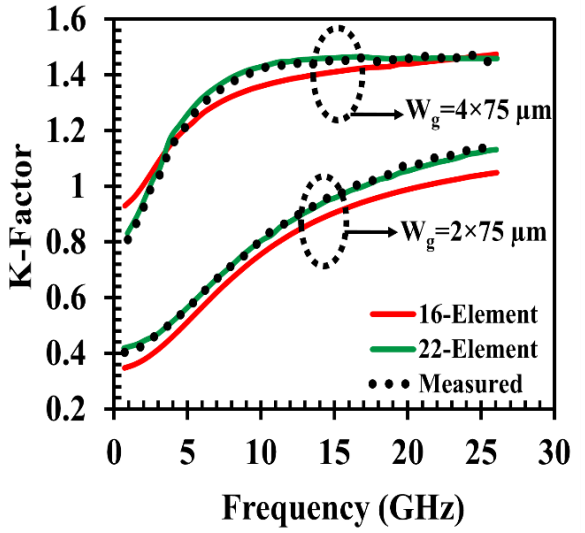

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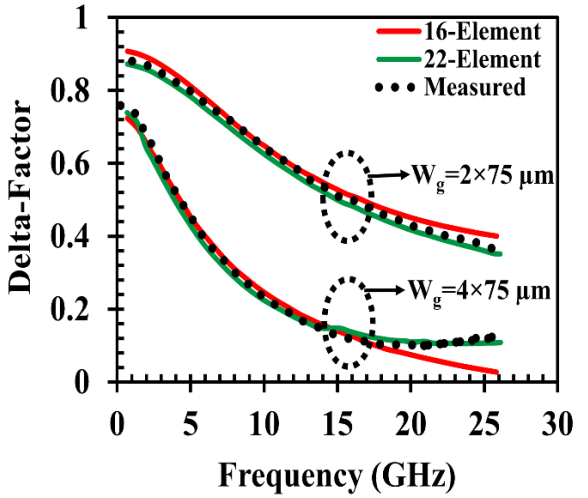


(c)

Fig. 4. Comparison of (a) Maximum Gain and Stability Factor, (b) K-Factor and (c) Delta Factor between the measured, 16- and 22-element small-signal model of GaN HEMT.

RESULTS AND DISCUSSION

Following the extraction procedure, explained by the flow chart in figure 3, the intrinsic and extrinsic parameters were extracted using 16- and 22-element model using the measured s-parameters. The circuit was designed in ADS and S-parameter were simulated (frequency range 500 MHz to 26 GHz). To get a good congruency between the measured and simulated results, the optimization and tuning tools in ADS were used to tune the parameters [19] for both the models. The GaN HEMT devices, having different dimensions, were investigated. After optimization, the Stability Factor, K-factor, Maximum Gain and Delta Factor were simulated using both the models. The Stability Factor, K-factor, Delta Factor and Maximum Gain are represented (in terms of S-parameters) as follows [23]:

$$\textit{Stability Factor} = 1 + |S_{11}|^2 - |S_{22}|^2 - |S_{11}*S_{22} - S_{12}*S_{21}|^2 \quad \text{.....(1)}$$

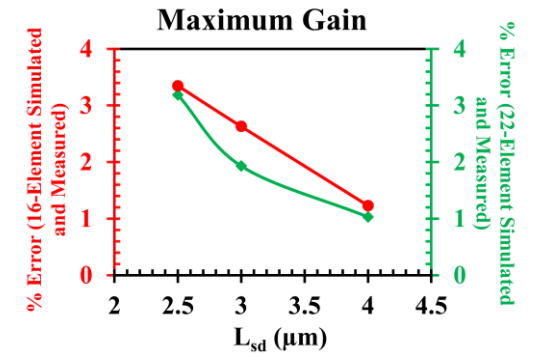
$$K\text{-}Factor = \{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2\} / \{2*|S_{12}*S_{21}|\} \quad \text{.....(2)}$$

$$\textit{Delta Factor} = \Delta = S_{11}*S_{22} - S_{12}*S_{21} \quad \text{.....(3)}$$

$$\textit{Max. Gain} = (K - \sqrt{(K^2-1)})*(S_{21}/S_{12}) \quad \text{.....(4)}$$

The results obtained for Stability Factor, K-factor, Maximum Gain and Delta Factor for 16- and 22- element models were compared with the measured data which are depicted in figure 4 (a-c). The % error, depicted in figure 5 (a-d) were calculated between the simulated 16- and 22-element model with measured [19] Stability Factor, K-factor, Maximum Gain and Delta Factor for GaN HEMTs. From figure 5, it can be observed that, as the source to drain distance is increased, the percentage error is reducing for the 22-element model. In case of stability factor the reduction is as following:13.47%–8.11% with difference of 5.36% for L_{sd}=2.5 µm, 13.05%–7.40% with difference of 5.65% for L_{sd}=3.0 µm and 10.42%–4.74% with difference of 5.68% for L_{sd}=4.0 µm. Analogous effect can be observed for the increased number of fingers of the device. Thus can be concluded that the 22-element model gives more accurate small-signal equivalent circuit model for large gate periphery devices [19].

The intrinsic parameters have been extracted for different V_{gs} and V_{ds} as these parameters are bias dependent. The intrinsic parameters were optimized (extrinsic element values were constant). The RF characteristics (fT, fMax., voltage gain, current gain, power gain) of the GaN HEMT are the functions of device intrinsic parameters. The intrinsic parameters of the device are dependent on the gate and drain bias. Hence, the gate and drain bias will affect the RF characteristics (fT, fMax., voltage gain, current gain, power gain) of the GaN HEMT. To show the bias dependency of the intrinsic parameters, the extraction were carried out for different V_{gs} and V_{ds}. Fig. 6 (a-f) represents the intrinsic parameters versus gate bias for different drain bias.



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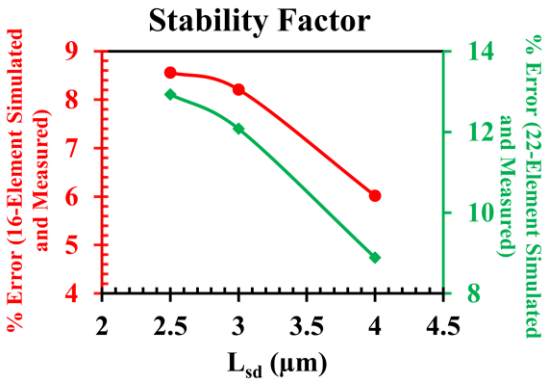

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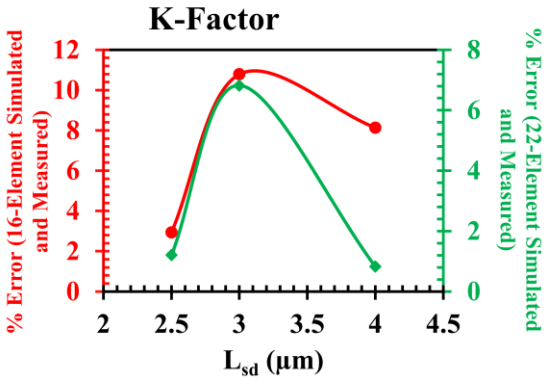

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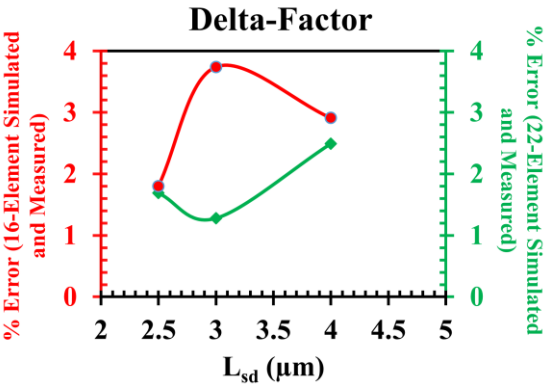
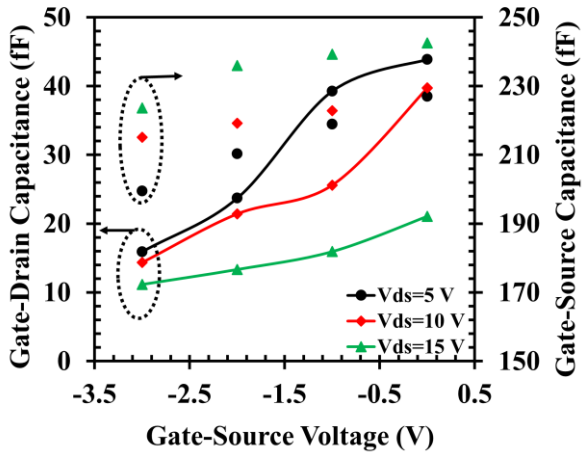


(d)

Fig. 5. The percentage Error Between The 16- And 22-Element Model Simulated with Measured (a) Maximum Gain, (b) Stability Factor, (c) K-Factor and (d) Delta Factor.

The depletion layer behind the gate controls the capacitance (C_{gs}) between the gate metal and channel charge in 2DEG. When V_{gs} rises from the pinchoff region, C_{gs} rises as well. Beyond a certain voltage, the drain current saturates as V_{gs} rises, and the depletion area stops changing. C_{gs} and V_{gs} become constant at that voltage. The drain voltage creates a lateral electric field that accelerates the channel's carriers. As a result, the depletion layer depth is decreased, which leads to a modest increase in C_{gs} with V_{ds}. The extended depletion region in the gate-drain area is the cause of C_{gd}. This depletion area widens as the drain voltage rises. As a result, a slight rise in C_{gd} with rising V_{ds} can be seen. A collapse follows a strong increase in the G_m-V_{gs} characteristic that occurs above pinch-off voltage which can be observed in figure 6(c).



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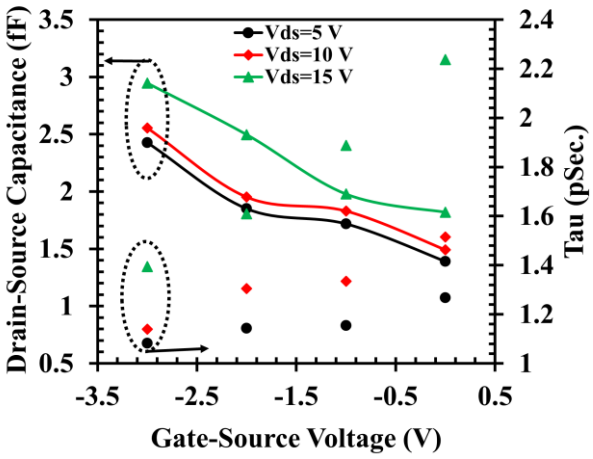

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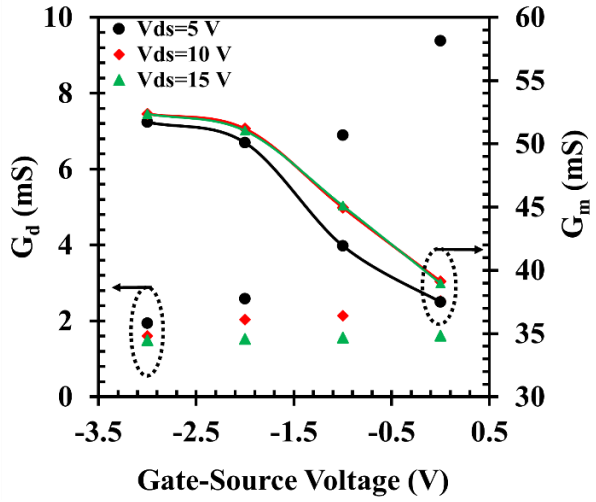

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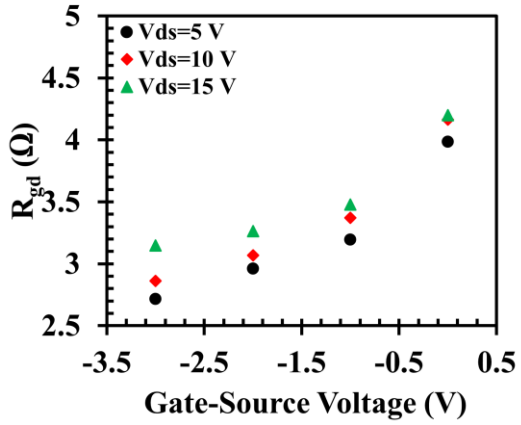

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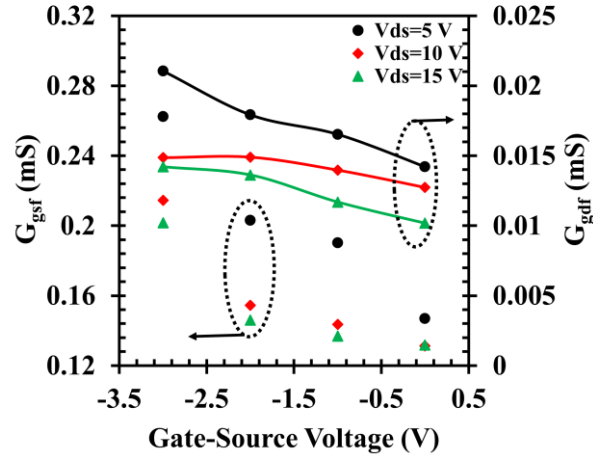
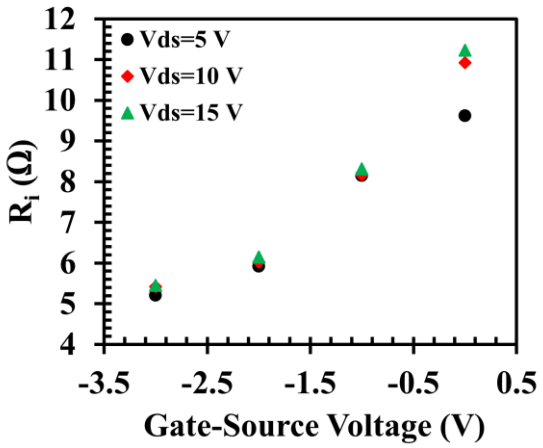


(e)

Due to the abrupt increase in current with V_{ds}, G_d grows with V_{gs} at low V_{ds}. However, in the saturation zone, G_d is minimal. With V_{gs} and V_{ds}, R_i and R_{gd} rise. The transit time for the electrons grows longer as the depletion zone spreads in the gate-drain region. As a result, rises with V_{gs} and Vds.

After the multibias linear model extraction, the non-linear model of the device can be developed. While generating the large-signal model, the non-linear



(f)

Fig. 6. Bias dependent intrinsic parameters for GaN HEMT with 0.4 µm gate length and source to drain length 2.5 µm.

behavior of the device must be captured. Hence, the nonlinear capacitances C_{gs} and C_{gd}, as well as the current source I_{ds}, are primarily considered. The current source (I_{ds}) demonstrates the electrical performance of HEMT, which is controlled by Gate voltage and drain voltage. The I-V characteristic of the device can be accurately modeled using this non-linear current source.

CONCLUSION

The findings from the 22-element model demonstrate strong correlation and fewer percentage mismatch with the measured data. The devices with large gate periphery show high accuracy. Hence, the 22-element model gives more accurate small-signal equivalent circuit model for large gate periphery devices. The large-signal model for GaN HEMT device can be generated for further circuit design implimentations with precision to measured results using the multi-bias small-signal equivalent circuit parameters.

ACKNOWLEDGEMENT

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Impact of Super Junction Concepts in Silicon and Wide Bandgap Semiconductors (Invited paper)

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The first two-dimensional varactor, which closely resembles the modern day super junction concept, was proposed by Shirota and Kaneda in 1978, as shown in Fig 1, to enable spread of depletion regions into a multi-layer n/p layer composite structure so that the range of capacitance-voltage characteristics could be widened in comparison to conventional varactor structures [1]. The first reported charge balance structure to enhance the breakdown voltage in a lateral device is the REduced SURface Field (RESURF) concept, introduced by Apple and Vaes in 1979 [2]. This concept alone widened the scope and application of power ICs into a multi-billion market today. The first power device structure employing composite n/p layer was proposed by Coe in 1982 [3] and the first super-junction device making use of such layers in a vertical device was reported by Infineon in 1990s [4]. Ever since, the super-junction concept has revolutionised the silicon power MOSFET market up to 900 V. This is simply because, the super-junction concept enabled silicon power MOSFETs to achieve area specific on-state resistance for a given breakdown voltage beyond the 1-D material limits of Silicon. As shown in Fig 2, doing so enabled achievements of linear increase in on-state resistance with breakdown voltage, when historically, the onstate resistance (Rds(on)) relationship as a function of breakdown voltage is typically $BV^{2.5}$ in conventional MOSFETs. Not only that, but the super-junction concept also led to better area effectiveness of the devices to fit into smaller packages as well as significant reduction of switching losses. The area-specific on-state resistances of the present-day SJ- power MOSFETs are only limited by their capacitive effects.

The super-junction concept is highly suited to MOS-Bipolar devices such as the IGBT [5] and/or the Clustered IGBT [6], as shown in Fig 3 and 4. In these devices, the pillars enable (a) charge balance (b) a path for extraction of holes in the turn-off conditions and keep the drift regions as thin as possible. In an IGBT, employing a p-pillar is a complex design challenge. In the trench Clustered IGBTs, where these p-pillars are only connected to the floating p well, an effective PMOS can be formed to extract holes in a very effective way, which can lead to a very significant reduction in turn-off energy losses from 7.2 mJ to 2.5 mJ, without affecting on-state losses, as shown in Fig 5 [7]. As TCIGBTs are devoid of limitations posed by the dynamic avalanche, our studies showed that such SJ-TCIGBTs can be operated at 500 A/cm^2 with significantly low switching losses and can operate beyond the 1-D material limits of SiC at 3 kV or so, as shown in Fig 6.

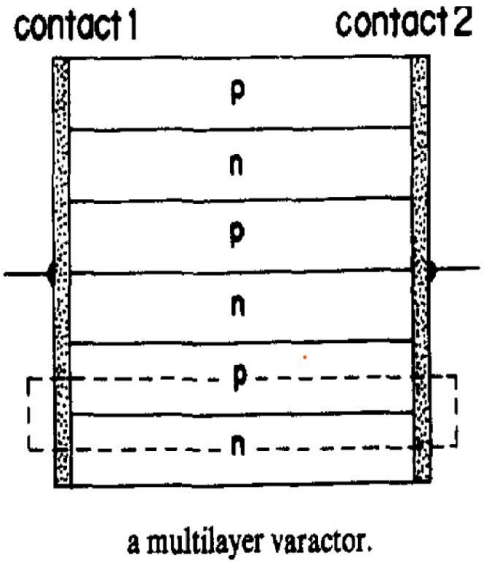

Fig 1. The simplified view of the Varactor [1].

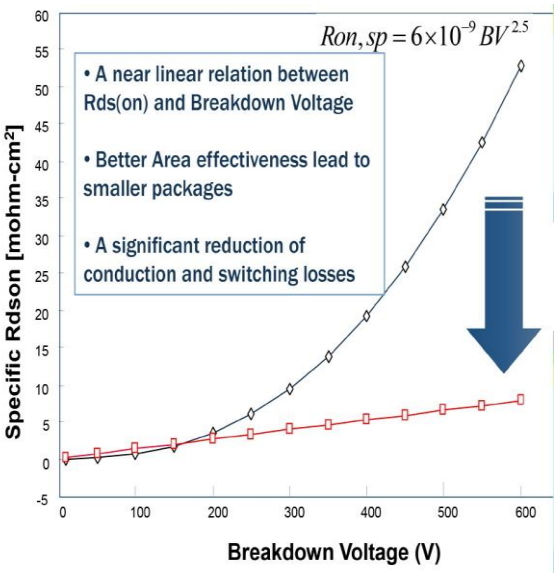

Fig 2. The influence of Super-junction on the Ron(sp) as a function of breakdown voltage.

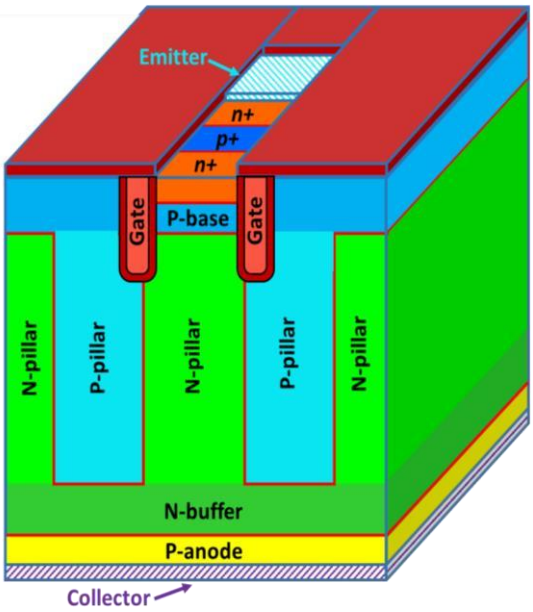

Fig 3: A Simplified 3-D cross-section of a SJ-IGBT

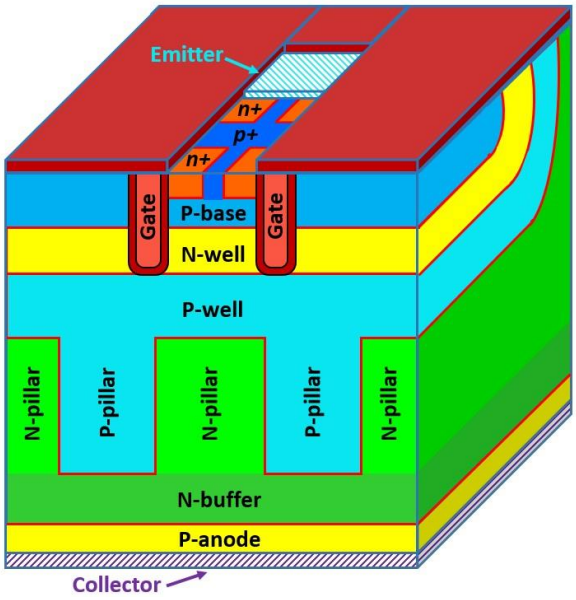

Fig 4: A Simplified 3-D cross-section of a SJ-TCIGBT

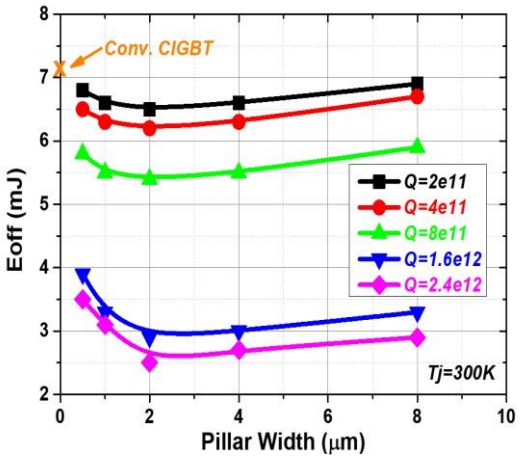

Fig 5: Predicted reduction in Eoff losses as a function of SJ charge and p pillar width in a SJ-TCIGBT [7].

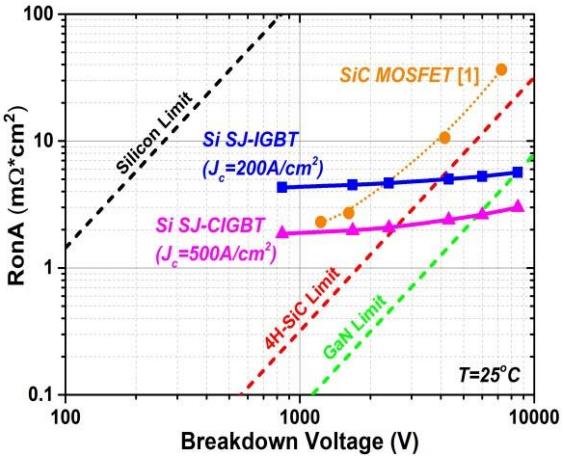

Fig 6: Predicted performance improvements of the SJTCIGBT and SJ-TIGBT [7].

The super-junction concept can be effectively used in SiC to reduce the epitaxial layer thickness as well as approach the 1-D material limits of 4H-SiC [8]. It is well known that the cost of SiC MOSFETs are considerably higher than that of Silicon counterparts. As most of the costs are in the bulk and epitaxy growth of SiC materials, it is difficult to see how these can be reduced to the levels of Silicon devices in a foreseeable future. The application of SJ concepts in SiC are like that of Silicon technology but need more advanced manufacturing facilities. Jury is out, therefore, on the performance over cost advantages of SiC SJ devices. Moreover, the increase in background doping concentrations due to the employment of SJ pillars can lead to higher switching losses in WBG technologies in SiC and conventional vertical GaN technologies. However, such is not the case with lateral devices made of Gallium Nitride, which use polarisation properties to achieve super-junction. Polarisation Junction based concepts were first hypothesised in 2006 [9] and first devices were reported in 2011 [10].

Conventional lateral GaN power devices are primarily based on positive polarisation, which results in high density 2-Dimensional Electron Gas at the AlGaN/GaN heterostructures. These devices make use of field plates to achieve high blocking voltages. As shown in Fig 7, Polarisation Super Junction based lateral GaN devices make use of double heterostructures of GaN/AlGaN/GaN structures to avail of charge balance of high density 2-Dimensional hole gas to co-exist with high density of 2-Dimensional Electron Gas and achieve charge balance. In such devices, the charges are not created by doping and are optimised by growth. Therefore, these charges are not largely dependent on temperature, which makes these GaN based Polarization Super Junction (PSJ) technologies highly suited for cryogenic operations as well as high temperature operations.

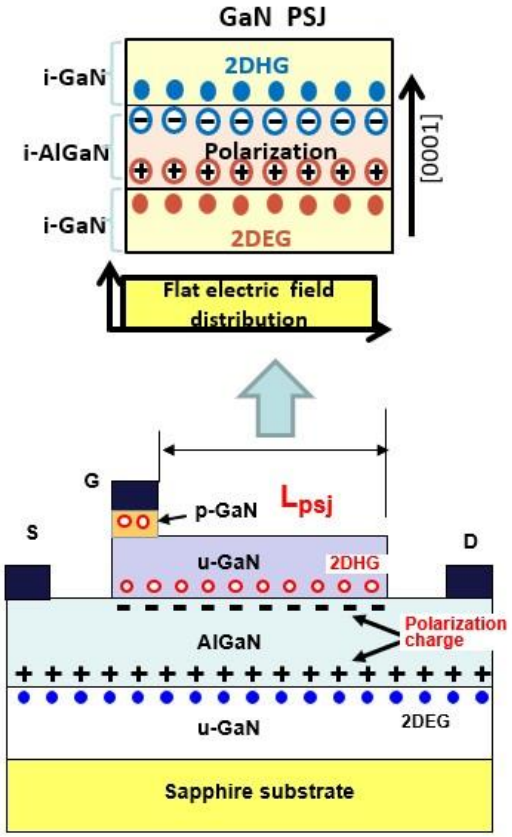

Fig 7: Details of the PSJ concept and the conceptual design of a simplified PSJ-HEMT

Material	E_{cr} (V/cm)	Q_{opt} (/cm^2)	Drift (µm) for 1.2 kV
Silicon	3e5	1e12	120
GaN	3e6	1e13	15

- Charge balance by **GROWTH**.
- Charge balance independent of temperature.

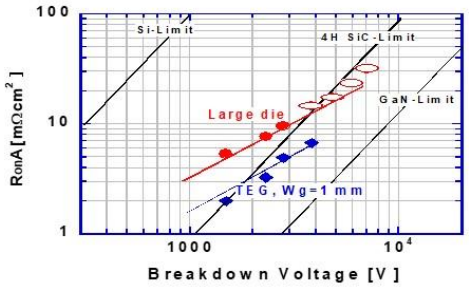

Fig 8: Key benefits of GaN technology over Silicon and the measured performance of PSJ HEMTs [13].

There are no field plates employed in the PSJ devices, which makes the processing much cheaper, and the blocking voltages can be directly scaled as a function of the charged balanced drift region (known as Lpsj) [11]. On Sapphire substrates, blocking voltages as high as 10 kV has been reported [12], while on Silicon substrates, the blocking voltage is limited by the vertical breakdown of the GaN/Silicon region. From a perspective of 1-D material limits, these devices perform close to 4H-SiC limits, as shown in Fig 8, [13] and large area devices are limited by the constraints posed by the geometrical limits posed by semiconductor processing.

Most recent results of the 1.2 kV rated large area diodes and HEMTs are highly encouraging. For example, the hybrid Schottky-Junction Diode shows excellent surge current capability [14] and no parasitic turn-on of the junction diode at least up to 6 to 8 times the rated current. 1.2 kV PSJ HEMTs show excellent static electrical characteristics as well as dV/dt capability as low as 1 kV/us, as shown in Fig 9 and with very low energy losses shown in Fig 10, which makes these devices suited for motor drive applications [15]. The bidirectional switches are in development [16] and promise to be ideal for various emerging current source inverter applications. As shown in Fig 11, PSJ technology is a platform technology on which power diodes, transistors, or bidirectional switches as well as PMOS and NMOS devices can be made simultaneously [17]. It is important to note that complementary MOS devices are possible and can be a highly suited platform for Power Management IC operating in voltages above 1.2 kV.

It is also possible to consider vertical polarization based super-junctions at nano-scale level [18]. A reduction of almost two orders of magnitude in R_{ON}.A can be achieved using VI-PSJ structures for breakdown voltage of 1kV, which could extend to three orders of magnitude improvement for 10kV devices, in comparison to conventional SiC devices, can be possible, as shown in Fig 12. Thus, the predicted performances of such devices are very attractive, but these will also require highly complex processing.

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ORAL PRESENTATIONS

New Power MOSFET and their use in Intermediate Bus Converters

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Abstract

This work investigates the performance of our latest trench power MOSFET technology in an Intermediate Bus Converter as widely used in telecom and data centre power supplies. Based on the advantages of a revolutionary new cell design combined with the benefits of an advanced manufacturing technology, the new devices combine the benefits of low conduction losses and superior switching performances with an extended SOA and good ruggedness. These features make the devices an ideal fit especially for high switching frequency applications. The recent release of 80 V and 100 V devices offers the potential for further optimization.

Keywords: power semiconductor, charge compensation, MOSFET, SMPS, IBC

INTRODUCTION

Since their introduction, MOSFET technologies have been noted as excellent candidates to be used as switches in power management circuits [1-9].
Vertical diffused MOSFET (VDMOS) structures, commercially available since the late seventies, first addressed the needs of a power switch (Fig. 1a) [1]. The superior switching performance together with a high input impedance placed the MOSFET as an attractive alternative to the bipolar technologies that dominated the power semiconductor arena at the time.
Nevertheless, the high on-state resistance limited the current-handling capabilities of the VDMOS and hence its use in power electronics applications. For medium-voltage devices, the total on-state resistance between drain and source was set by the intrinsic channel resistance, and by the JFET region between the body regions that limits the channel current flow into the drift region (Fig. 1a).
It took more than a decade of development in device design and process engineering to overcome these limitations in the late 1980s with the commercialization of the first trench gate power MOSFETs, which set a milestone for the broad adoption of field-effect transistors in the power electronics industry [1,10]. By aligning the channel along the vertical direction, the JFET region was virtually eliminated and the cell pitch dramatically reduced (Fig. 1b). The ultralow specific channel resistance achieved no longer prevented low on-state resistances, although as a result the substrate and

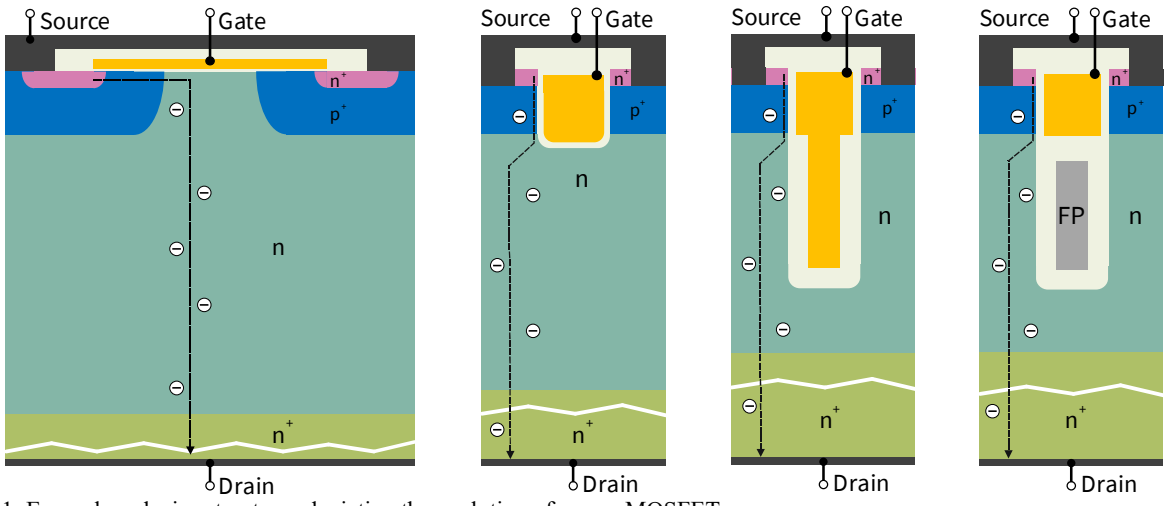

Fig. 1: Exemplary device structures depicting the evolution of power MOSFET:
a) VDMOS structure with lateral channel and planar gate
b) Trench MOSFET structure with vertical channel
c) Trench MOSFET with lateral charge-compensation by a gate-connected field plate
d) Trench MOSFET with lateral charge-compensation by an insulated field plate connected to source

package resistances became more significant contributors.
However, the remarkable increase in cell density has also brought to light significant disadvantages. The gate-drain capacitance and gate-source capacitance both increase linearly with the number of trenches, i.e. with the cell density. Together with a sublinear scaling in the on-resistance $R_{DS(on)}$, this significantly impacts the technology figure-of-merit $FOM_G = R_{DS(on)} \times Q_G$.
Since the MOSFET is uniquely controlled through its gate terminal, the gate driver circuitry has to provide the total gate charge Q_G required to turn on the transistor. In the case of high switching frequency applications, as found for switched-mode power supplies (SMPS), the lowest gate charge is desirable since it proportionally reduces the driving losses. A part of the total gate charge is associated with the gate-to-drain charge Q_{GD}, which governs the drain voltage transient. Larger values of the Q_{GD} impact the transient speed, result in an increase of the switching losses, and additionally force the use of longer dead-times. Additionally, another constraint is imposed by the Miller charge ratio: Q_{GD}/Q_{TH} must be lower than one. This is needed in order to ensure an intrinsic robustness against parasitic turn-on of the MOSFET under fast drain voltage transients [11].
The introduction of charge-compensated structures, exploiting the same principle as super junction devices, marked the beginning of a new era. The introduction of devices employing an insulated deep field plate as an extension of the gate electrode enabled the lateral depletion of the drift region in the off state (Fig. 1c) [2]. The lateral depletion alters the electric field distribution throughout the structure, and it is possible to block the same voltage within a shorter length. In turn, the electric field can now be supported by a thinner and more heavily doped drift region, which leads to a substantial reduction in the on-state resistance.
Unfortunately the field plate as an extension of the gate electrode leads to a significant increase of the gate-drain capacitance C_{GD} (hence also Q_{GD} and Q_G) and a nonlinear dependence on the drain voltage. This causes a sharp drop in the transfer capacitance as soon as the mesa region completely depletes.
These disadvantages were soon overcome by the use of a separated field plate, which was isolated from the gate electrode and instead electrically connected to the source potential (Fig. 1d). While the charge compensation principle operates as before, the buried field plate does not introduce any additional contributions to the gate-drain capacitance. Instead, the field plate shields the gate electrode from the drain potential, which reduces the gate-drain capacitance C_{GD} and related charges.
These devices, at the time of their introduction to the market, showed best-in-class performance with low gate charge and gate-drain charge characteristics, high switching speeds and good avalanche ruggedness [3]. While the presence of the field plate comes with the disadvantage of an increased output capacitance C_{OSS} and output charge Q_{OSS} (a consequence of the lateral charge-compensation), a careful device optimization enabled field plate-based power technologies with $FOM_{OSS} = R_{DS(on)} \times Q_{OSS}$ comparable to those of the standard trench MOSFET [12,13].

THE NEW MOSFET TECHNOLOGY.

Novel Cell Concept

New MOSFET devices are required to provide improvements across all figures of merit, as this is needed to enable high-frequency SMPS operation where losses are associated both with charges (switching) and on-state resistance (conduction). To meet these requirements, a novel cell-design approach was developed, which explores a true three-dimensional charge compensation.
State-of-the-art MOSFET technologies currently use an insulated deep field plate underneath and separated from the gate electrode. The gate electrodes employ a stripe

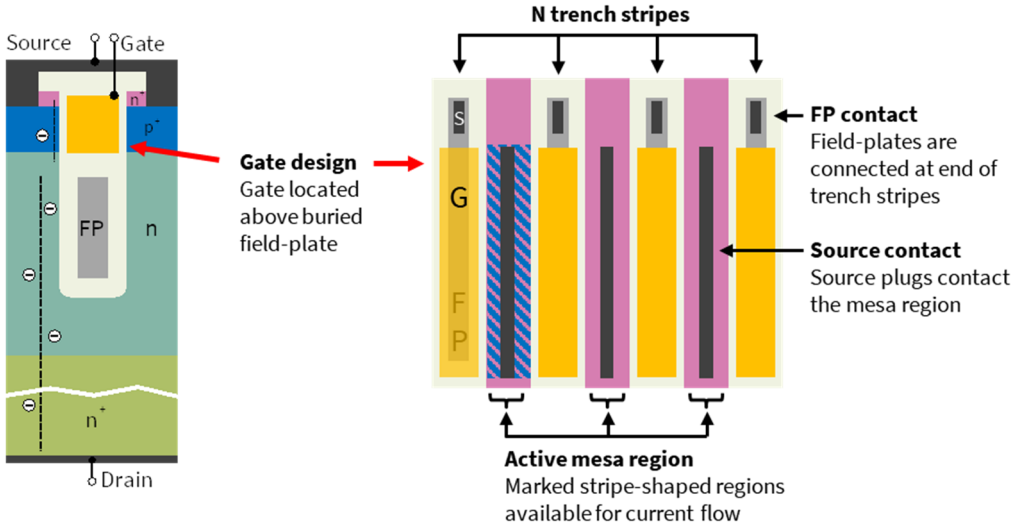

Fig. 2: Typical Trench MOSFET structure with lateral charge-compensation by an insulated field-plate connected to source (left) and commonly employed stripe layout approach in the chip design (right)

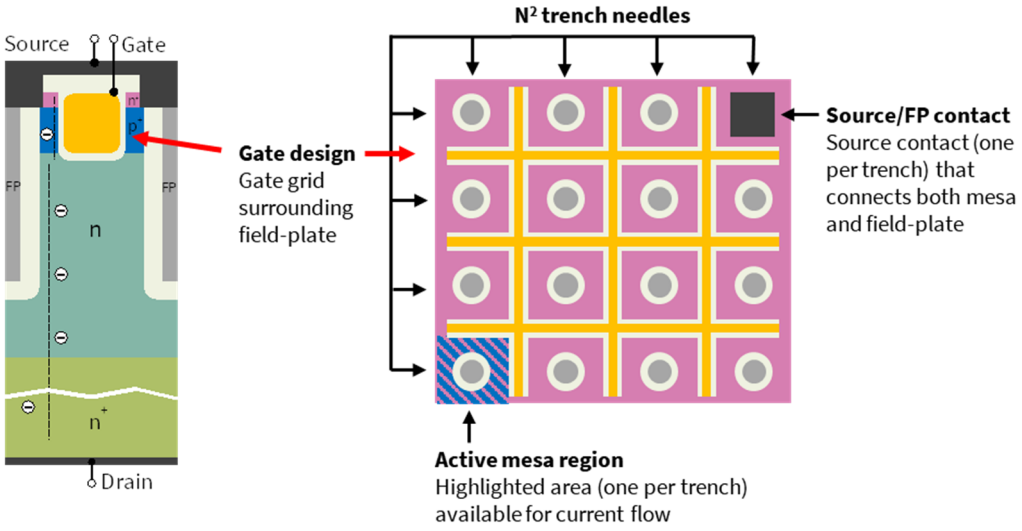

Fig. 3: Trench MOSFET structure with lateral charge-compensation by an insulated field-plate and separated gate trench (left) and the new grid-like layout approach in the improved chip design (right)

layout as depicted in Fig. 2. The new generation separates the field plate trench, which is now formed with a needle-like structure, from a grid like gate trench which surrounds the needles [14]. Fig. 3 depicts this changed layout and schematic cell cross section. This increases the silicon area available for current conduction, allowing for a further reduction in the overall on-resistance [14]. In order to further reduce the $FOM_G = R_{DS(on)} \times Q_G$ and $FOM_{GD} = R_{DS(on)} \times Q_{GD}$ values, the gate trench underwent a complete redesign to minimize its lateral extension. Fig. 4 summarizes the gained improvements in device parameters on product level.

However, the substantially shrunk dimensions of the gate impose a new challenge. The use of common polysilicon as gate material would result in unacceptably large internal gate resistances. Large values for the internal distributed gate resistance lead to a slowed-down switching behaviour, increased switching losses and inhomogeneous switching across the chip which may reduce device ruggedness, hence it is mandatory to avoid such an increase.

The introduction of gate fingers represents a common solution to reduce the chip's internal gate resistance. The disadvantage of this measure is a reduction of the available active area due to the space consumed, linked to an increase of the products on-resistance especially for smaller die and the use of several gate fingers. Fig. 5 illustrates this correlation between gate resistance and active area loss for a best-in-class chip in a PQFN 3.3 x 3.3 mm² package.

To avoid this loss in active area, a metal gate system was developed [14]. This not only eliminates the need for gate fingers, but also improves the gate resistance uniformity across the chip.

Improvements in device switching behaviour

Simulation approach. The new device concept offers substantial benefits in switching performance, providing reductions in the switching losses under both hard and soft switching conditions. The metal gate in combination with the use of a gate grid layout, together with a direct connection of the field-plates to the source metal, realizes a device set-up that ensures a very fast and homogeneous transition at turn-on and turn-off. This not only minimizes switching losses, but also reduces the risk of an unwanted dv/dt induced parasitic turn-on of the MOSFET. To enable an understanding of the differences

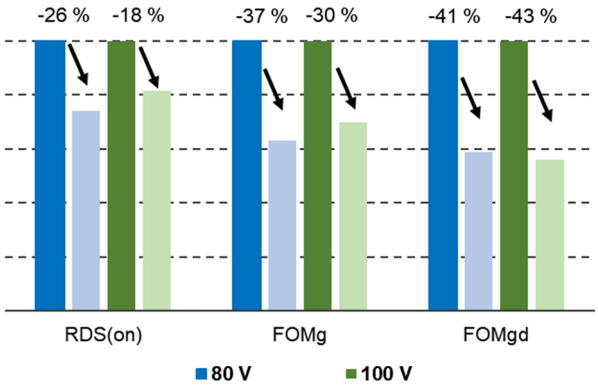

Fig. 4: Improvement of device parameters for best-in-class devices in the PQFN 5x6 package

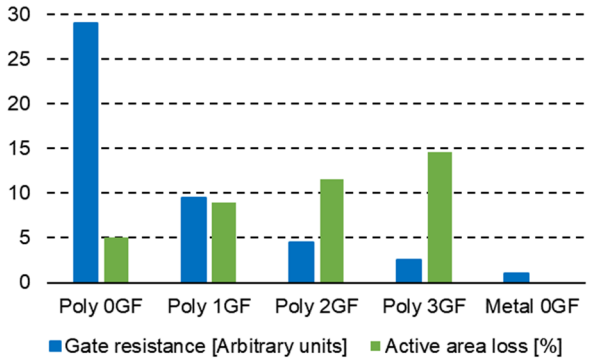

Fig. 5: Reduction of gate resistance with the number of gate fingers (GF) and lost active area loss [14]

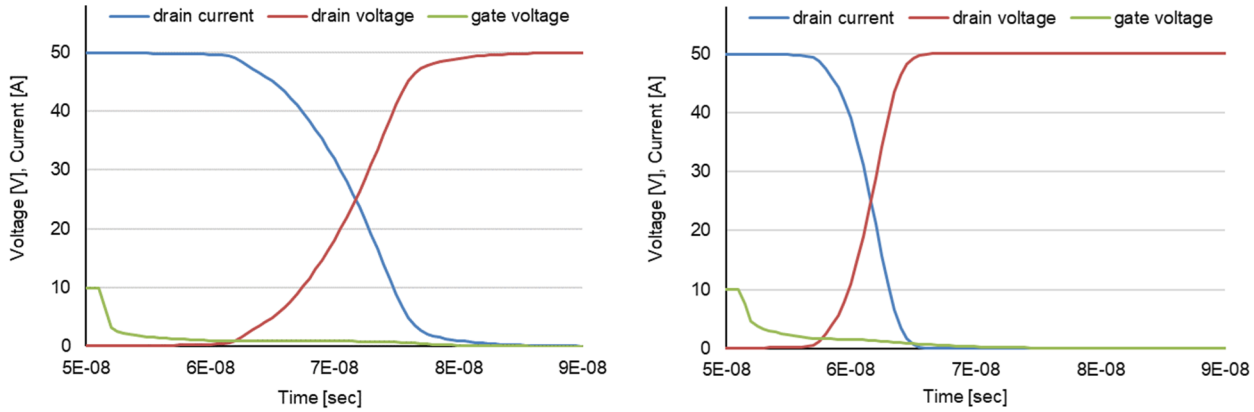

Fig. 6: Comparison of the simulated turn-off characteristics of the previous (left) and new (right) device technologies

in the switching behavior between a traditional stripe layout and the grid layout approach used in the new technology, the potential distribution during the switching of the device is studied based on circuit simulations representing the chip. This approach uses a distributed SPICE model of the transistor and connects 25 x 30 transistor elements within a grid network, which extends across the chip in both directions. The connections between local gate, source and field-plates are modelled by resistive elements.

The values of the resistors represent the material properties of the material used and the geometric dimensions of the respective electrode or layer. The transistor cells, which are located on the crossing points of the resistor network, scale with the fraction of the chip area that results from the chosen number of elements in the grid. Other functional elements, like the gate-pad or gate and source runners, are added to the circuit as necessary for a more precise description of the chip.

Simulation results. A transient simulation of the distributed SPICE model now allows a realistic study of the chip behavior. In contrast to the case of simple RC networks, this approach includes full device models for active cells. As such, this approach correctly considers the voltage-dependence of capacitances as well as feedback effects due to the miller capacitance, and yields the local signal propagation over the chip. Fig. 6 shows the simulated turn-off waveforms for the two approaches, assuming for both cases a chip size of 12 mm². The characteristics show that the new technology with the grid-like gate layout enables a shorter delay time, and clearly switches faster. It only needs approximately half the time of the previous generation.

Figs. 7 & 8 give the simulated distribution of the gate and field-plate potential across the chip for the predecessor technology with a common stripe layout, and for the new technology with a grid-like layout, at several points in time with reference to the waveforms shown in Fig. 6.

In the case of the stripe design, the gate potential over the chip clearly reveals inhomogeneous distributions during the first half of the turn-off process. The gate potential is highest in the middle of the chip where the distance to the gate runners at the upper and lower side of the chip is largest. During the second half of the turn-off process, it is the field-plate potential distribution that becomes strongly inhomogeneous, with the highest potential at the upper and lower sides of the chip where the distance to the source runner in the middle of the chip is biggest.

Due to the combination of a metal gate with the gate grid layout, the new device shows a clearly improved homogeneity of the gate potential across the chip, supporting faster switching of the chip. The strongly improved homogeneity of the gate potential is also advantageous for device robustness, for example avalanche ruggedness, by reducing the probability that a part of the chip is affected by gate signal delays [15] or parasitic turn-on. In former transistor generations, both gate signal delay and parasitic turn-on degrade the device ruggedness as power dissipation is limited to just a part of the chip.

The distribution of the field-plate potential across the chip is actually completely flat for the new device approach. This supports fast transitions and is beneficial for achieving a high avalanche ruggedness, as an increased local field-plate potential may alter the local breakdown voltage [16] and can lead to an inhomogeneous power dissipation over the chip area. The direct connection between the source and field-plate also minimizes resistive losses while charging and discharging the output capacitance.

IMPACT ON CONVERTER EFFICIENCY

The Intermediate Bus Converter

The Intermediate-Bus Converter (IBC) is the only isolated converter in the intermediate-bus architecture (IBA) of a typical telecom power supply, as depicted in Fig. 9. The IBC operates as a pre-scaling converter followed by point-of-load (POL) step-down converters. This architecture is popular in telecom and server applications, where DSP chips and microcontrollers which operate at very low voltages (1.2 V … 5 V) are powered locally by the POL converters, yielding a more efficient system [17].

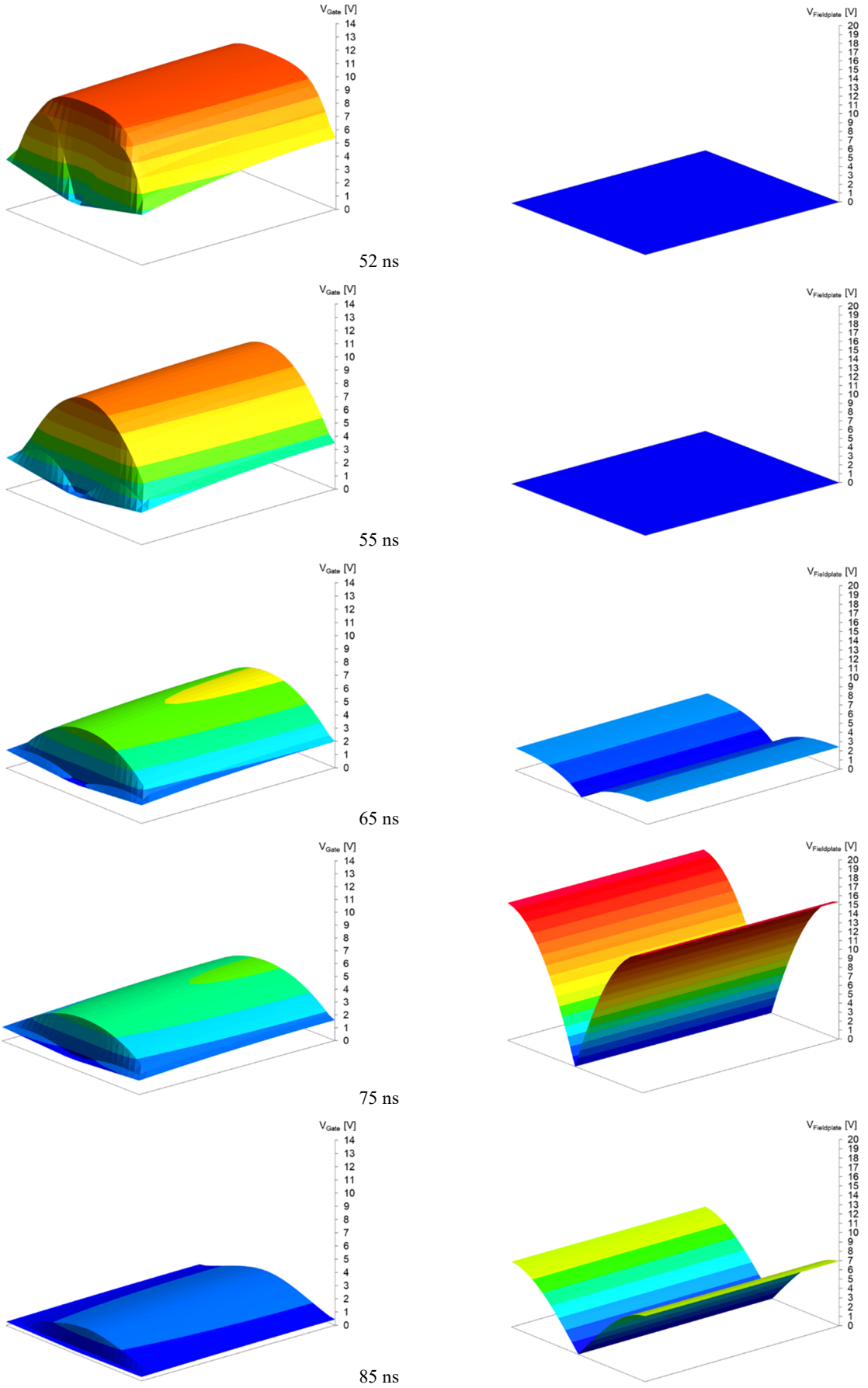

Fig. 7: Distribution of gate (left) and field-plate (right) potential at different points in time for the previous device technology with a stripe layout

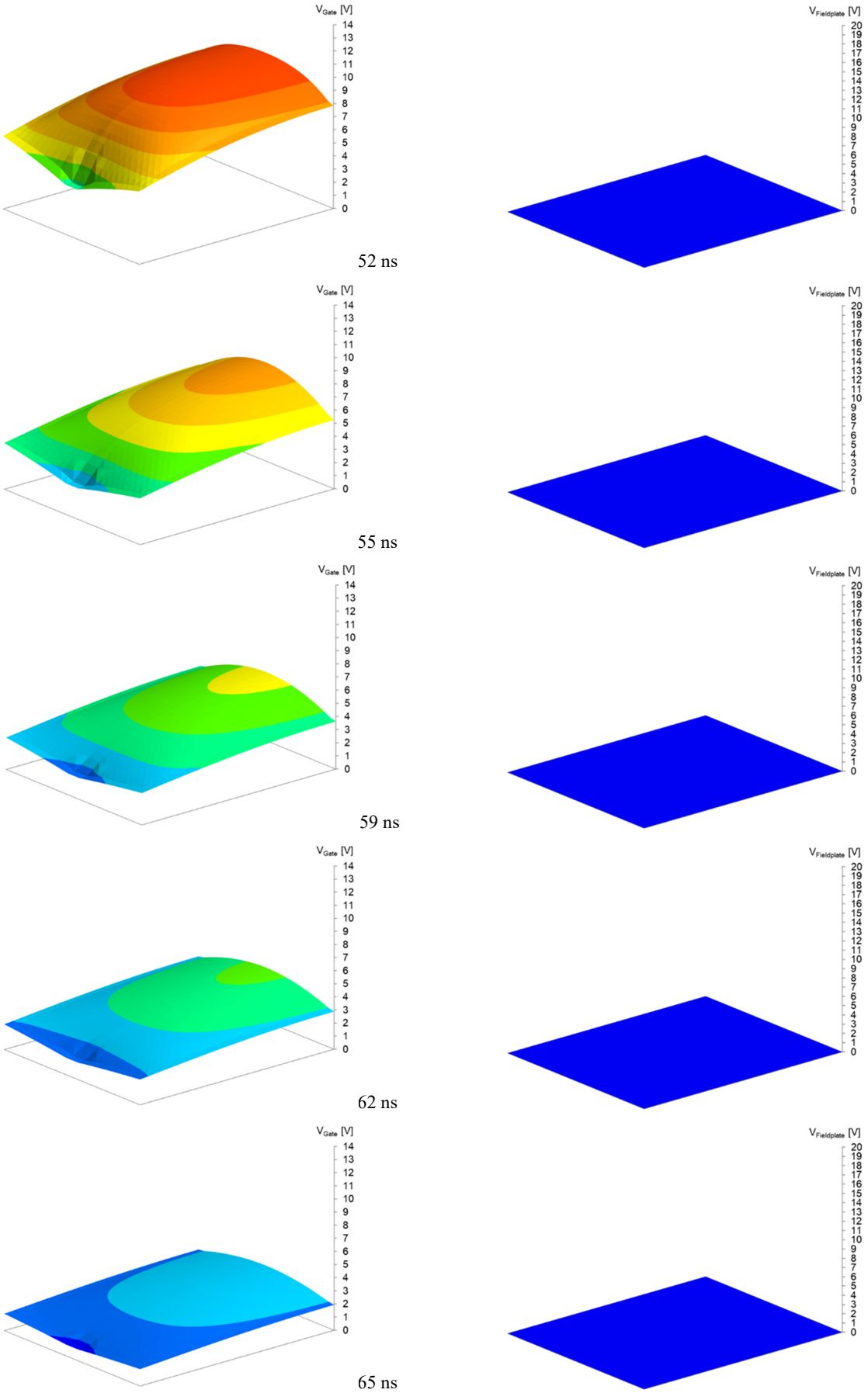

Fig. 8: Distribution of gate (left) and field-plate (right) potential at different points in time for the new device technology with a grid-like layout

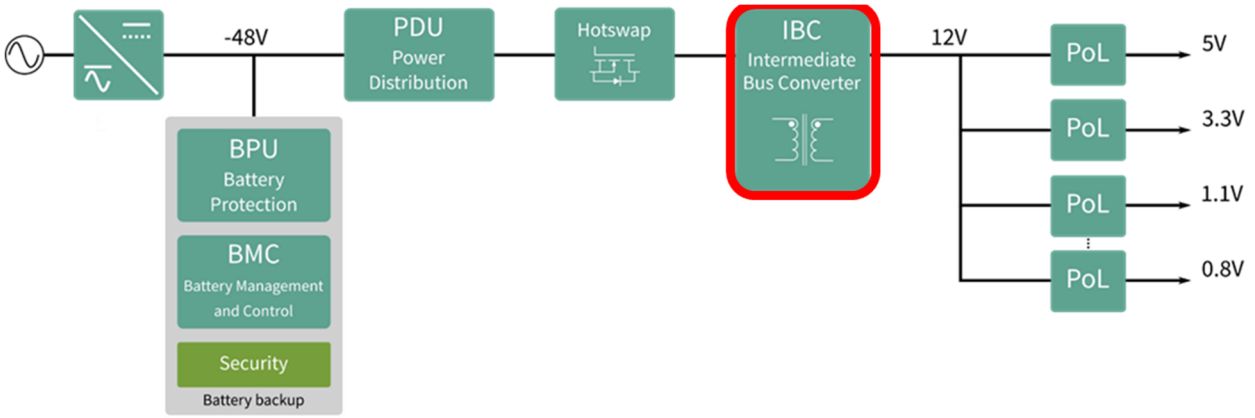

Fig. 9: Simplified schematic representation of a typical telecom power system based on the Intermediate Bus Architecture (IBA)

There are two cascaded converters between the front-end power supply and the IBA load: the IBC and the POL converters. The IBA system must operate with high efficiency, and this requires the IBC converter to have an extremely high efficiency. For common 48 V telecom and datacom systems, the front-end power-supply voltage ranges from -40.5 V to -57 V [18].
To realize the IBC, one can in principle choose from different topologies, which can be either hard switching or resonant.

600 W IBC board for telecom applications

In this work, the efficiency of the devices is studied in a DC/DC converter as typically used in telecom and datacom power systems. The converter uses a hard-switching full-bridge (FB) topology on the primary side, and a centre-tapped (CT) synchronous rectifier (SR) on the secondary side. Fig. 10 illustrates the basic converter schematic.
Thanks to the continuous improvement in MOSFET technologies leading to a stunning power density increase, the IBC in a standard quarter-brick form factor can deliver 600 W. The board operates with a switching frequency of 250 kHz, and the operating input voltage is allowed to vary between 36 V and 75 V. The turns ratio of the transformer is 3:1. Fig. 11 shows the top and bottom of the realized test board. The primary side devices on the board are marked by the red rectangle while the secondary side devices are indicated by the blue rectangle.
Now that the new devices in the 80 V voltage class are available, it is possible to study the efficiency using MOSFETs with an optimal voltage rating.
For this comparison, the primary side employs 100 V devices BSC035N10NS5 with 3.5 mΩ of the previous technology OptiMOS 5 ™, or ISC030N10NM6 3.0 mΩ in case of the new technology OptiMOS 6 ™. Both devices come in PQFN 5 x 6 mm² packages.
The secondary side is equipped with 80 V MOSFETs, either four paralleled devices BSC040N08NS5 with 4.0 mΩ of the established technology OptiMOS 5 ™, or four paralleled devices ISZ053N08NM6 with 5.3 mΩ of the new technology OptiMOS 6 ™. While the OptiMOS 5 ™ devices come in a PQFN 5 x 6 mm² package, the new technology enables the use of the smaller PQFN 3.3 x 3.3 mm² package.

Test results

Fig. 12 is a comparison of the measured efficiencies for both technology generations. The solution using the new generation of devices yields an impressive efficiency improvement of 0.35 % at full load, and an even more remarkable increase of 0.75 % at 20 % load in comparison with the previous generation.
The maximum temperature at the hotspot of the converter on the primary side reduces by 9°C (Fig. 13). On the

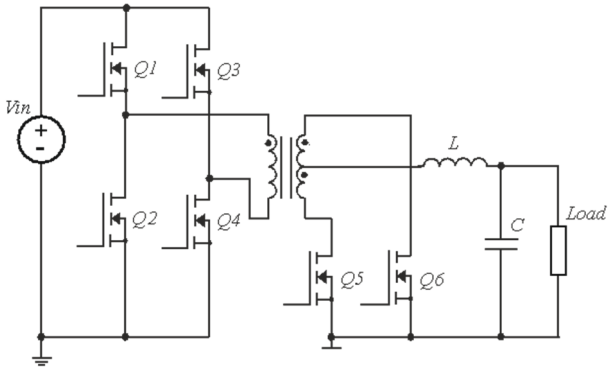

Fig. 10: Basic schematic of the 600 W isolated DC/DC IBC test board in FB-CT configuration

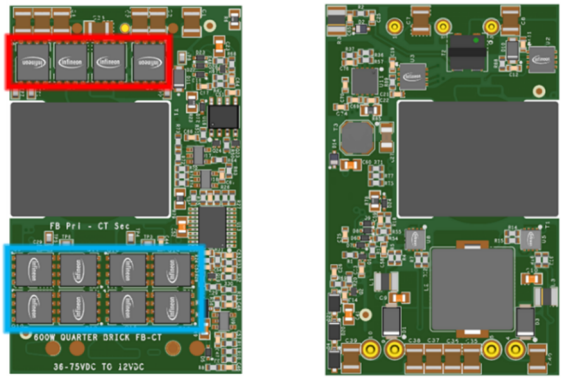

Fig. 11: Top and bottom view of the 600 W IBC test board, red: primary side MOSFET, blue: secondary side MOSFET

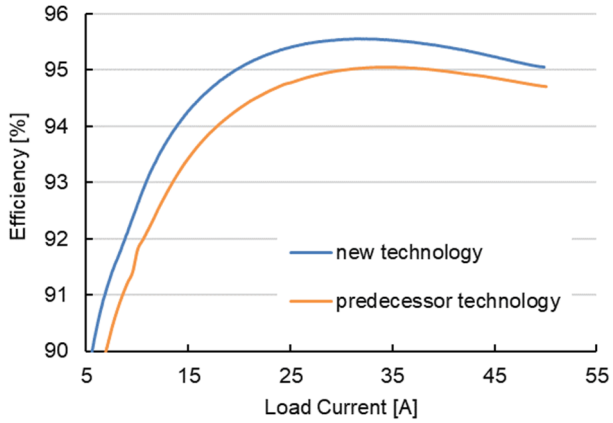

Fig. 12: Overall efficiency of the 600 W IBC comparing the previous and new technology generations

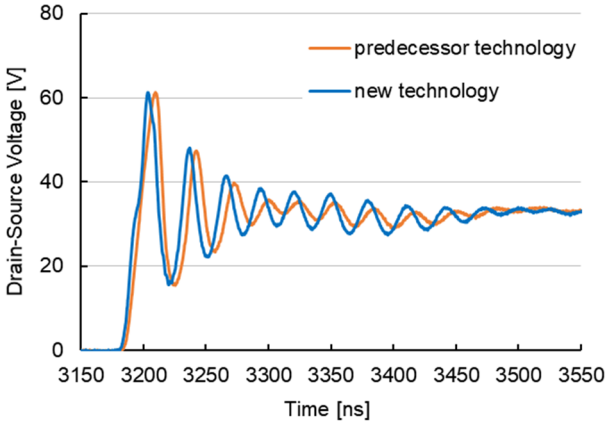

Fig. 15: Comparison of the drain-source-voltage waveforms of the secondary-side SR MOSFET (V_{IN} = 48 V, I_{LOAD} = 12.5 A)

secondary side, despite the use of smaller devices with a clearly reduced footprint, the temperature still reduces by 2°C (Fig. 14).

This remarkable increase in the converter efficiency results from the lower gate charge Q_G and gate-drain charge Q_{GD} of the latest technology devices, and further benefits from a lowered reverse-recovery charge Q_{RR}.

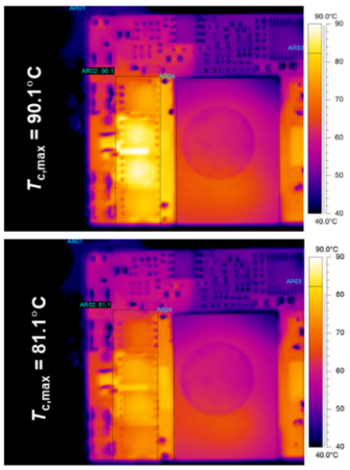

Fig. 13: Maximum temperature for using the predecessor (top) and new 100 V technology (bottom) on the primary side

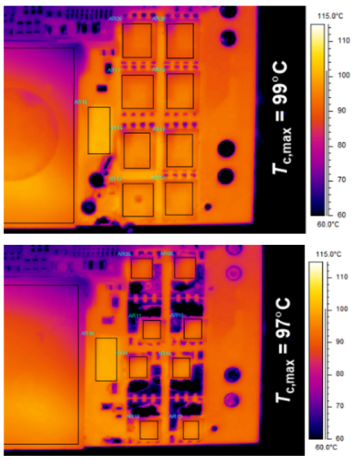

Fig. 14: Maximum temperature for using the predecessor (top) and new 80 V technology (bottom) on the secondary side

Fig. 15 compares the waveforms of both technologies measured across the SR MOSFET on the secondary side at 20 % load.

CONCLUSION

This work introduces the 100 V and 80 V voltage classes of our latest power MOSFET technology family OptiMOS 6™. This new technology realizes improvements in all important device parameters and combines the benefits of low on-state resistance with superior switching performance. The new technology is specifically optimized for high switching frequency applications such as telecom and datacom SMPS.

The remarkable progress in the overall device performance is enabled by substantial improvements at the device technology level. This has culminated in a unique device structure, which is the first to employ three-dimensional charge compensation combined with the first ever use of a metal gate in a trench power MOSFET. As explained by means of circuit simulations reflecting the chip layout, the new design provides a so-far unmatched homogeneity of the dynamic potential distributions across the chip.

The reduction achieved in the on-resistance, the dramatically lowered gate and gate-drain charges, the low output charge and the improved switching homogeneity across the device area promises to enhance the system efficiency across all load conditions. The new device structure is also beneficial for the behaviour of the internal body diode of the MOSFET. Because the silicon area conducting the current is increased, the body diode current density is decreased which, for the same current level, translates into a decreased reverse recovery charge. Efficiency measurements in a 600 W intermediate bus converter board for telecom applications confirm the findings at the semiconductor device level. The efficiency improves by up to 0.75 %, depending on the load condition.

The much better device performance further enables the use of smaller footprints, without having a negative

impact on the temperature of the devices. Overall, these improvements offer significant efficiency gains in the demanding telecom power arena as well as in other application fields.

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Charge Balance Effects on UIS Performance of Trench MOSFETs

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Abstract

The Unclamped Inductive Switching (UIS) test is a widely used technique for evaluating the robustness of power MOSFETs under avalanche conditions. The aim of this paper is to optimize the charge balance condition for active and termination cells for optimal UIS performance, characterized by a higher and tighter avalanche current (I_{av} or I_{pk}) distribution across the wafer, resulting in a minimum loss in UIS yield during production. The paper investigates the design layout of active and edge termination cells to ensure that avalanche failures occur in the active cell area rather than in the edge termination cell area, which has a weaker UIS capability.

Approach

The shielded-gate trench FET is a charge balanced structure (Fig. 1) that requires a delicate balance of charge across the die layout (Fig. 2), that includes active cells, transition from active to termination cells, and the edge termination cells to achieve the best tradeoff between breakdown voltage, BV, and on-resistance, $R_{DS(ON)}$.

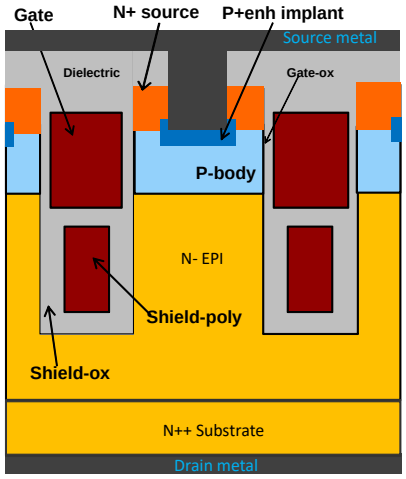

Fig. 1 Shielded-gate Trench MOSFET.

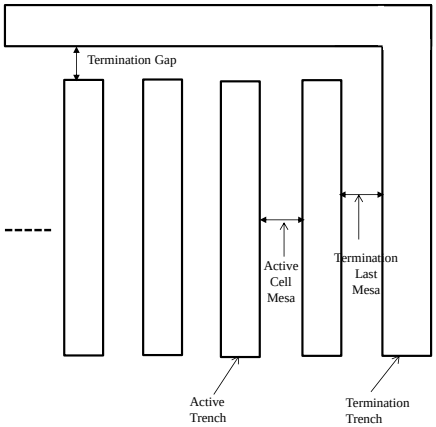

Fig. 2 Power MOSFET top view layout.

While a balanced charge across the die has the best tradeoff in terms of higher breakdown voltage and lower on-resistance, it unfortunately comes with the penalty of poor UIS performance [1]. The UIS robustness or the die's ability to handle the higher UIS energy depends on which portion of the die breaks down first and whether that specific portion of the die can withstand the high current and voltage during the avalanche time. If the termination edge cells or the transition cells break down earlier or at a lower voltage than active cells, peak current, I_{pk} or the UIS energy will be lower as termination or transition cells usually have smaller area than active area with little or no body contacts to absorb all the UIS energy. The purpose of a robust design is to make sure that breakdown occurs at the active cell region, which is loaded with source/body contacts to absorb all the currents during an UIS event.

It is also crucial that both active and edge termination cells have a good breakdown voltage margin before the BV falls off the cliff on the charge balance curve (Fig. 3) and fails to meet the minimum BV requirement. In most cases, the breakdown voltage of active and termination cells is designed to stay on the left-hand side of the charge balance curve (under-charge region, labeled in Fig. 3) with active cells having a lower BV (Point-A) than the termination or transition cells BV (Point-B). It is not desirable to design the active and termination cells' breakdown voltage on the other side of the charge balance curve (Point-C, over-charge region, labeled in Fig. 3) as the BV and UIS robustness become more sensitive to process variation or prolonged field use.

Experimental results have shown that a small amount of charge imbalance between active cell and termination edge cell can lead to higher and tighter avalanche current (I_{av} or I_{pk}). Hence, the active cells are deliberately designed more under-charged than the edge termination cells (termination last mesa and termination gap cells) by making the active cell mesa narrower than the edge termination cells. In other words, the active cell mesa has a lower charge (Q=width*doping conc) than the termination last mesa charge and the termination gap charge, pushing the termination last mesa and the termination gap BV (Point-B in Fig. 3) higher than the active cell BV (Point-A in Fig. 3).

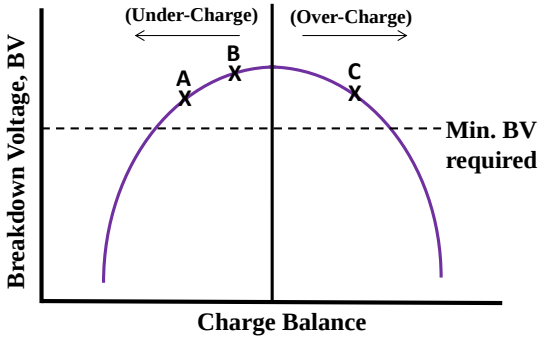

Fig.3 Charge balance curve.

Results and Significance

Figs. 4a, 4b, and 4c illustrate the distribution of peak or maximum avalanche current with respect to design, trench depth, and PHV body dose for a 60V product.

Fig. 4a shows that a higher I_{pk} and tighter distribution is achieved when the termination last mesa is wider than the active mesa. This results in the lowest UIS related yield loss across trench depth and PHV body dose variations.

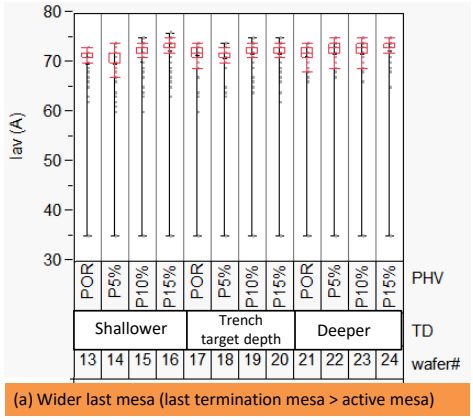

Fig. 4a Peak avalanche current (Ipk or Iav) distribution – last mesa wider than active mesa.

Fig. 4b shows that a lower and widely distributed I_{pk} is observed when the width of the termination last mesa is narrower than the active mesa, leading to significant UIS yield loss. A deeper trench improves the I_{pk} value, but the distribution is still significantly wider for manufacturing.

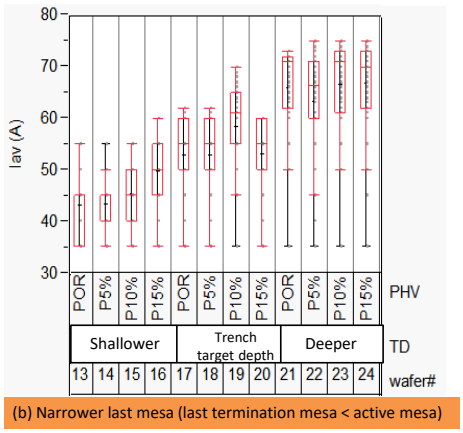

Fig. 4b Peak avalanche current (Ipk or Iav) distribution – last mesa narrower than active mesa.

Fig 4c shows that the I_{pk} distribution is better than that in condition (4b) with equal active and termination last mesa widths, but the I_{pk} distribution is still not as good as that in condition (4a) when last mesa is wider than the active mesa.

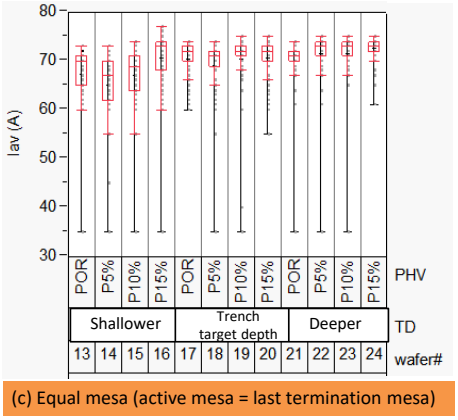

Fig. 4c Peak avalanche current (Ipk or Iav) distribution – last mesa equal to active mesa.

Trench depth and PHV dose has little or no impact on UIS distribution based on Figs. 4a-4c, hence, trench depth and PHV conditions are chosen for the best tradeoffs for BV, threshold voltage, and on-resistance.

Fig. 5 shows the BV_{DSS} distribution with respect to trench depth, PHV body dose, and mesa variations. Narrower mesa and the shallower trench have lower BV_{DSS} comparatively.

Fig. 6 illustrates the TCAD impact ionization rates [2] for three different mesa conditions – impact ionization rates move from the last mesa towards the active cells, as the last termination mesa width moves from narrower mesa width to equal mesa width, and then to wider mesa width. This TCAD impact ionization study validates the experimental findings that the wider last mesa shifts the impact ionization rates from the termination cells towards the active cell region, resulting in improved UIS performance.

Fig. 7 shows the typical burnt marks after UIS failure. For the case with a wider termination last mesa, the failure burnt marks are in the active cell area as desired. And, for the case with a narrower termination last mesa, the failure burnt marks are always at the die edge or at termination last mesa, which is not desired.

Conclusions

The paper presents that a small amount of charge imbalance between active cell and termination cell can lead to higher and tighter UIS energy capability. This charge imbalance is achieved by designing the last termination mesa wider than the active cell mesa in the die layout, considering a specific doping condition. The experimental findings are further validated by a TCAD study.

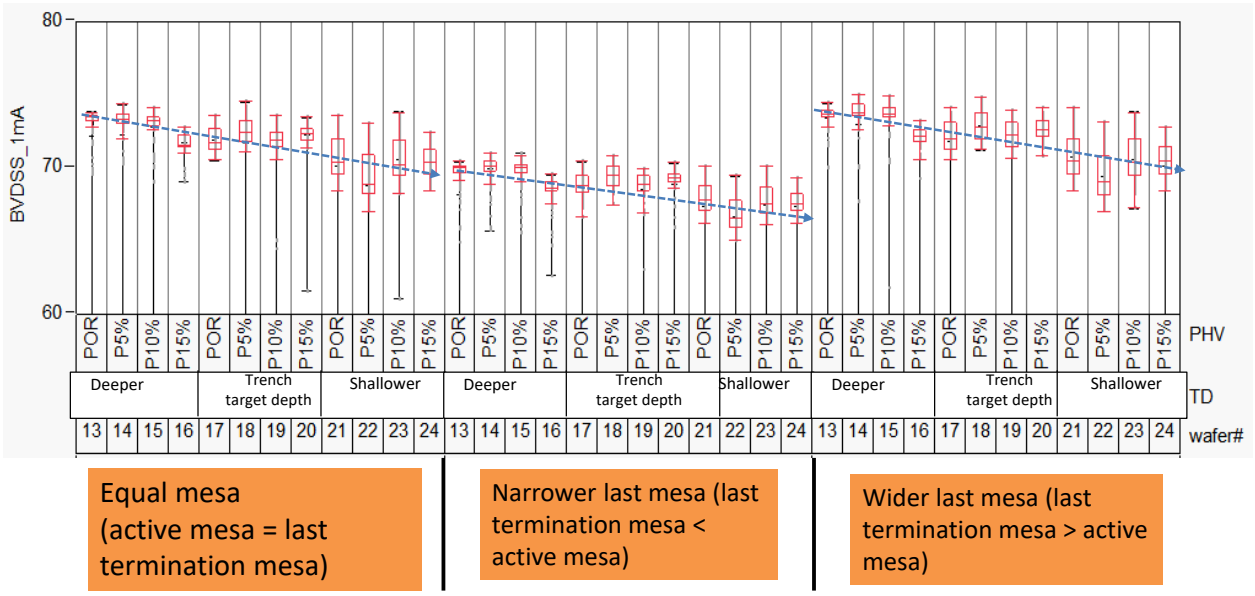

Fig. 5 BVdss with trench depth and body PHV dose variations for equal mesa, narrower mesa, and wider last mesa designs.

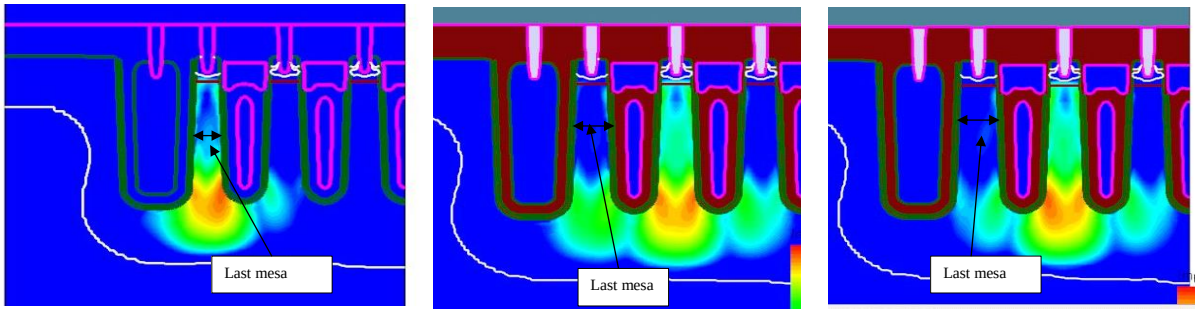

Fig. 6 Impact Ionization rates at breakdown. Left: narrower last mesa; Center: equal active and termination mesa; Right: wider last mesa.

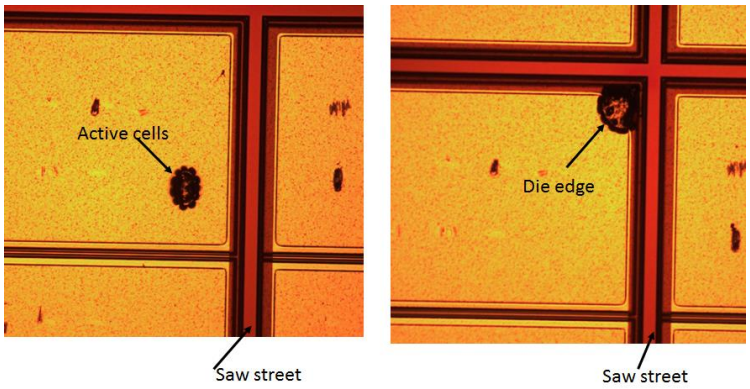

Fig. 7 Burnt marks after UIS failures; Left: wider termination last mesa, usually seen in the active cell area (preferred case); Right: narrower termination last mesa, usually seen in the die edge corner (worst case).

ACKNOWLEDGMENT

The authors would like to thank process integration team for wafer process and design of experiments.

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[1] Insulated gate semiconductor device having trench termination structure and method – Patent Application No. 16/134,598.
[2] Sentaurus TCAD Process/Device Simulation Tools – SPROCESS, SDEVICE.

Press Pack IGBTs for MVDC-breaker Applications

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Abstract

With the rising demand for higher power densities and robust system control, the need for using press pack IGBT (PPI) devices in medium voltage (MV) applications is also increasing. So far PPI manufacturers have majorly focused on devices with paralleling of IGBTs/diodes inside a single housing, that drives thousands of Amperes and is used for high-power switching in various converter applications, like High Voltage Direct Current (HVDC), Flexible Alternating Current Transmission Systems (FACTS), and MV drives.

However, the absolute capabilities of a single chip are yet to be intensively explored for applications that do not require fast turn off, standard ±15 V gate voltage, and continuous switching, such as MV-DC-breaker.

The idea of this work is to investigate the boundaries and robustness of a single chip at higher gate voltage for all possible conditions and eventually realize an application out of it. The major focus of the work is on determining the maximum potential of the 4.5 kV trench IGBT chip at a gate voltage as high as 40 V. After performing several robustness and stability tests, it can be claimed that a single chip can turn off at least 12 times the nominal current after conducting about 10 milliseconds, a requirement which is very important for the DC hybrid circuit breaker.

Keywords: Press pack IGBT, Circuit breaker, MVDC, Surge current, High gate voltage applications

I. INTRODUCTION

As the demand for energy is rising around the world the way of transportation is also being reviewed. HVDC has been an alternative method of transmitting electric power from one location to another with some inherent advantages over AC transmission systems, such as lower losses and decoupling of networks for different frequencies or phase shift. The efficiency and rated power carrying capacity of direct current transmission lines depend highly on the converter used in transforming the current from one form to another (AC to DC and vice versa). This is the introduction of the voltage source converter to HVDC application and the demand for IGBTs has increased.

A. DC grids and DC breaker

Due to the trend of moving towards DC grids there is an increasing demand for DC circuit breakers, especially in mashed grids. Today's concepts for DC breakers for higher power ratings are mainly based on hybrid solutions, a combination of contactors and semiconductors which can be actively turned off. In Hybrid circuit breaker the load current is carried during normal ON operation by the vacuum interrupt switch (VIS). Only in case of switching, the current, I_{SS}, is taken by a semiconductor for up to 1 ms. Therefore, the function of the semiconductor is to conduct the current for up to 1 ms. and afterwards turn off the I_{SS} current. As semiconductors in a hybrid DC breaker today mainly use IGBTs as discrete devices or for higher power rating IGBT modules.

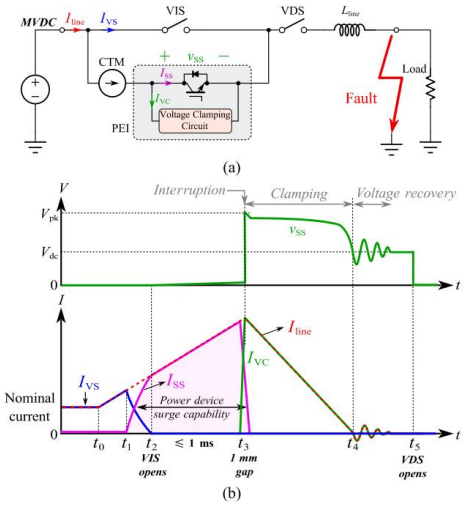


Fig. 1. (a) Hybrid circuit breaker unit with an IGBT-based system using a current transfer module (CTM) to enable current commutation from the VIS to the PEI branch. (b) Typical fault interruption waveforms of the hybrid circuit breaker. [8]

B. **Requirements for IGBTs in high current hybrid circuit breakers**

Today's state of the art IGBT modules are optimized for continuous operation in frequency converters. Therefore, the developments of the last decades are focussed on low losses, low thermal resistance, and high-power cycling capability. Now a new market of IGBTs for circuit breakers is emerging which has different requirements for the semiconductor. The main requirement is to conduct and switch off the highest current in the smallest area. A possible way to increase the maximum I_{SS} current of an IGBT is to increase the gate voltage during the on-state phase.

Due to the fact that the switching of a hybrid circuit breaker does not happen too often, the pulse for the IGBT can mainly be considered as a single pulse event. The power losses that occur during the pulse heat up the silicon and nearby components. For such low pulse operations, therefore, optimized cooling for continuous operation is not necessary. To increase the level of I_{SS} current, double-sided cooling for a short time is beneficial. To get a better understanding of the effect of double-sided cooling, Infineon's bipolar chip stack has been evaluated for the hybrid circuit breaker application.

II. New press pack IGBT

The first product of PPI is a 4.5 kV 3000 A device with 125 mm pole piece diameter. It contains 36 pieces of IGBT chip stacks. The innovative design of chip stack and housing technologies enables the creation of a perfect fitting portfolio with different current values and, in addition, with or without internal freewheeling diodes (FWD) to cover different applications and power ranges.

A. **IGBT chip technologies**

IGBT chip with a trench gate structure is designed to reduce conduction losses with negligible influence on the tail current and turn-off losses. It has been proven as an effective solution to minimize the saturation voltage of the IGBT chip. Another point, field stop technology is used to reduce the thickness of silicon for lower conduction resistance and higher blocking voltage, which also reduces the tail current and lowers the turn-off loss slightly. The IGBTs with trench gate and field stop technology have been in commercial production for many years already [5].

For this new press pack IGBT, the latest innovative 4.5 kV trench IGBT chip technology has been adopted. The same chip technology has been successfully used in the latest IGBT module generation for a long period of time. Only slight mechanical modifications needed to be performed to adapt the chip for use in press pack devices. One of the big improvements of the trench technology is of course the increase in maximum operating temperature from 125°C to 150°C of the IGBT chips. Besides this benefit, the conduction losses of the chips are decidedly reduced a lot compared to IGBT with planar technology. The typical on-state voltage is only 2.16 V under 25°C junction temperature and 2.70 V under 150°C junction temperature as shown in Fig. 2.

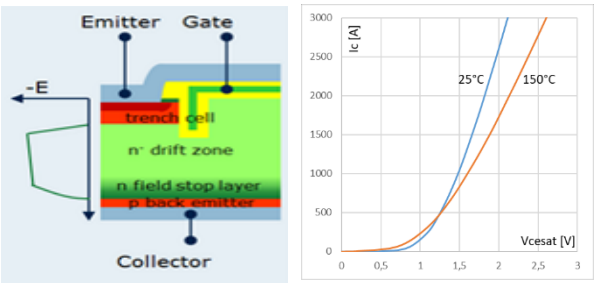


Fig. 2. The diagram of chip design (trench gate and field stop technology) and the typical output characteristic curve (Tj is 25°C and 150°C).

An IGBT, to be used in an Multi Modular Converter circuit, can be optimized for low switching frequency (50 ~ 150 Hz). Due to this and the technology curve of the silicon semiconductor, Vcesat can also be optimized for a low value. This reduces whole converter losses. In addition, reverse bias safe operating area (RBSOA) is enlarged by an optimized chip design that offers better IGBT robustness during turn-off in field applications [6].

B. **Chip stack by low temperature sintering (LTS)**

Due to its excellent conducting properties for heat and electric current, copper is the customary material for connecting high power semiconductors. However, there is a mismatch in thermal expansion between silicon and copper, which can lead to severe stress and ultimately to device failure if copper and silicon are attached directly. This is why, a layer of a better matching metal, usually molybdenum, is used to shield the silicon from the stress generated by the mismatch of thermal expansion. There are several options for joining silicon and molybdenum, such as free-floating, alloying, and sintering.

The free-floating (FF) assembly is the simplest configuration since the molybdenum is just put on both sides of the silicon and the contact is created by outside force. This is easiest to manufacture but increases thermal resistivity compared to other alternatives. Alloying offers better thermal performance but requires a process temperature of around 700°C. This leads to thermal stress inside the device and changes device behavior due to heavy modification on the alloyed surface. Besides this, the high process temperature results in changes inside the silicon, which is not acceptable. Therefore, for optimum device performance and reliability, silver sintering is recommended as the best solution. It is called low-temperature sintering (LTS). Here, a layer of silver is placed between silicon and molybdenum. Under high pressure and moderate temperatures (200 to 300°C) silver sintering creates links between the silicon, molybdenum, and each other, thereby creating a durable connection [7].

After the silicon is attached between two plates of molybdenum as a chip stack, the IGBT chip is well-protected from both thermal and mechanical stress. Due to the LTS process, the electrical data of this chip stack is stable under a wide range of pressures. This makes the semiconductor absolutely robust to check, at that level, static parameters as well as the electric dynamic robustness of the IGBT during turning on and off. The effort of conducting such tests at the chip level or free-floating arrangements is very high and can create a lot of scrap due to mechanical deviations. In addition, the tested electrical values can change a lot if the chip is connected again.

Within static and dynamic parameters, measurements of, for example, VGEth, VCEsat, Eon, Eoff, etc. made with similar parameters are recommended into one group for PPI assembly, which would ensure the static and dynamic current sharing among the IGBTs or diodes in one housing. Each chip stack is marked with an individual QR code on both surfaces to identify, thus a full traceability of chip-stacks is possible.

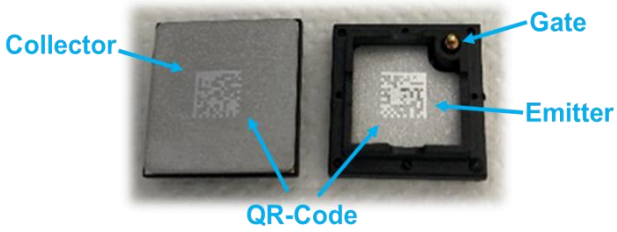


Fig. 3. Chip stack design including a QR code on both sides.

Besides this benefit, the mechanical robustness of the chip stack, comparing with a pure silicon chip, is also improved dramatically. By this, handling in production is gets much easier and many negative influences, e.g., particles, are reduced to zero. In addition, the production is highly automated to reduce variation in processing.

The LTS technology enables the reduction in the number of surface interfaces by 50% compared to free-floating, which decreases the thermal resistance of each chip. This allows a higher power density of the chips and increases the current capability of the PPI. In addition, the risk of surface problems is reduced because of fewer interfaces.

Alongside, the electrical robustness during switching is also increased by using the good connection to molybdenum as a sink for storing heat energy from the IGBT turning on or off.

III. IGBT chip capabilities

A. Surge current/static test

The first challenge for the 4.5 kV, trench IGBT chip having a total area of 246 mm^2 and an active area 144 mm^2, is to withstand a current several factors higher than the nominal current for at least 1 ms. The nominal and continuous current rating of the IGBT is 83 A at a maximum gate voltage of ±20 V. To meet the DC breaker requirements, the IGBT needs to be evaluated at high surge current and go beyond the existing forward bias safe operating area (FBSOA). Damage at surge current can be caused by extreme power dissipation, which is a function of current and the conduction time.

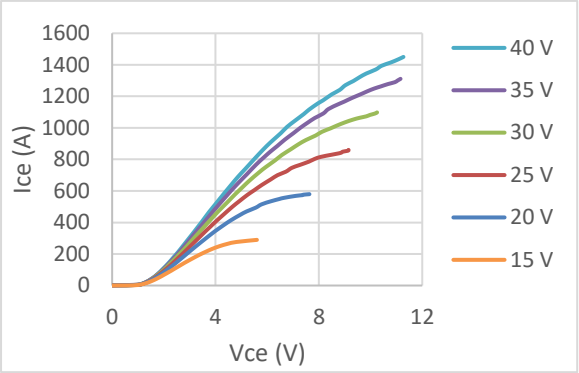


Fig. 4. Ice-Vce with different gate voltages till 40 V Vge

Fig. 4 gives an initial idea on what the chip is capable of at different gate voltages at 25°C without going into desaturation mode. To produce this result, ten samples were taken and tested at increasing gate voltages. Tests were also done at a maximum of 100°C to check the shift of the IGBT output characteristics. However, for the breaker application, 25°C is the standard operating temperature.

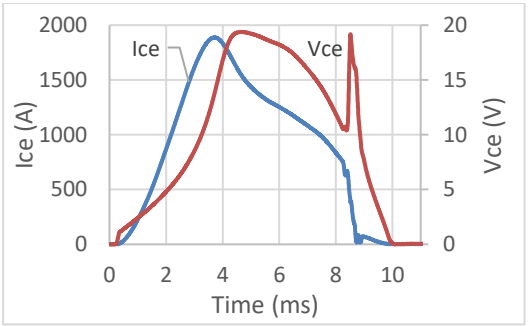
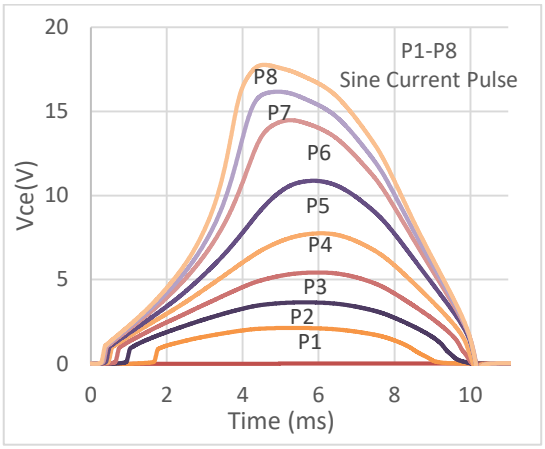


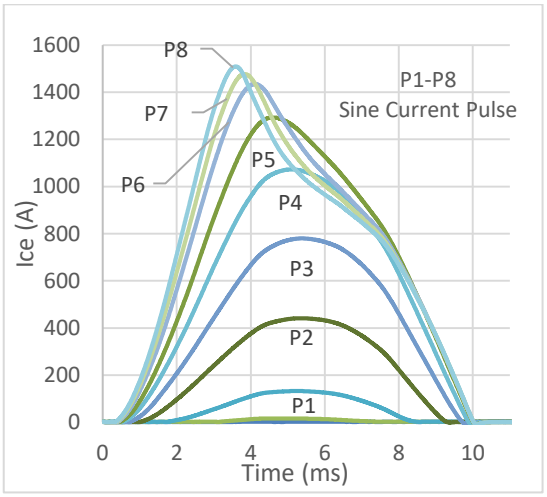
Fig. 5. Current and voltage curve for an IGBT damaged through surge current at 50 V Vge and Tvj = 25°C

The critical electric field for the Gate oxide of this IGBT is measured to be three times the nominal gate voltage, and there has been sufficient test data to statistically get an idea of the critical electric field at the corresponding gate voltage. However, these standard tests were done with a constant voltage in the gate for less than a millisecond and with an open collector emitter terminal. It was, therefore, important to investigate the high V_{ge} behavior when large collector current is flowing for a long period of time, the maximum being 10 ms for this work. For the first evaluation, the gate voltage was set close to the critical value and the first set of trials were done at 50 V with five devices, three of which got damaged, producing a data trend not supporting high currents over 1500 A. Fig. 5 is a current and voltage curve indicating when and where the IGBT got damaged at 50

V and at 25°C. Therefore, after careful consideration, the gate voltages were limited to 40 V, adding some buffer in case of overvoltage transients and to reach a gate voltage value where all samples would experience an electric field well below the absolute limit. For all FBSOA tests, a half sinusoidal wave was applied for 10 ms and the corresponding current and voltage of the chips were measured. It is important to note that for this work, IGBTs with V_{cesat} 2.7 V were measured at 83 A, 15 V Vge, and 150°C.



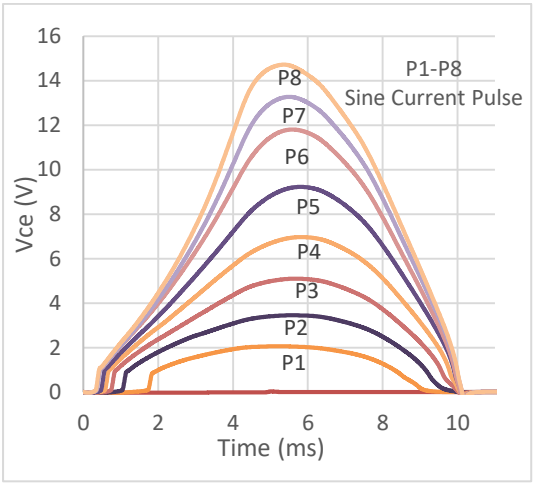
(a)



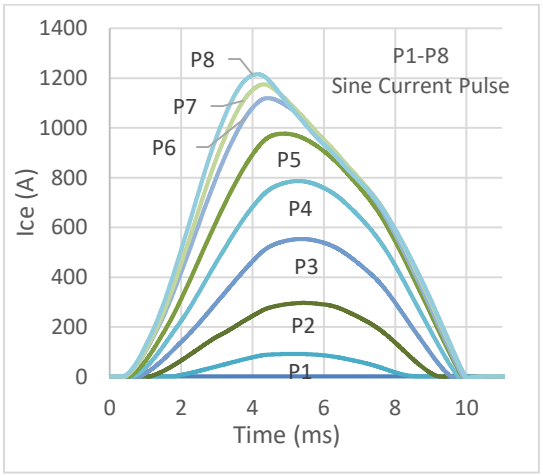
(b)

Fig. 6. Surge current pulse at 25°C, 10 ms and 40 V Vge; (a) Voltage (b) Current

Fig. 6 and 7 show measured surge currents and voltages at 25°C and 100°C respectively at V_{ge}= 40 V and 10 ms after a series of sinusoidal current pulses were applied to the IGBT. As can be seen in both the figures, as the IGBT approaches desaturation, the shape of the current sinusoid starts getting distorted, thereby adding to the power loss. Fig. 8 clearly shows the power dissipation distribution for the maximum current waveform for both temperatures. Because of the higher current capability at 25°C, the total energy reached as high as 94 kJ for a 10 ms pulse duration.



(a)



(b)

Fig. 7. Surge current pulse at 100°C, 10 ms, and 40 V Vge; (a) Voltage (b) Current

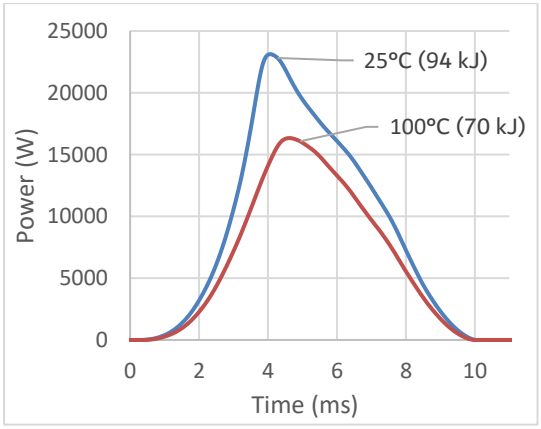


Fig. 8. Power at maximum current and 10 ms; total energy at 25°C = 94 kJ, and total energy at 100°C = 70 kJ

With the knowledge that a single chip can easily survive as high as 94 kJ, more samples were needed to statistically validate the trend. Fig. 9 is the measured data for 30 samples in the same settings with two temperatures. All devices safely reached more than 1300 A.

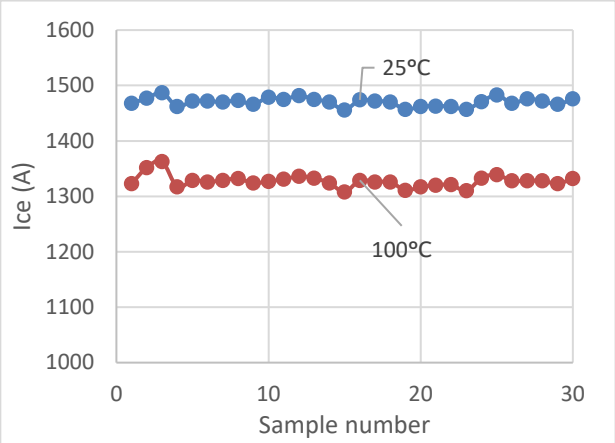


Fig. 9. IGBT surge current sample test with V_{ge} = 40 V

Thus, FBSOA can be claimed to be extended by at least 15 times the continuous rated current at higher gate voltages of up to 40 V.

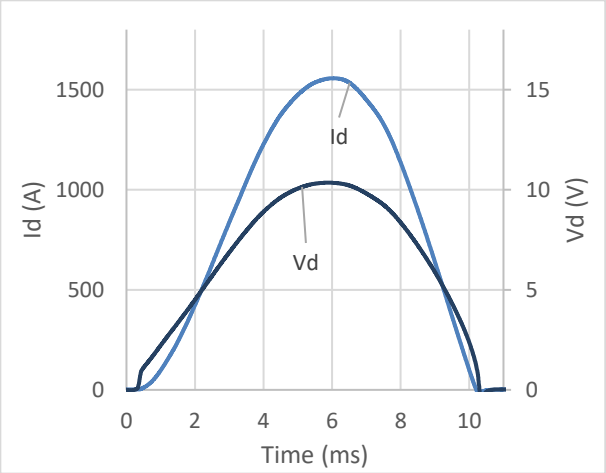


Fig. 10. FW diode surge current pulse for 10 ms at 100°C

Although the focus and scope of this work is limited to IGBTs, every IGBT needs a partner free-wheeling diode. To make the picture complete, the surge current capability of a 4.5 kV emitter-controlled diode is also shown in Fig.10. It shows that for a single chip reaching 1500 A is still under its destruction limit.

B. Long term stability

Like the extended FBSOA, it is also extremely important to test the long-term gate oxide stability for the IGBT at two temperatures. In this work, long term is defined by the number of cycles the chip will be experiencing in its entire lifetime. Generally speaking, for a circuit breaker application the IGBT needs to turn off currents a maximum of 100 to 500 times in its entire lifetime. However, since absolute limits of the device are being investigated, two modes of cycle tests were performed here.

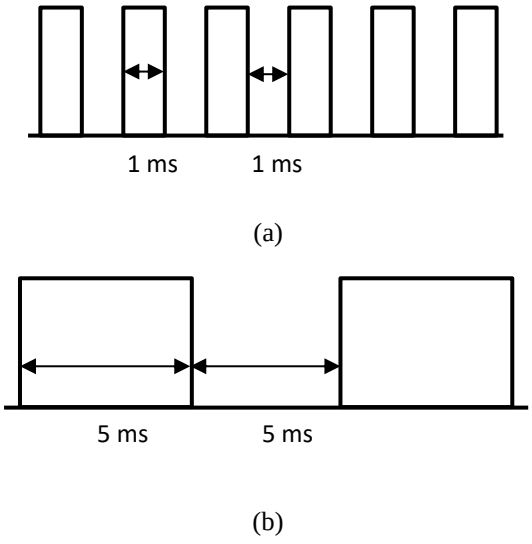


Fig. 11. Gate oxide stability test with 40/-8 V Vge (a) 10000 cycles (b) 25000 cycles

Fig. 11 illustrates the two modes of continuous pulse fed to the IGBT gate oxide. The 1 ms/1 ms pulse was for 25000 cycles and the 5 ms/5 ms was for 10000 cycles. Every time the Vge was changed between 40 V and – 8 V.

	25°C		100°C	
Parameters	**Before**	**After**	**Before**	**After**
V_{br} (V)	5148	5148	5148	5148
I_{ces} (mA)	0.0221	0.021	5.2	4.82
V_{geth} (mV)	6564	6567	5575	5588
V_{cesat}(mV)	2205	2179	2476	2450
t_{doff}(µs) (30 pcs)	10.30	10.16	10.36	10.34
t_{don}(ns) (30 pcs)	449	446	446	446
di/dt (A/µs) (30 pcs)	2843	2805	2765	2682

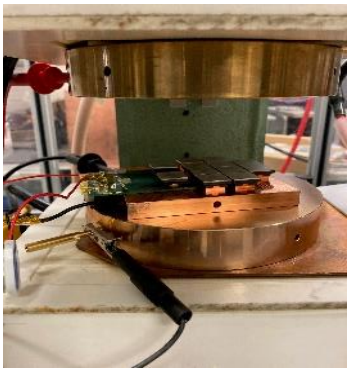
Table 1. Summary of the results before and after the cycle test

Once again, 30 samples were taken for the tests and every time before and after the cycle tests, both static and dynamic parameters were compared. The threshold voltage in the static parameters, has the most impact in case there is any change in the gate oxide. For the dynamic parameter, there can be a change in Miller plateau which is manifested by t_{doff}, t_{don}, and di/dt. However, as can be seen from Table 1, even with two temperatures, after the cycle test, there has been no significant changes in the parameters, thereby concluding that the single chip is able to withstand 40 V/-8 V without

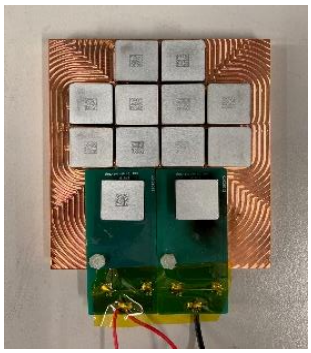
a problem for at least 25000 cycles, both at warm and room temperatures.

C. **Dynamic tests**

This section addresses the most important criteria for establishing the usability and advantages of this IGBT chip for the circuit breaker application. In this part, the IGBT was switched off multiple times. The objective was to determine the maximum turn-off current with absolute safety, which stretches the RBSOA.



(a)

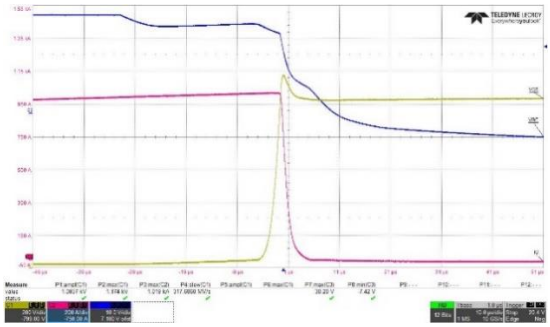


(b)

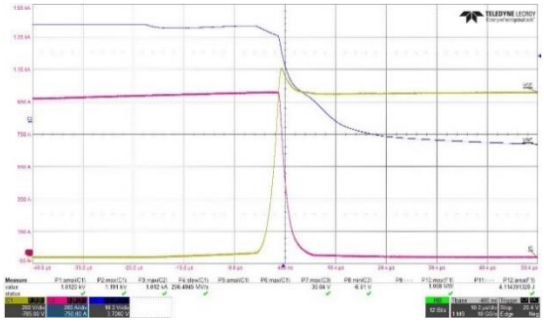
Fig. 12. Dynamic test setup (a) Press system (b) Chip stack system

For the dynamic tests, the chip stacks were pressed in a press system with copper pole pieces built specially for this project. The test circuit used here, was the classic double-pulse test setup with FWD connected anti-parallel to the load inductor.

The tests were conducted at two voltage levels, as can be there in the application as well – 1000 V and 2800 V. As 40 V is the maximum allowable gate voltage coming from the previous tests, additional safety margins were given to turn off with absolute robustness and hence all the tests were done at 30 V and switched off with -8V and a higher R_{goff}. The first trials were done to check with all 30 samples if 1000 A can be turned off at 1000 Vdc and 2800 Vdc at 25°C and 100°C. The following diagrams are the dynamic response of a single chip.

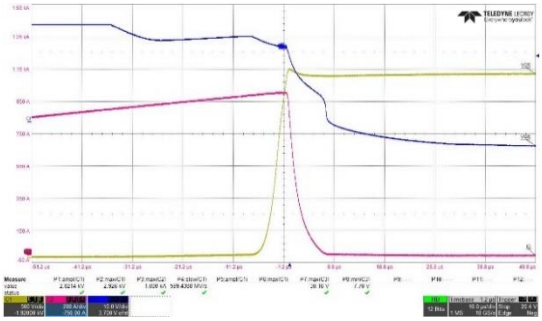


(a)

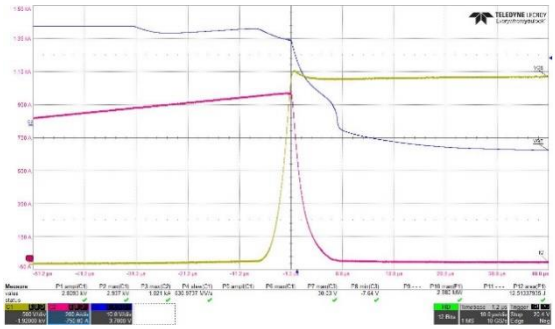


(b)

Fig. 13. Turn off 1000 A, 1000 Vdc (a) 25°C (b) 100°C



(a)



(b)

Fig. 14. Turn off 1000 A, 2800 Vdc (a) 25°C (b) 100°C

As the diagrams depict, turning off at 1000 A for voltages up to 2800 V does not show any robustness issues. In the pursuit of a higher current, keeping 30 V, V_{ge} as constant, it was found that some devices were damaged at about

1250 A (Fig. 15). Therefore, if the safety margin 30 V is fixed and if absolute robustness is required, 1000 A is the maximum current a single chip can be turned off at temperatures up to 100°C.

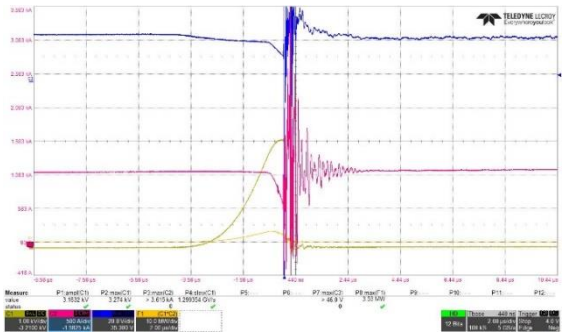


Fig. 15. Damaged IGBT at Turn off 1200 A, 2800 Vdc at 25°C

With this observation and supporting test results, the work concludes that a single 4.5 kV trench IGBT is able to turn off current in the range of 1000 A safely and can be realized for an application like hybrid DC breakers.

IV. Conclusion

The work started with the objective to explore the limits of the press pack 4.5 kV trench IGBT chip outside the standard ±15 V gate voltage range and investigate the surge current turn off capability, which was later exploited to find an application in the DC hybrid circuit breaker. The requirement for the breaker is that the chip needs to conduct a very high current for a maximum period of 1 ms and turn off slowly.

Since the work focused more on the chip level and not on the application, the first part started with exploring and eventually stretching the FBSOA. As can be seen from Fig. 16, the FBSOA was extended to 12 times the nominal current and up to 10 ms, instead of 1 ms, with 94 kJ being the typical energy loss at the conduction phase.

The next part addressed the turn-off of the chip at high currents, thereby stretching the limits of the existing RBSOA. As shown in Fig. 17, it was successfully tested that the chip can safely turn off 12 times the rated current at DC voltages up to 2800 V at 30 V gate voltage.

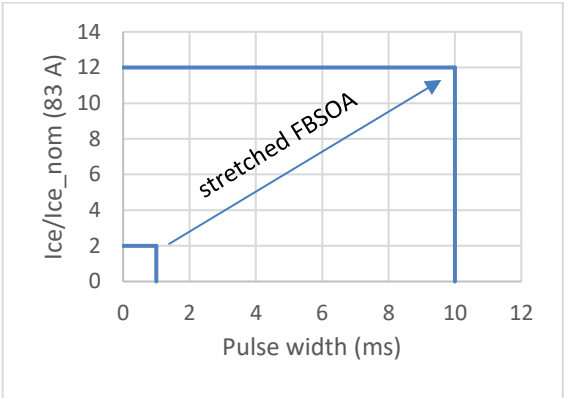


Fig. 16. Revised FBSOA for surge current operations such as hybrid circuit breakers

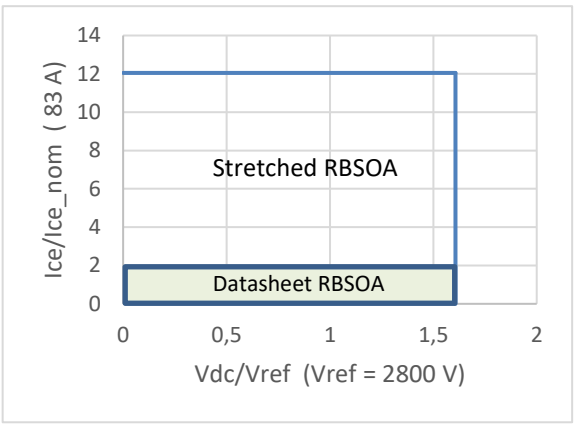


Fig. 17. Revised RBSOA for surge current operations

This work also investigated the long-term stability of the gate oxide by applying cycle tests till 25000 cycles and the oxide was able to retain its property before and after the tests.

The critical gate oxide having started with 50 V, the test parameter, i.e., the final gate voltage was brought down to 30 V in a stepwise manner, to provide a safety margin and better response to transient robustness. The press pack packaging also helps in better power cycling and increased mechanical stability. As of now, the objective has been met and the robustness boundaries have been explored. However, in future, investigations can be done at 40 V gate voltages. It should also be noted that turning off IGBT chips in parallel will add more current breaking capability, something that needs to be tested as an extended version of this work.

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Threshold Voltage Temperature Dependence for a 1.2 kV SiC MOSFET with Non-Linear Gate Stack

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Abstract

The use of Silicon Carbide (SiC) power MOSFETs is becoming increasingly popular due to their unique properties, including a wide bandgap, higher critical electric field, and superior thermal conductivity compared to traditional Silicon (Si) MOSFETs. The reliability assessment of SiC power MOSFETs holds significant importance across various industries, such as automotive and aerospace, where these devices find numerous applications. One crucial aspect of their reliability is evaluating their performance during short-circuit (SC) events. To address this concern, this study employs TCAD simulations to analyze the behaviour of a SiC power MOSFET equipped with a gate insulator that consists of a stack of silicon dioxide (SiO_2) combined with a non-linear dielectric (NLD) material. This NLD exhibits a Curie-Weiss temperature dependence, characteristic of ferroelectric materials. During short-circuit events, failures are often associated with temperature rises. The study demonstrates the effectiveness of using an NLD with a temperature-dependent permittivity (ε) as a gate insulator. By doing so, the temperature increase is mitigated, and the MOSFET's ruggedness during short-circuit events is enhanced. This advancement in gate insulator technology could significantly improve the overall reliability and performance of SiC power MOSFETs in various applications.

Keywords: Silicon Carbide, Power MOSFET, TCAD Simulations, Ferroelectric Materials, Short-circuit Test.

INTRODUCTION

The use of Silicon Carbide (SiC) power MOSFETs is becoming increasingly popular due to their unique properties, including a wide bandgap, higher critical electric field, and superior thermal conductivity compared to traditional Silicon (Si) MOSFETs [1]. The reliability assessment of SiC power MOSFETs holds significant importance across various industries, such as automotive and aerospace, where these devices find numerous applications. A crucial validation test to assess reliability of SiC power MOSFETs is short-circuit (SC) [2]. Typical applications require a minimum short-circuit withstand time (SCWT) in the microsecond range. Typically, current devices are required to withstand the supply voltage for at least 5 µs. In this investigation, TCAD simulations are employed to gain insights into the behaviour of a 1.2 kV SiC power MOSFET, with a gate insulator that consists in a stack formed by silicon dioxide (SiO_2) and a non-linear dielectric (NLD) exhibiting a Curie-Weiss temperature dependence commonly found in ferroelectric materials [3,4]. During a short circuit event, the device experiences a sudden surge in current, which can lead to a significant increase in power dissipation. This sudden increase in power can cause localized heating, leading to hotspots within the device. This study illustrates how the implementation of an NLD, characterized by a temperature-dependent permittivity (ε), can effectively reduce the temperature rise. This advancement in gate insulator technology could significantly improve the overall reliability and performance of SiC power MOSFETs in various applications. A sketch of the proposed device, with a SiO_2/NLD stack as gate insulator, is reported in Fig.1.

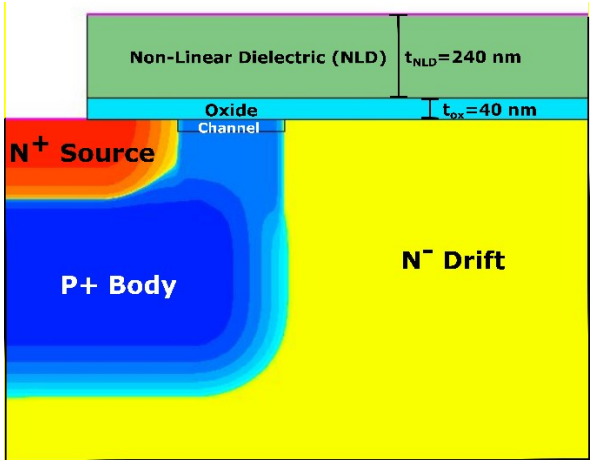

Fig. 1. Sketch of the proposed design, with an oxide/non-linear dielectric stack as gate insulator.

DEVICE MODELING

In the initial phase of the study, the non-linear dielectric (NLD) was implemented via the physical model interface of Sentaurus TCAD. The NLD was designed with the same properties of an oxide, except for its temperature-dependent permittivity. The latter was based on the ferroelectric material vinylidene fluoride trifluoroethylene P(VDF-TrFE) [5], whose permittivity has the behaviour described by Eq. 1.

$$\varepsilon = \lambda \frac{C_{CW}}{T - T_0} \; with \begin{cases} \lambda = -1/2 & for \quad T < T_0 \\ \lambda = 1 & for \quad T > T_0 \end{cases} \qquad (1)$$

P(VDF-TrFE) is characterized by a Curie Temperature (T_0) of 355 K, a Curie Weiss constant (C_{CW}) that is 3429 K, for the ferroelectric phase ($T<T_0$), and 11878 K for the paraelectric phase ($T>T_0$). The graphical representation of the resulted permittivity, varying the temperature, can be seen in Fig. 2.

Subsequently, the capacitance exhibited by the oxide/NLD stack was analyzed through AC simulations. Fig. 3 illustrates the variation of capacitance per unit area with temperature for anthe oxide/non-linear dielectric stack, featuring an oxide thickness (t_{OX}) of 40 nm and different NLD thicknesses (t_{NLD}). Below the Curie Temperature, as the temperature of the stack rises, the capacitance increases owing to the rising permittivity of the NLD. However, once the temperature surpasses the Curie Temperature, the permittivity of the NLD starts to decrease, resulting in a reduction of capacitance exhibited by the stack.

Next, the oxide/NLD stack replaced the standard gate oxide into the TCAD model of a commercial 1200 V SiC MOSFET, which had been previously calibrated using experimental data [6]. To match the transfer and output characteristics of the MOSFET with a standard gate oxide at the typical operating temperature of 340 K in automotive applications, the oxide thickness (t_{OX}) and the NLD thickness (t_{NLD}) were set at 40 nm and 240 nm, respectively. The performance of this proposed structure was compared to a reference structure with a gate oxide thickness of 50 nm, which is the typical thickness for 1.2 kV SiC MOSFETs. The comparative analysis of the two structures is presented in Figs. 4 and 5, witnessing a good agreement between the proposed and reference structure both sub-threshold and over-threshold.

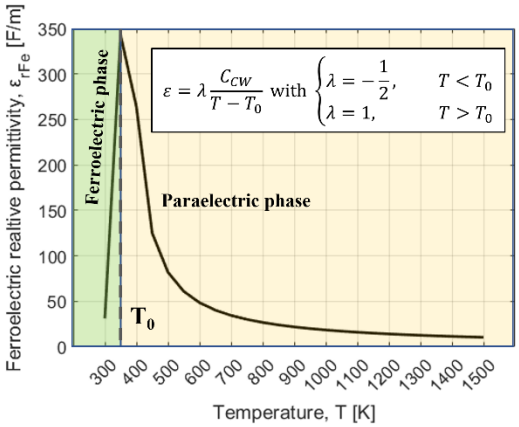

Fig. 2. Relative dielectric permittivity of the ferroelectric material P(VDF–Trifle), used to model the non-linear dielectric. Inset of the figure: general analytical model of the relative dielectric permittivity of a ferroelectric material.

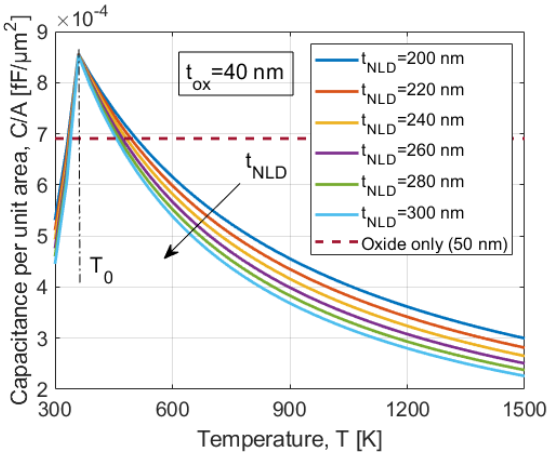

Fig. 3. Oxide/NLD stack capacitance keeping the oxide thickness (tox) fixed and varying both temperature and NLD thickness. As the temperature rises, the capacitance of the stack increases until it reaches the Curie temperature, T_0. Beyond T_0, the capacitance starts to decrease with further increases in temperature. Additionally, the capacitance decreases as the NLD thickness increases.

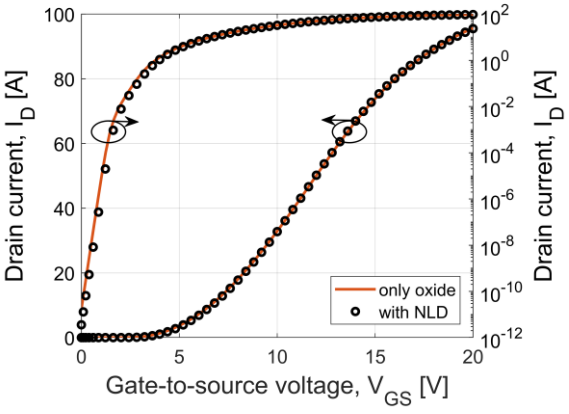

Fig. 4. Comparison between isothermal transfer characteristics of the reference MOSFET (with a 50 nm-thick oxide as gate insulator) and the proposed design (with the oxide/NLD stack, t_{ox}=40 nm and t_{NLD}=240 nm) at T=340 K (V_{DS}=20 V).

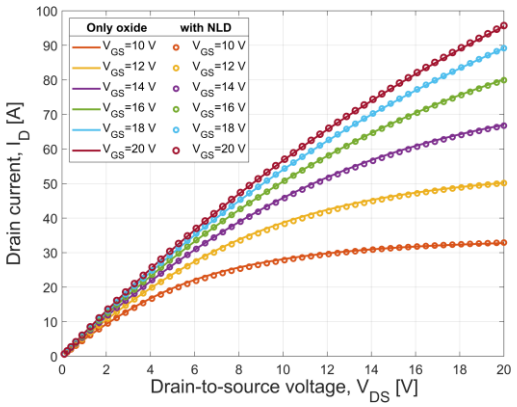

Fig. 5. Comparison between isothermal output characteristics of the standard MOSFET (with a 50 nm thick oxide as gate insulator) and the proposed design (with the oxide/NLD stack, t_{ox}=40 nm and t_{NLD}=240 nm) at T=340 K..

RESULTS AND DISCUSSION

Short-circuit behaviour

To evaluate the performance of the proposed design in short-circuit scenarios, mixed mode electrothermal simulations were conducted [7]. The circuit used for the short-circuit simulations is reported in Fig. 6. In this setup, a pulse source is connected to the gate terminal to allow the current flow into the device, while a constant supply voltage (V_{BUS}) is connected to the drain terminal. To account for thermal effects arising during the transient operation, a thermal resistance (R_{TH}) of 0.01 cm^^{2}K/W is connected to the drain terminal. Moreover, to address parasitic elements introduced by wires and connections, additional stray inductances of 7 nH and 40 nH are integrated into the circuit, connected to the source and drain terminals, respectively. The test was performed with a gate-to-source voltage (V_{GS}) of 18 V and a V_{BUS} of 800 V, with an on-state time (T_{ON}) of 5 µs. As shown in Fig. 7, the proposed structure demonstrates better short-circuit performance, with a maximum temperature 40% lower than that of the reference structure (1230 K instead of 2050 K). Furthermore, the proposed structure exhibits a notable absence of the change in slope at the end of the SC pulse, which is commonly observed in the standard structure [8]. This absence is attributed to the lower temperature reached in the proposed design. As a result, the risk of failure due to thermal runaway is mitigated significantly. These observations are corroborated by the current density of electron and hole, observed at 5.5 µs (i.e., at turn-off) and reported in Fig. 8. Regarding to the structure with the NLD stack, the hole current density distributions (Fig. 8(a, c)) witness a lower current conducted, while the electron current density distributions (Fig. 8(b, d)) show a decrese in the generations of the holes in the body body region, compared with the standard one.

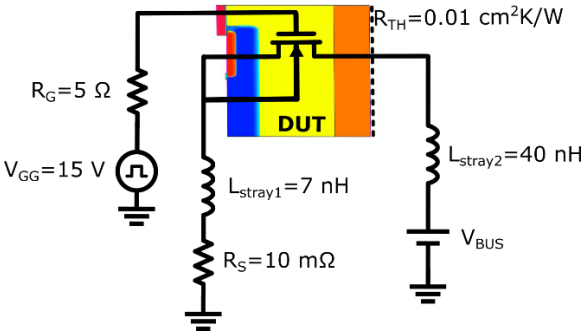

Fig. 6. Mixed-mode circuit for the electrothermal simulation of shortcircuit. RG=5 Ω, RS=10 mΩ, Lstray1=7 nH, Lstray2=40 nH. A thermal resistance (RTH) of 0.01 cm2K/W is set on the drain contact.

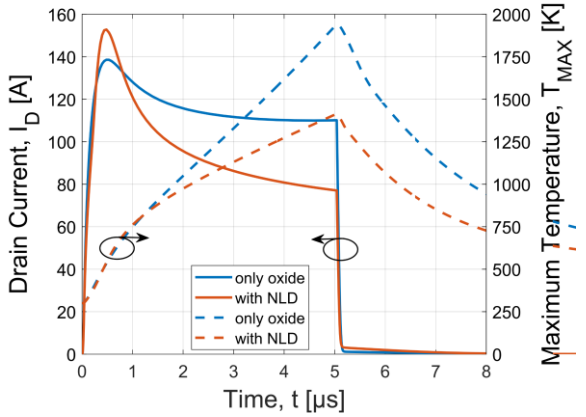

Fig. 7. Short-circuit waveforms for a supply voltage of 800 V applied for 5 µs. The proposed structure reaches a maximum temperature more than 500 K lower than the standard structure.

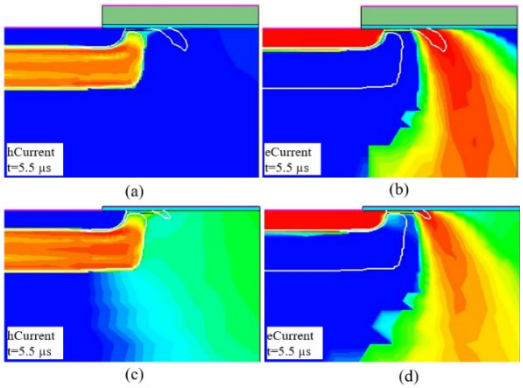

Fig. 8. Holes current density (a), (c), and electrons current density (b), (d) at t=5.5 µs for the proposed structure (top) and standard structure (bottom) for a SC test at 800 V.

Threshold voltage temperature dependence

In Fig.6, the temperature dependence of the threshold voltage of proposed structure and standard structure is shown. The threshold voltage was extracted as the voltage at which the electron density value in the channel reached the ionized acceptor concentration. The analysis was performed for a V_{DS} of 0 V, in order to eliminate two-dimensional effects. When the temperature reaches high

values (e.g., for T>600 K), V_{TH} of NLD-stack structure becomes lower than standard structure due to the increasing influence of the NLD. However, such a small discrepancy cannot be responsible for the short-circuit capability enhancement.

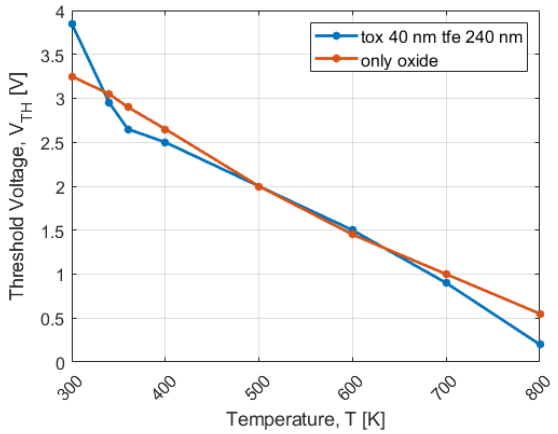

Fig. 9. Threshold voltage comparison varying temperature between proposed structure and reference

CONCLUSION

In this work, it has been shown how replacing the standard gate oxide of a 1.2 kV SiC MOSFET with a oxide/NLD stack would improve its short-circuit capability, since the temperature increase of the device is lowered of about 40% compared with a MOSFET with a standard gate oxide. Since the variation of the threshold voltage with temperature does not present substantial variation between standard and proposed structures, the improved behaviour is dominated by the variation of the capacitance on the current.

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Evaluation of Characteristics and Turn-off dV/dt Controllability of 1.2 kV SiC Si Hybrid Power Switch

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Abstract

Maintaining high efficiency and low power loss during different load conditions are key requirements for power electronic applications including electrical motor drives. Silicon carbide (SiC) MOSFETs offer fast switching with low losses. However, the cost of SiC MOSFETs is significantly higher compared to silicon (Si) trench IGBTs and will remain so for a considerable future. Also, at high currents, the on-state resistance of SiC MOSFETs becomes higher compared to the slope resistance of Si trench IGBTs. Furthermore, the sharp switching edges of SiC MOSFETs and their high dV/dt can cause degradation of motor winding or failure, detrimental bearing current and electromagnetic interference (EMI). This paper reports the device characteristics, working principle, and dV/dt controllability during turn-off of a 1200V hybrid power switch (HPS) based on parallel configuration of Si IGBT and SiC MOSFET technologies. The results, which are based on the latest IGBT and SiC technologies, show a significant reduction in switching as well as conduction losses and show that such a combination can combine the advantages of both of these technologies while being cost effective. It is demonstrated that the hybrid power switch can achieve switching losses as low as a SiC MOSFET with intelligent control of the device.

Keywords: Silicon Carbide, MOSFET, IGBT, Hybrid Power Switch, Power Density

INTRODUCTION

Silicon based insulated gate bipolar transistors (IGBTs) are key players in industrial motor drives and electric vehicle (EV) traction systems because of their high performance to cost ratio. IGBTs rely on conductivity modulation schemes where both electrons and holes contribute to the current flow to achieve a lower on-state resistance beyond the 1-dimensional material limit of silicon. While this is beneficial for on-state resistance, this feature also limits the switching speed, particularly during turn-off. The additional charges created by the conductivity modulation need to be evacuated from the drift region before the device can turn-off. The charge removal process is slow due to a long carrier lifetime which results in a tail current effect that increases the switching losses. IGBTs also suffer from an inherent p-n junction voltage drop of ~0.7V that results in significant conduction losses at low current levels. Moreover, trench IGBTs suffer from dynamic avalanche. Dynamic avalanche appears during turn-off switching transitions where the current filamentation may occur near trench gate edges at high dV/dt conditions [1]. This poses a fundamental current limiting factor for IGBTs to achieve high power density, low switching losses and long-term reliability [2, 3]. Unipolar devices such as SiC MOSFETs, are capable of fast switching with low losses that are at least an order of magnitude lower than their silicon IGBT counterparts [4, 5]. Unlike IGBTs, they turn-on at zero drain bias as long as the applied gate voltage is above its threshold voltage that enables current flow with low on-state resistance particularly at low current levels. However, a major issue is the significantly high costs related to these devices. The costs increase significantly with area (or current) requirements due to defect density limitations and associated yield.

In EVs, the power is sourced from battery packs or fuel cells which have a limited capacity. Thus, high efficiency is a critical aspect in the design of electrical powertrain to sustain over a distance. Since such systems operate at wide ranging load conditions, power semiconductor devices should be capable of sustaining efficient low loss operation over a wide range. It is clear that neither of these technologies (Si IGBTs or SiC MOSFETs) can offer a complete solution today. This is one of the reasons why most, if not all the EV drive systems include parallel combinations of SiC MOSFETs and Si IGBTs as separate modules.

Hybrid power switches (HPS) have been proposed to combine the advantages of bipolar and unipolar devices [6, 7]. HPS are formed by parallel configuration of IGBTs and MOSFETs. The exact ratio of MOSFET to IGBT depends on the application requirements and their mission profiles. Many studies have reported HPS designs based on discrete packaged devices and recently in module formats [8-16]. HPS current and power rating can be scaled up by addition of more Si IGBTs without a significant increase in costs and switching losses. Hybrid devices rely on a MOSFET (or multiple MOSFETs) for

handling partial load current conditions as well as switching transitions. IGBTs, have longer switching delay times than MOSFETs. The gate drive circuitry is one of the main challenges in HPS designs. A special gate drive circuit scheme is needed to account for the delay times of each individual switch in such a way to ensure the MOSFET is turned-off after the IGBT. Several studies have reported various gate driver designs for HPS [17, 18].

One of the key aspects of hybrid switches for their application into industrial motor drives and EVs is their dV/dt controllability. In motor drives, a high dV/dt can induce a detrimental bearing current, insulation degradation or failure of motor windings that limits the operational life span of the system [19-21]. Also, a high slew-rate contributes to EMI related issues if not controlled. To address these challenges, addition of passive filter components is necessary which results in increased weight, size, and costs [22]. Alternatively, this requirement can be met through dV/dt control of the power switching devices which can be realised via a high gate resistor which results in higher switching losses.

This paper presents a hybrid device configuration based on discrete Si IGBT [23] and SiC MOSFET [24] both of which are housed in TO-247 package. The device characteristics, working principle and turn-off dV/dt controllability are presented and analysed. The turn-off energy loss is also investigated with respect to the dV/dt to evaluate the improvements against the HPS constituent components, IGBT and MOSFET.

DEVICE STRUCTURE & CHARACTERISTICS

Configuration and Working Mechanism

The hybrid device is made by parallel configuration of a SiC MOSFET (CoolSiC from Infineon) [24] and Si IGBT (IGBT7 from Infineon) [23] as shown in Fig. 1. Both devices are rated 50A and 1200V and are housed in TO-247 packages.

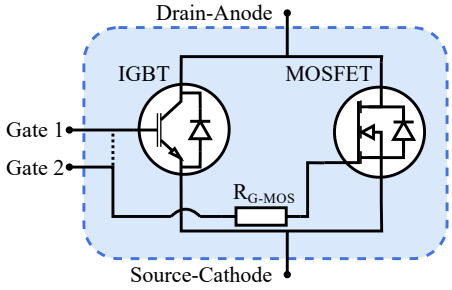

Fig. 1. 1200V hybrid power switch (HPS) configuration. The gates can be controlled independently or connected depending on the gate driver configuration.

The MOSFET is much faster, and its delay time is smaller than the IGBT. Consequently, during the turn-on, the MOSFET is switched prior to the IGBT. Thus, the turn-on behaviour is mainly determined by the MOSFET. However, during the turn-off, this leads to undesirable turn-off of the MOSFET before IGBT. Ideally the two gates need to be controlled independently to ensure that the IGBT is turned-off before the MOSFET. Alternatively, this can partially be improved by adding a separate gate resistor ($R_{G\text{-}MOS}$) for the MOSFET. The resistor increases the delay time of the MOSFET. The drawback of this method is that it limits the slew-rates of the device. The resistor can also help to dampen high frequency gate oscillations due to parasitic inductances and characteristics mismatch. The constituent components of the HPS are capable of withstanding short circuit fault. The IGBT and MOSFET are rated for short circuit withstand time of 8µs at 600V and 3µs at 800V respectively [23, 24].

In forward conduction mode, the device operates in unipolar or bipolar regime depending on the load current. At high load current of above ~35A, the IGBT handles the majority of current due to its lower resistance. Meanwhile, at low current levels, the current is primarily handled by the MOSFET. The exact current sharing between the individual devices depends on the on-state resistance and voltage drop of each device at a given operating current and temperature. The reverse conduction is facilitated via the IGBT extrinsic Si diode and the MOSFET. An ideal solution would be to co-pack a SiC Schottky barrier diode that has a low reverse recovery and fast switching characteristics. In this paper, the HPS performance is tested with both gates connected using a single gate control and separately using dual gate control.

Forward Characteristics and On-state Behaviour

The forward I-V characteristics of the hybrid device were measured at room temperature at different gate voltages as shown in Fig. 2.

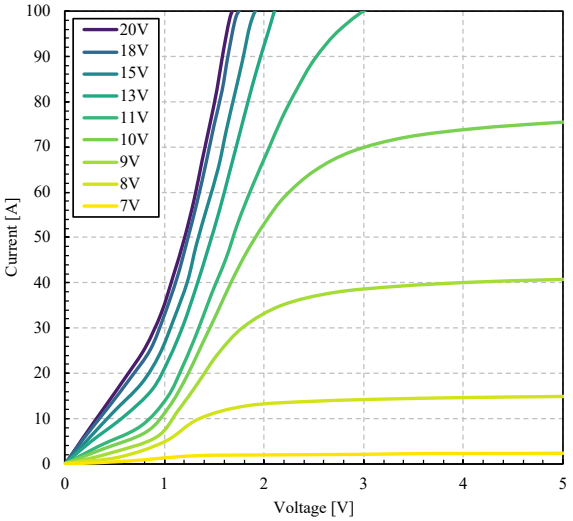

Fig. 2. Measured forward (I-V) characteristics of the hybrid power switch at different gate voltages at 25˚C. The pulse width is 250µs.

The voltage drop across the device is 1.2V at 50A, 18V gate voltage, and at 25˚C. This is 28% and 39% lower than the individual components of IGBT and MOSFET

respectively. The I-V curves of the hybrid device are compared to constituent individual devices as shown in Fig. 3.

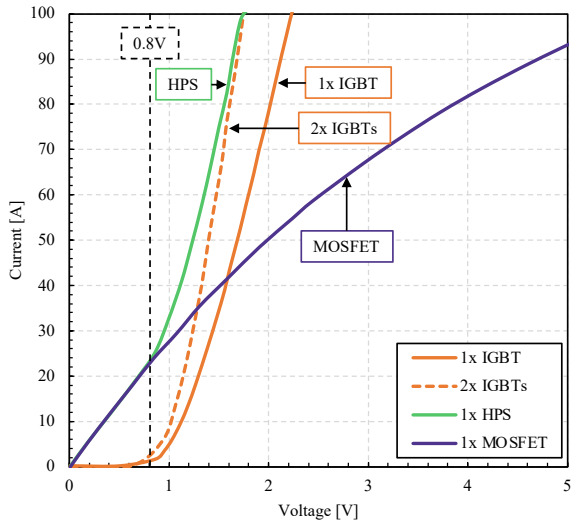

Fig. 3. Measured I-V curves of devices at 25˚C. The gate voltage is 18V.

In the low current region of less than 25 A, the HPS characteristics match with the 1x MOSFET. This is because the voltage across the IGBT must be higher than ~0.7V before it can conduct any current at room temperature. On the other hand, due to the unipolar nature of the MOSFET, there is no initial voltage drop and the device conducts at any drain voltage (V_{ds}) larger than 0V when the gate voltage (V_{gs}) is higher than its threshold voltage ($V_{gs\text{-}th}$). In high current region, above 25A, the HPS enters the bipolar mode of operation. The MOSFET resistance rises and the current starts to divert to the IGBT. This characteristic of the HPS can result in an optimum current handling capability over a wide range of load conditions. To evaluate the conduction losses, the on-state voltage drops of the HPS, and each individual component are measured at 50A at different junction temperatures as illustrated in Fig. 4.

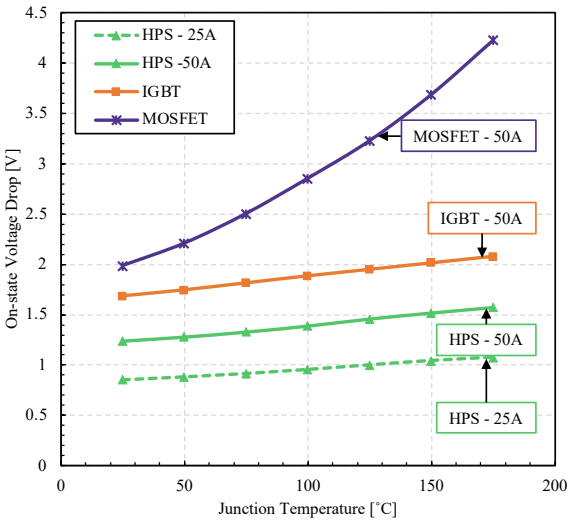

Fig. 4. Measured comparison of the on-state voltage drops of the HPS and its individual components at different junction temperatures at gate voltage of 18V.

SiC MOSFETs have a higher positive temperature coefficient of voltage than the Si IGBT and the HPS. This is because of the conductivity modulation of the IGBT and HPS. Therefore, the HPS can maintain a minimal conduction loss over a wide range of load current and temperatures. At high operating temperatures (175˚C), the hybrid device shows 63% lower voltage drop compared with that of the MOSFET. It is also important to note that as the temperature rises, the bipolar onset voltage decreases and IGBTs can conduct at lower drain/anode voltages. This property enables the HPS to demonstrate high efficiency at high temperatures.

Reverse Conduction Characteristics

The reverse conduction characteristics of the HPS are shown in Fig. 5 and compared with the HPS components.

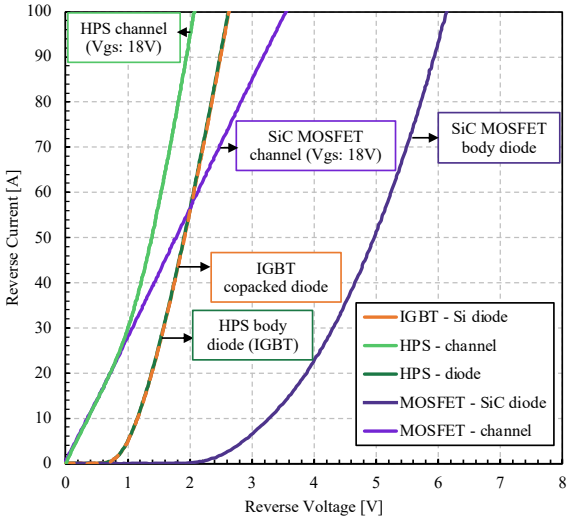

Fig. 5. Measured reverse characteristics of the HPS and its integral components.

The HPS consists of an IGBT that is co-packed with an extrinsic Si diode and a SiC MOSFET that has an intrinsic SiC body diode. The SiC p-n body diode has a high forward voltage drop of 5V at 50A while the forward voltage drop of Si diode at 50A is 1.9V. During the off-state (V_{gs} = 0V), the reverse characteristic of the HPS is identical to the IGBT co-packed Si diode. Once a positive gate voltage (V_{gs} = 18V) is applied, the voltage drop decreases further as the current is shared between the MOSFET and the co-packed Si diode. The voltage drop of the HPS during reverse conduction is 1.39V compared with 1.78V of the MOSFET at 50A because the current is shared by the Si diode within the HPS. Under normal operating conditions, the SiC body diode does not contribute to current flow due to its high forward voltage drop.

EXPERIMENTAL SETUP

A clamped inductive switching test bench was set up to evaluate the switching performance of the hybrid power switch as shown in Fig. 6.

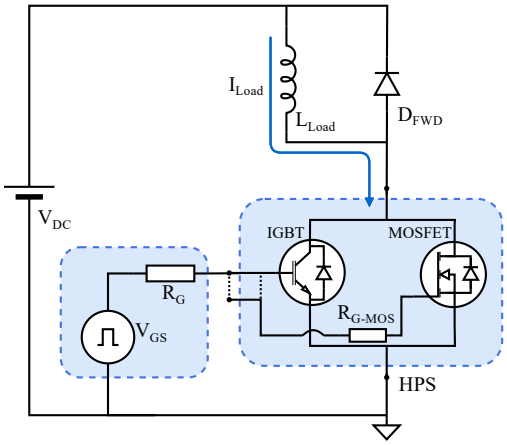

Fig. 6. Simplified circuit diagram of the experimental setup.

The setup uses a 240µH inductor as the load which is clamped by a 1200V SiC Schottky barrier diode (D_{FDW}). The supply voltage (V_{DC}) is fixed at 600V, and the load current (I_{load}) is 50A. The test was conducted at different external gate resistor values to determine the dV/dt controllability and switching losses. In part one of the experiment, the HPS was controlled using a single gate drive approach. In this configuration both gates are connected. The gate drive circuitry provides a pulse with an amplitude of +18V and -5V for turn-on and turn-off respectively. In the second part, a dual gate control was implemented to control the HPS gates separately. In this part, the turn-off gate voltage is 0V and -5V for the MOSFET and IGBT respectively. The positive gate voltage is 18V for both devices. A delay time of ~1µs is imposed on the MOSFET. The experiment was repeated for individual components of the hybrid device for comparison purposes. For fair evaluation, the gate driving conditions are kept the same. The dV/dt and rise time are calculated based on the changes in drain/anode voltage from 10% to 90% of the drain switching transition. The switching power losses are determined by the overlap of the voltage and current during the switching transition and it is then integrated to calculate the energy loss.

MEASUREMENTS RESULTS AND DISCUSSION

Independent Gate Control Method

As previously mentioned, MOSFETs delay times are generally shorter than their IGBTs counterparts which is particularly important during the turn-off. To address this issue, two gate signals are required to add a delay to the MOSFET gate. This results in a smaller pulse width applied to the IGBT gate. Fig. 7 shows the dual gate control waveforms of the HPS.

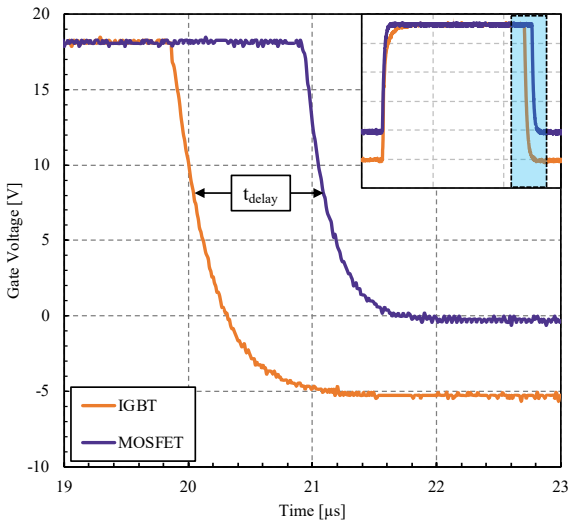

Fig. 7. Measured Individual gate of the HPS using independent dual gate control.

The delay time needs to be adjusted to ensure that the IGBT is fully switched-off before the MOSFET. The switching waveforms of the HPS with ~1µs delay time is shown in Fig. 8.

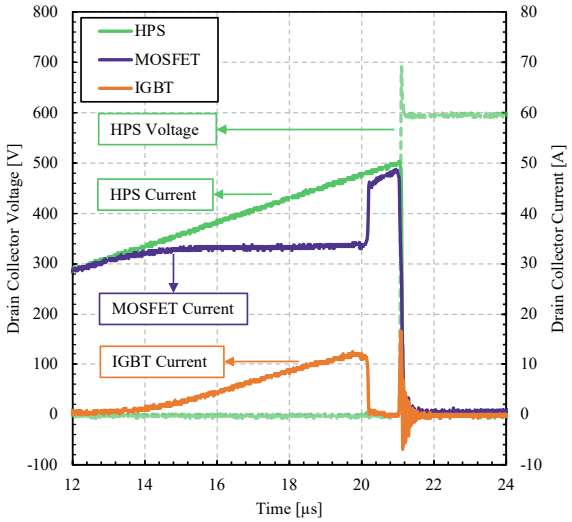

Fig. 8. Measured turn-off switching waveforms of the HPS using dual gate control.

In this configuration, the IGBT experiences zero-voltage-switching (ZVS) and does not contribute to the switching losses of the HPS. Consequently, the switching characteristics of the HPS is mainly determined by its MOSFET. As the HPS current rises, the MOSFET drain current is clamped to ~34A, as the IGBT takes over current share due to its lower voltage drop. As the IGBT turns-off, the current is diverted to the MOSFET for the period of delay time that causes a surge current. The delay time should be kept minimal to avoid extra load stress on the MOSFET.

Turn-Off Switching Characteristics

The test was conducted to determine and evaluate the turn-off switching characteristics and dV/dt controllability of the hybrid power switch. Initially, the HPS was tested with a single gate control. The corresponding switching waveforms are shown in Fig. 9 at different gate resistances.

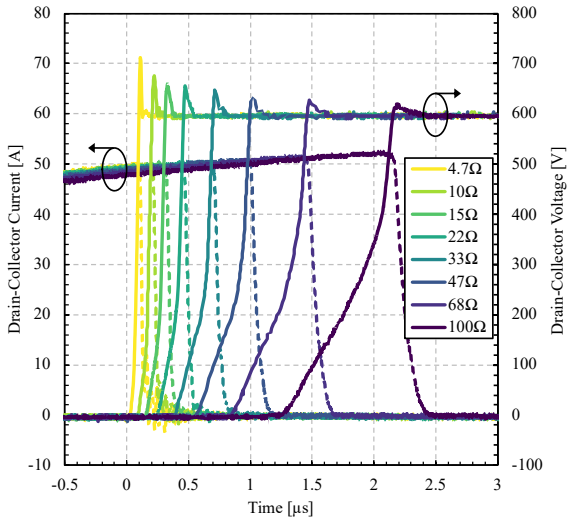

Fig. 9. Measured turn-off switching waveforms of the HPS using the single gate control at different gate resistances. The gate voltage is 18V and -5V for turn-on and turn-off respectively.

The test was repeated for the HPS using dual gate control approach. In this configuration both gates were driven independently. A delay time of 1µs was added to ensure the IGBT turns off before the MOSFET. The gate resistor for the IGBT was fixed at 15Ω and the gate resistor for the MOSFET was varied from 1Ω to 150Ω. The turn-on and turn-off gate voltage is 18V and 0V for the MOSFET respectively. The turn-on gate voltage of the IGBT is also 18V with -5V for the turn-off. The corresponding switching waveforms are shown in Fig. 10.

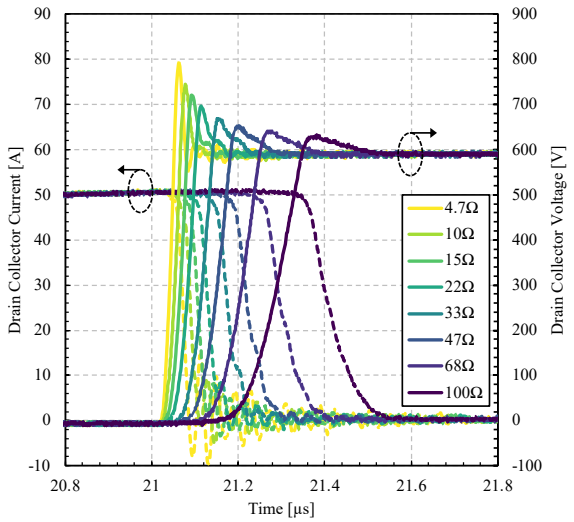

Fig. 10. Measured turn-off switching waveforms of the HPS using dual gate control at different gate resistances. The IGBT gate resistance is fixed at 15Ω with a 1µs delay time.

In both configurations, the switching slew-rates decrease as the gate resistor value increases, which demonstrates the dV/dt controllability of the hybrid device. It can be observed that at high gate resistances the switching waveforms of the HPS using a single gate control are like the IGBT switching waveforms shown in Fig. 11. This is because the delay time of the IGBT is dominant at high gate resistances.

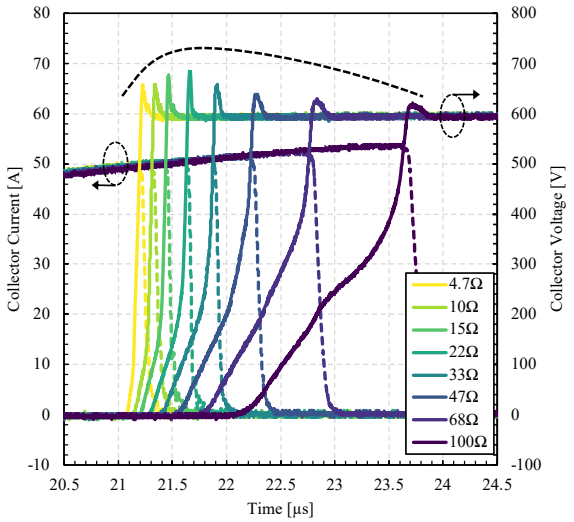

Fig. 11. Measured turn-off switching waveforms of two IGBTs in parallel configuration at different gate resistances. The gate voltage is 18V and -5V for turn-on and turn-off respectively.

While the slew rate slows down at high gate resistances, an inverted 'U' shape can be seen by the peaks which is attributed to dynamic avalanche. This is a critical limitation for IGBTs which limits their operating dV/dt. For example, in this case, the device's minimum required gate resistor for reliable operation is about 22Ω to effectively suppress the dynamic avalanche. In hybrid configurations, dynamic avalanche is suppressed because the current is handled by the MOSFET which does not suffer from dynamic avalanche.

dV/dt Controllability and Switching Losses

The dV/dt and voltage rise time of the HPS were extracted from the measured switching waveforms and compared with the HPS constituent components as shown in Fig. 12.

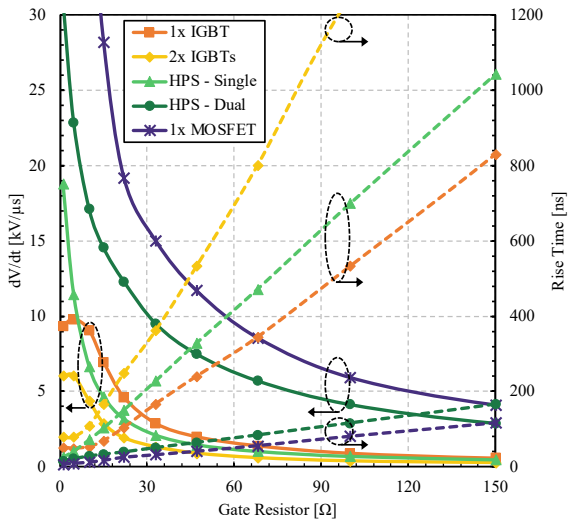

Fig. 12. Measured dV/dt and rise time of the HPS and its components. HPS single refers to the single gate drive and HPS dual refers to the dual gate drive methods.

Due to the absence of dynamic avalanche in the HPS, dV/dt can reach as high as 19kV/µs with single gate control. The HPS dV/dt can further increase beyond 30kV/µs by using a separate dual gate control. The dV/dt of the 1x IGBT and 2x IGBTs are limited due to presences of dynamic avalanche at low gate resistances (R_g < 10Ω). In the dual gate approach of the HPS, the IGBT turn-off transition is completed before the MOSFET, and the gate capacitances are discharged. The output capacitance of the IGBT and its co-packed diode, however, needs to be charged and thus the rise time is slightly higher than the 1x MOSFET.

The corresponding turn-off energy losses are calculated from the measured data for each device as shown in Fig. 13.

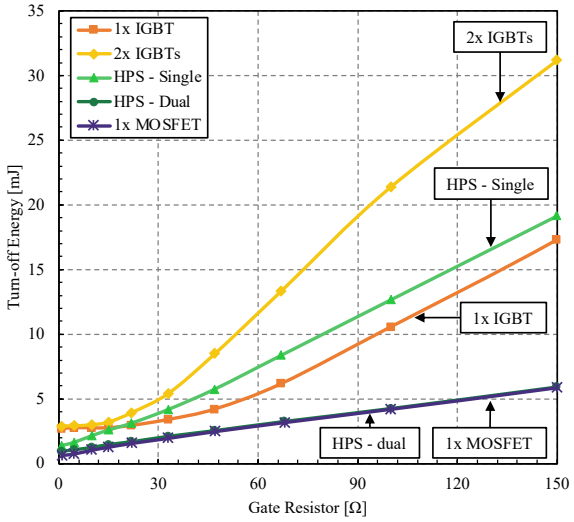

Fig. 13. Comparison of the corresponding turn-off switching energy losses at different external gate resistances.

The HPS using a dual gate control offers a significant reduction in energy losses due to the enhanced switching capability. In this configuration the IGBT is not involved in the switching and the MOSFET determines the switching behaviour. Therefore, the turn-off energy of the HPS using dual gate control is effectively the same as 1x MOSFET. Also, with a single gate control, the HPS switching losses are much lower compared to the equivalent 2x IGBTs. It is important to note that, in both 1x IGBT and 2x IGBTs, the energy losses are not linear at lower gate resistances (R_g < 22Ω) because of the dynamic avalanche. As stated before, such an effect does not exist in the HPS configuration.

CONCLUSION

In this work, a hybrid device configuration using a Si IGBT and a SiC MOSFET is presented. The device characteristics, working mechanism and turn-off dV/dt controllability are demonstrated experimentally. It has been shown that the hybrid device can combine the advantages of both technologies in terms of cost and performance effectively while maintaining a low power loss under different load conditions. The device can operate in unipolar or bipolar mode depending upon the current level. The hybrid configuration also maintains a low conduction loss at high operating temperatures. The switching losses show a significant reduction compared to its constituent components as standalone devices. With independent gate control of the HPS, the switching losses can be further optimised. Choosing the appropriate MOSFET is essential as the current during partial load is significantly affected by it. The concept can be scaled up according to the application requirements to accommodate a larger current capacity by addition of more IGBTs. The optimum ratio of IGBT to MOSFET can be investigated in future works. Overall, the hybrid device concept offers a significant reduction in cost to performance ratio due to the widely accessible low price of Si devices, which well suits integration in intelligent power modules.

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Adapted Temperature Calibration for Schottky p-GaN Power HEMTs

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Abstract

The determination of the junction temperature in power semiconductor devices is an important but challenging task. For GaN HEMTs, no universal temperature sensitive electrical parameter (TSEP) is available. In this study, different GaN HEMTs with Schottky p-GaN gate were subjected to stress by positive gate bias and temperature. The gate leakage current is one parameter to determine the junction temperature of Schottky p-GaN gate devices. An adapted calibration routine is applied to stabilize the desired TSEP of different GaN HEMTs. The gate current method can be applied to GaN Systems devices. Furthermore, the investigations indicate stability of the on-state resistance of Innoscience devices and threshold voltage of EPC devices, respectively.

Keywords: GaN HEMT, Schottky contact, p-GaN gate, TSEP, adapted temperature calibration.

INTRODUCTION

Gallium Nitride (GaN) power HEMTs are key components to design power electronic systems with high efficiency and smaller volume. The wide band gap (3.39 eV), the high critical electric field strength and low device capacitances enable small drift layers and high frequency operation. Thereby, switching- as well as conduction losses can be reduced. Currently, devices with Schottky gate are available from several manufactures in the voltage range from 15 V to 700 V [1]–[5]. The device concept enables normally-off operation with a voltage controlled gate. However, due to the lateral concept, the package and chip-near interconnections differ significantly from vertical power electronic devices made of Si (IGBTs, diodes) as well as from SiC (MOSFETs, diodes). Instead of thick-wire wedge bond technologies, nailhead technologies [6], [7] or low-inductive integration [8] are used. Precise knowledge of the junction temperature is relevant for lifetime modelling in e. g. power cycling, but also for the measurement of the transient thermal impedance. Therefore, the use of temperature sensitive electrical parameter (TSEPs) is established [9]. In Schottky p-GaN devices no pn-junction is directly accessible and the forward gate leakage current was introduced as alternative [10]. During this process, the Schottky p-GaN junction at the gate is biased in reverse direction. This is a simultaneous gate stress test within datasheet limits. No hard failures were observed, but device parameters tend to shift [3], [11]. The calibration of temperature at constant gate bias V_{GS} is used to stress the device at high temperatures and static device parameters are monitored.

TEMPERATURE CALIBRATION

In the following, temperature determination in power electronics for reliability testing is discussed. Furthermore, an introduction of the devices and the temperature determination by using the Schottky junction is given.

Temperature Sensitive Electrical Parameters

The temperature of the power electronic chip is usually referred to as junction temperature. Indirect or contactless measurement of these is possible by means of optical processes or electrical methods. Optical measurements for example infrared thermography are challenging in practice, because they require access to the chip surface. Electrical methods like the $V_{CE}(T)$ method utilize the temperature dependency of chip internal parameters like the diffusion voltage of the pn-junction (see **[12]**) for determination of the temperature:

$$V_{bi} = \frac{kT}{q} \cdot \ln\left(\frac{N_D \cdot N_A}{n_i^2}\right) \quad (1)$$

Equation (1) is dominated by the intrinsic carrier concentration n_i, which results in a negative temperature coefficient behavior. Therefore, a constant measurement current is applied to the devices and one obtains the voltage across the total active area. It is also referred to as the virtual junction temperature T_{VJ}. The maximum of the junction temperature cannot be determined by TSEPs, but by simulation or optical methods. In gate injection transistors (GITs); the pn-junction of the gate can be biased at constant gate current of e.g. 10 mA (Figure 1).

The curve can be fitted accurately with a second order polynomial function.

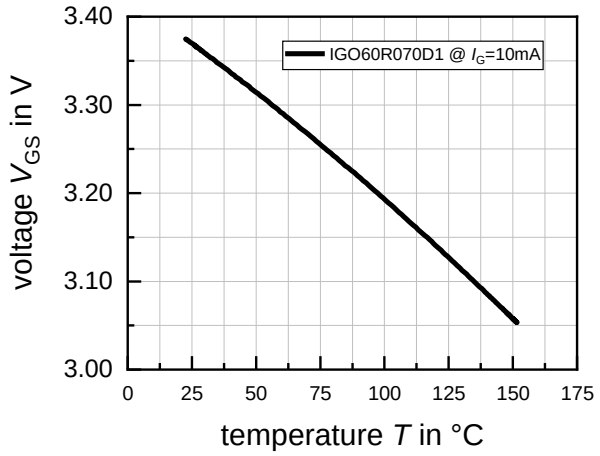

Figure 1: Temperature calibration curve of a GIT IGO60R070D1 from Infineon

Alternatively, on-chip temperature sensors [13] or the internal gate resistance as another TSEP [14] can be used. In contrast to an average value like the virtual junction temperature, on-chip sensors provide local temperatures and permit a measurement also during load current of the device. Overall, on-chip sensing can offer very unique and valuable information, but they are strongly dependent on the sensor positioning.

Schottky p-GaN HEMTs

The schematic cross-section of GaN HEMTs with Schottky p-GaN gate is displayed in Figure 2. The two-dimensional electron gas (2DEG) is depleted by a p-GaN at the gate. The Schottky gate metal results in two back-to-back diodes between gate and source. In MOSFETs, an alternative TSEP is given by the body diode [9]. Despite the fact, that there is no body diode in GaN HEMTs, an inverse barrier forms at zero gate voltage in reverse operation [15]. While the inverse barrier was found to be stable for GITs [16], no stable operation of the V_{SD}(T) voltage was demonstrated for devices with Schottky gate. The back-to-back diode structure has the property that one of the diodes is always operated in the reverse direction. For positive gate bias, the Schottky junction is operating in blocking- and the AlGaN pn-diode in forward direction. In low current regime, below the V_{bi} of the AlGaN pn-diode (approx. 3 V), the current is limited through this. Above, the blocking Schottky p-GaN junction dominates the behavior with its leakage and breakdown behaviour.

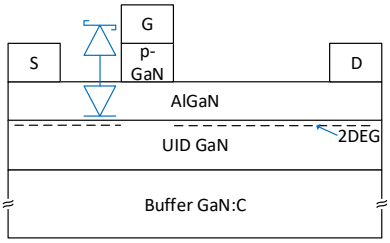

Figure 2: Schematic cross-section of a Schottky p-GaN HEMT

In [10], the possibility of utilizing the reverse leakage current of the Schottky junction at positive gate bias was introduced as TSEP. Therefore, instead of a constant current, a constant gate voltage is to be applied and the temperature dependent gate current I_G(T) is monitored. The gate leakage current of MOSFETs is usually given as I_{GSS} for shorted drain-to-source. Thereby, both capacitances C_{GS} and C_{GD} are biased simultaneously, which theoretically results in a higher overall gate leakage current. However, there is hardly any change between the open-drain and drain-to-source short configuration visible at a nominal voltage of V_{GS} = 6 V (see Figure 3). For online junction temperature determination e.g. in a power cycling test, the additional shortening would represent an increased effort. Hence, the drain can be left open for the temperature calibration, but should be shorted to drain for the gate stress tests. The temperature dependency of the gate leakage current of the Schottky junction can be described by the saturation current in reverse operation [12]

$$j_s = A^* \cdot T^2 \cdot e^{\frac{q(V_B - \Delta\Phi)}{kT}} \qquad (2)$$

Here, A* is the effective Richardson constant and qV_B is the contact barrier height. Under reverse bias operation, the potential is lowered and the image force $\boldsymbol{\Delta\Phi}$ must be considered. Hence, the temperature dependency of the reverse leakage current follows ideally a quadratic dependency.

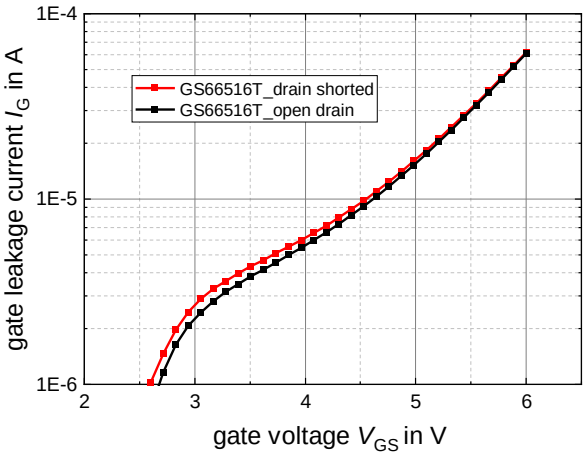

Figure 3: Gate leakage current in drain-to-source short and open-drain configuration for devices GaNSystems GS66516T at T= 25°C

EXPERIMENTAL RESULTS

The gate current method $I_G(T)$ was so far applied to GaNSystems devices in the voltage class of 650 V [7], [10]. Nevertheless, there are still some uncertainties to its validity. Particularly, the possibility of the degradation in the gate leakage current and instabilities in threshold voltage [11]. Here, three devices from different manufacturers and of different voltage class are under investigation. The behavior of the Schottky gate is to be observed under forward bias with respect to temperature, degradation and shift of parameters.

Gate I-V Characteristics

An overview of the devices and selected device parameters are displayed in Table 1. The level of the gate current varies due to the significantly different R_{DSon} that correlates to the gate width of the device and the active area.

Table 1. Investigated devices and selected device parameters

Manufacturer	**Device**	V_{BD} **[V]**	V_{GSnom} **[V]**	R_{DSon} **[mΩ]**
GaN Systems	GS-065-011-2-L **[17]**	650	6	150
Innoscience	INN650D350A **[18]**	650	6	350
EPC	EPC2302 **[19]**	100	5	1.8

The gate I-V characteristics of all three types of devices are displayed with respect to temperature in Figure 4, Figure 5 and Figure 6. The drain and source were shorted to acquire I_{GSS}. The gate current per mm was calculated using the estimated device gate width. The influence of the AlGaN diode is clearly visible for GaNSystems in Figure 4, but is less pronounced at Innoscience (Figure 5) or EPC device (Figure 6). At nominal gate voltage, the device from EPC has the lowest gate leakage current density.

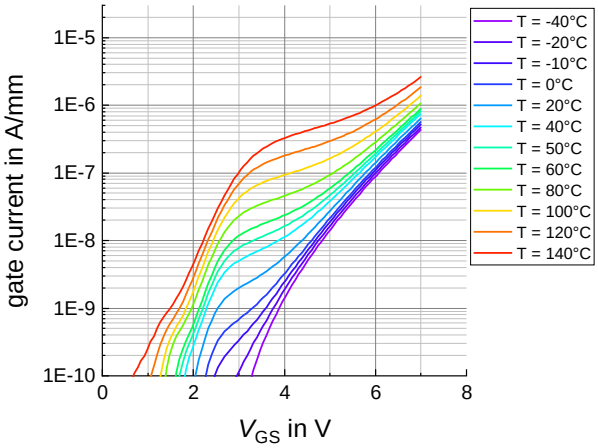

Figure 4: GaNSystems GS-065-011-2-L - gate leakage current at shorted drain-source for various temperatures

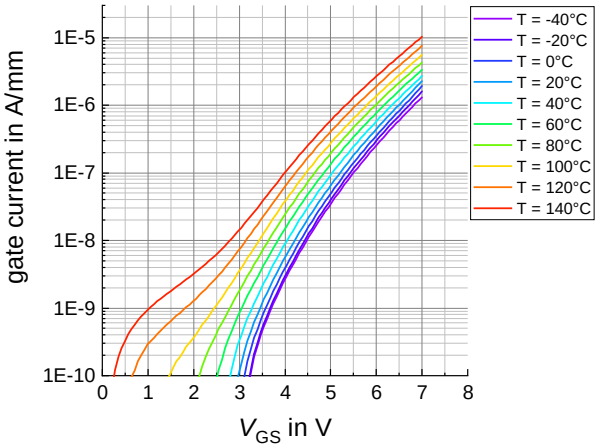

Figure 5: Innoscience INN650D350A - gate leakage current at shorted drain-source for various temperatures

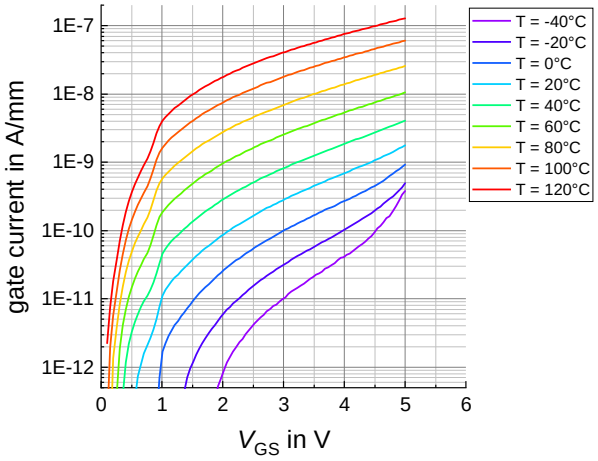

Figure 6: EPC 2302 - gate leakage current at shorted drain-source for various temperatures

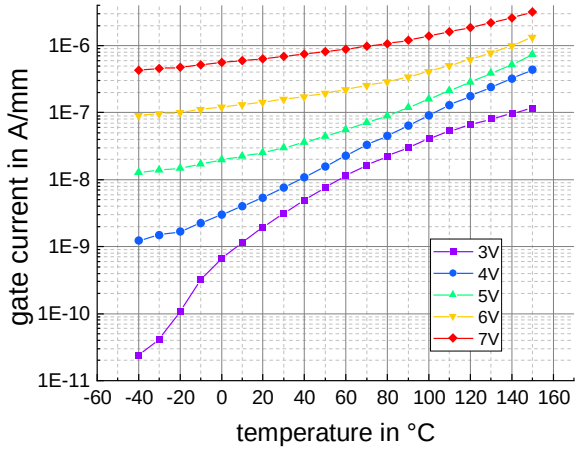

Figure 7: GaNSystems GS-065-011-2-L temperature dependent gate leakage current at shorted drain-source for different gate voltages

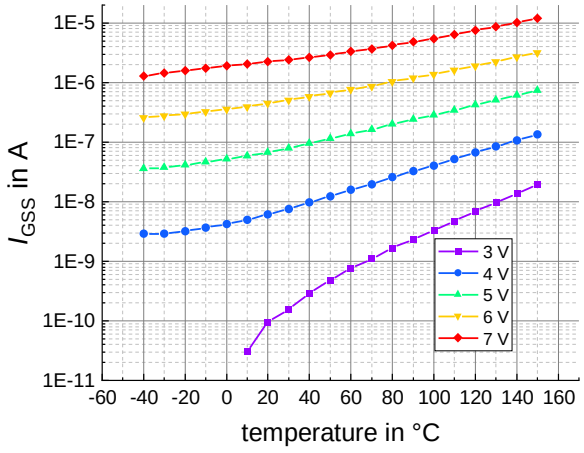

Figure 8: Innoscience INN650D350A temperature dependent gate leakage current at shorted drain-source for different gate voltages

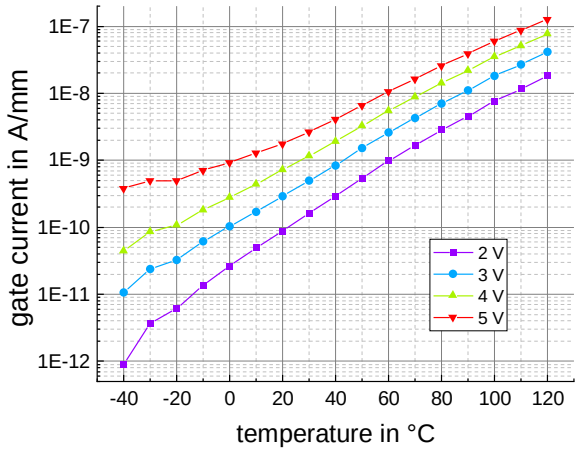

Figure 9: EPC 2302 temperature dependent gate leakage current at shorted drain-source for different gate voltages

The GaNSystems device in Figure 7 shows a strongly increasing gate leakage current tendency at higher temperatures and gate voltages. However, the influence of the gate voltage on the gate leakage reduces with increasing current and the curves are closer together at 150°C than at -40°C. Furthermore, at a gate voltage of 3 V, the influence of the temperature dependency of the pn-junction at low temperature is significant. Similar behavior is observed for the Innoscience device. It must be noted that the device – from on-state resistance point of view – is approximately 3 times smaller than the investigated GaNSystems device. For gate voltages of 4 V to 7 V a nearly parallel shift is identified. The EPC device in Figure 9 indicates a much stronger, highly exponential behavior across the complete temperature range. At 2 V, the gate current increases by five orders of magnitude from -40°C to 120°C. This increase reduces for larger gate voltages.

Ideally, the nominal gate voltage should be used for the temperature determination to achieve a high saturation current and low on-state resistance. From the perspective of curve fitting, the gate current method can be applied to all three devices at their nominal gate drive condition.

Degradation under Positive Gate Bias

In this work, the focus is on further exploring the methodology for temperature calibration by the Schottky gate leakage current, which is often implicating parameter deviations [11]. The degradation of the gate current during positive gate stress test is depending on the process technology, temperature and level of applied bias [11], [20]. Depending on the condition, the gate current either increases or decreases [20]. At high temperatures and high gate bias, a logarithmic increase of the gate current was observed [7]. At nominal gate voltage of V_{GS} = 6 V and temperature of 120°C, an increase by 13% is observed for the GaNSystems device (Figure 10). After 2 hours of continuous constant stress, I_{GSS} becomes almost stable.

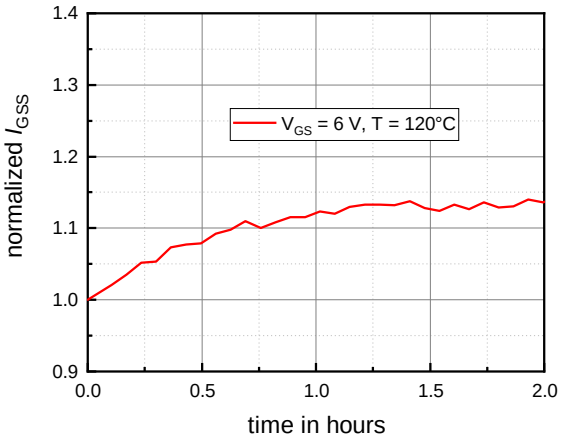

Figure 10: Course of the gate leakage current I_{GSS} for GaNSystems device at 120°C and 6 V over 2 hours

Calibration Routine and Parameter Deviations

Consequently, the temperature calibration itself can also introduce a drift at high temperature and constantly applied positive gate voltage. The temporal course of the applied temperature during the calibration is shown in Figure 11. During the calibration process, the gate voltage is only applied after the maximum temperature is reached. In power cycling tests, the initial maximum temperature is set at the limit of the datasheet and can increase by degradation of the device. Hence, the temperature calibration can exceed the maximum temperature ratings to cover the entire temperature range in the later test. After the devices reached 25°C in the calibration, the gate voltage is removed again. The devices stayed for less than 0.2 hours above 150°C. In order to monitor possible parameter deviation, a calibration and characterization flow was introduced for a comprehensible investigation (see Figure 12). A second, revised temperature calibration is introduced to verify the first temperature calibration.

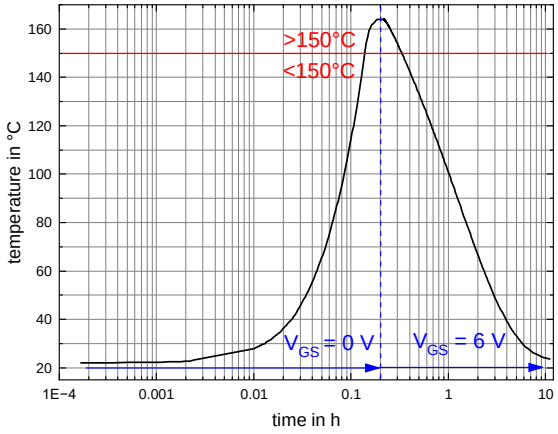

Figure 11: Temperature course with applied gate voltage and critical gate voltage

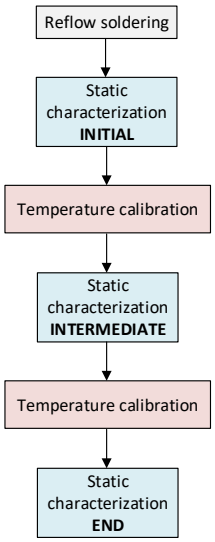

Figure 12: Flow of the temperature calibration and characterization

The described routine of the calibration was applied to all three types of devices. The parameters threshold voltage V_{Gth}, drain leakage current I_{DSS}, gate leakage current I_{GSS}, and on-state resistance R_{DSon} were monitored at initial, intermediate and end state. The results for GaNSystems are given in Figure 14. The first calibration introduces a shift of the static device parameters, but no significant further changes are visible due to the second calibration. The resulting temperature calibration curves are depicted in Figure 13. Except of one device (green), all obtained curves are very comparable. Moreover, the difference between the two calibrations is within measurement accuracy. Hence, the temperature calibration can be utilized to initialize the devices and the $I_G(T)$ method is applicable for GaNSystems. While the gate leakage increased by 22%, the threshold voltage decreased by approx. 24%. The latter corresponds to a maximum of 0.43V, which is within acceptable limits.

For the Innoscience and the EPC devices, further changes are present from first to the second stress by temperature calibration. In Figure 15, the gate leakage current of the Innoscience device increased further and only the R_{DSon} remained stable. The temperature determination by on-state resistance could be an alternative for this component, especially with such high R_{DSon} (350 mΩ). However, if degradation of the assembly and interconnection technology occurs, the calibration curve is only valid as long as an ideal chip sense contact is present.

In contrast to these results, a reduced gate leakage current was observed for the EPC devices (Figure 16). The threshold voltage and on-state resistance remained stable. With an on-state resistance of 1.8 mΩ, the latter is rather unsuited as TSEP. The stable threshold voltage indicates that the inverse barrier V_{SD} indeed might be the parameter of choice.

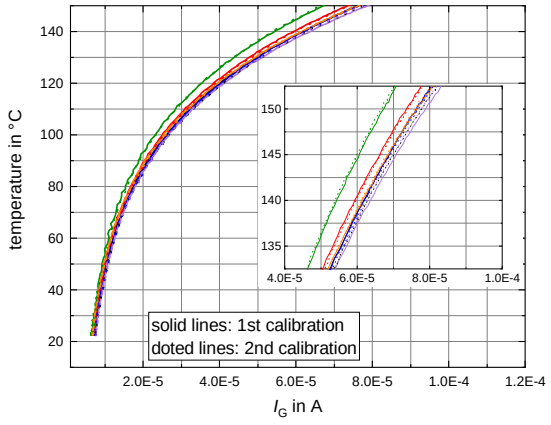

Figure 13: GaNSystems temperature dependent gate leakage current of six devices for two repeated calibrations at V_{GS} = 6 V

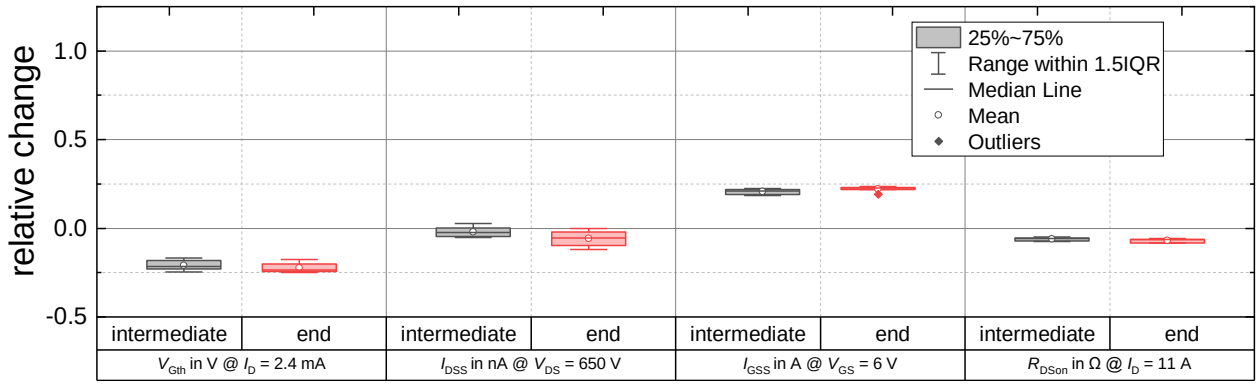

Figure 14: GaNSystems (6 devices) - relative change of parameters after the first and second calibration referred to the initial value

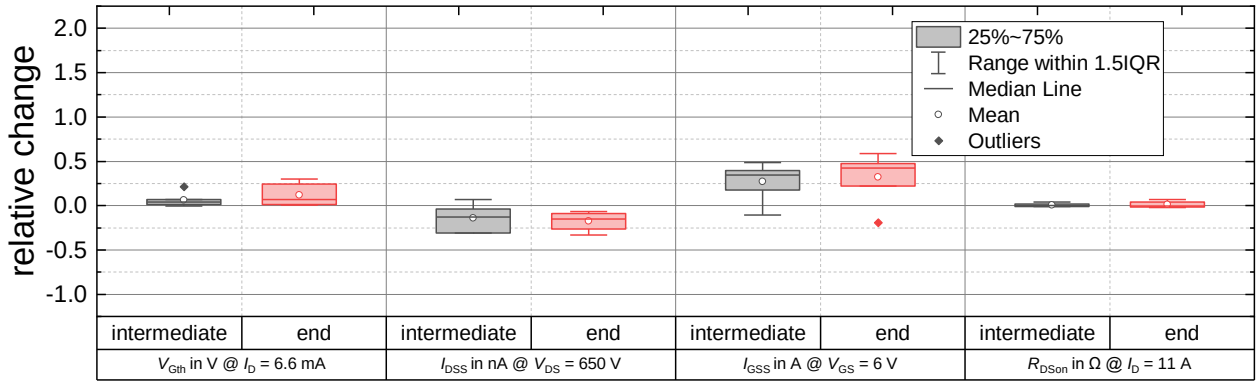

Figure 15: Innoscience (6 devices) - relative change of parameters after the first and second calibration referred to the initial value

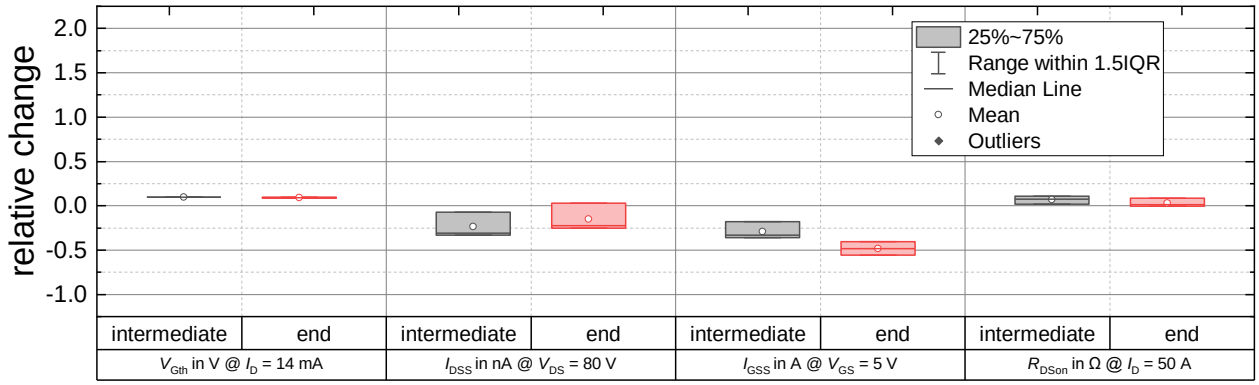

Figure 16: EPC (3 devices) - relative change of parameters after the first and second calibration referred to the initial value

CONCLUSION

The forward gate characteristic of Schottky p-GaN devices was characterized depending on temperature and gate voltage. The strong temperature dependency of the Schottky gate leakage current was pointed out.

During temperature calibration, shifts of device parameters are created under combined stress by gate voltage and temperature (similar effects could happen under power cycling). No universal, reliable parameter for temperature determination was found for GaN HEMTs. Already a temperature calibration can degrade and wear-in the components at once. The I_G(T) method is applicable for GaNSystems devices. Further, potential TSEPs are the on-state resistance for the Innoscience device and the inverse barrier for the EPC device. Further investigations on the degradation of the Schottky gate GaN HEMTs are necessary. For the calibration, a pulsed method is recommended to reduce the gate stress during the calibration procedure. In order to assess the influence of degradation during the power cycling test a recalibration is recommended.

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Power Diode Structures Realized on (113) oriented Boron Doped Diamond

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Abstract

Molybdenum, ruthenium, and platinum contacts covered by the gold capping layer were used for preparation of pseudo-vertical Schottky barrier diodes on (113) oriented homoepitaxial boron-doped diamond. After metal deposition, diodes were stabilized by annealing for 20 minutes at 300 ˚C and their I-V characteristics were measured at temperatures from 30 to 180 °C. Results show that all three metals can be used to realize Schottky diodes with sufficient forward and blocking capability. Moreover, molybdenum and ruthenium can also be used to create a stable ohmic contact on heavily doped contact p^{++} layer. Molybdenum provides optimum properties: a sufficient Schottky barrier height providing low leakage at a level of 10^{-8} A/cm^2 and an acceptable forward voltage drop of 3.80V@J_F=1kA/cm^2 (measured at 150 °C), the rectifying ratio then reaches 10^{11} over the entire temperature range under study. Ruthenium contacts exhibit lower Schottky barrier, their forward voltage drop is thus lower (2.85V@J_F=1kA/cm^2@150 °C), but leakage increases rapidly with temperature. Platinum provides the highest Schottky barrier and guarantees the lowest level of the leakage (<10^{-8} A/cm^2). However, the diodes have poorer forward characteristics: their ideality factor and forward voltage is high (7.35V@J_F=1kA/cm^2@150 °C). Maximum realizable diode area and achievable breakdown field (0.8MV/cm) then depend on the number of crystal defects (namely threading dislocations) appearing in the diode low-doped drift region.

Keywords: diamond, Schottky diode, (113) orientation, molybdenum, platinum, ruthenium.

INTRODUCTION

Diamond has attracted considerable attention due to its unique material properties (large bandgap, high critical electric field, high thermal stability, high carrier mobility, and extremely high thermal conductivity), which makes it a candidate for future high-power devices capable of operating at extreme temperatures [1]. Due to its simplicity, the Schottky diode will likely be the first diamond commercial power component.

This device requires both the Schottky contact (with high blocking capability and low on-state resistance) and the highly conducting ohmic contact. In the case of the pseudo-vertical version of Schottky barrier diode (pVSBD) [1,2], which uses the more affordable insulating monocrystalline substrate coated by a heavily boron-doped p^{++} contact layer and then by a top low-doped p^- drift layer, both the ohmic and Schottky contacts are formed from above and, in principle, can be made by one metallic layer. This is because the top low-doped drift layer is removed at the point where ohmic contacts will be formed on the underlying p^{++} contact layer.

When designing a Schottky diode, it is necessary to optimize, in addition to the drift region, both contacts between the metal and the diamond. So far, (100) orientated diamond surface has been preferred [1-3] and several metals (aluminum [4], copper [5], gold [3], molybdenum [6], platinum [7], ruthenium [6], tungsten [3], and zirconium [8]) have been used to ensure sufficient and stable rectification characteristics.

In this contribution, we present the results of the development of pseudo-vertical Schottky barrier diodes realized on epitaxial boron-doped diamond layers with (113) orientation. This orientation offers an excellent trade-off between the surface morphology, epilayer roughness and electrical properties compared to (100) and (111) oriented boron doped diamond (BDD) layers [9]. pVSBD structures using different metals (molybdenum, ruthenium and platinum) to realize Schottky contacts were fabricated on an equivalent BDD bi-layer to eliminate the effect of the scatter in drift region parameters on diode characteristics. Diode forward and reverse characteristics were measured over a wide range of temperatures (30 to 180 ºC), then differences in diode behavior are analyzed and discussed.

EXPERIMENTAL

A cross-sectional view of the fabricated pVSBD is shown in Fig. 1. The active part of the pVSBD consisted from the homoepitaxial boron-doped diamond p^{++}/p^{-} bi-layer grown by a Microwave Plasma Enhanced Chemical Vapor Deposition (MWPECVD) system (AX5010 from Seki Diamond Systems) on (113) oriented insulating diamond substrate (see Fig.2). The substrate was produced from high-pressure high-temperature (HPHT) grown synthetic 0.5 carats Ib diamond crystal by polishing along the (113) crystalline plane using traditional scaife polishing techniques [9]. The first grown heavily boron-doped p^{++} contact layer (1.95 µm thick with boron concentration of 10^{21} cm^{-3}) was overgrown by a lightly doped p^{-} drift region (thickness 1.35 µm and boron concentration of about 10^{17} cm^{-3}).

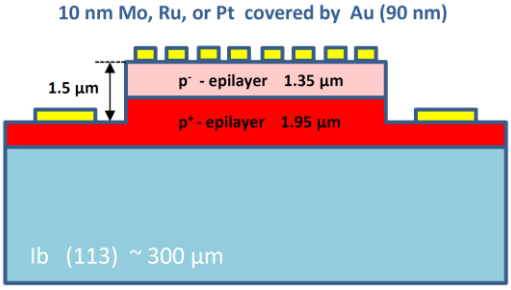

Fig.1 Cross sectional schematic view of the fabricated pseudo-vertical diamond Schottky barrier diode chip.

To realize the ohmic contact on the p^{++} contact layer, its outer part was etched away using a chromium hard mask covering the central part of the sample. Etching to a total depth of 1.5 µm was carried out by inductively coupled plasma using O_2 reactant gas (Oxford Instruments PlasmalabSystem 100). After etching, the sample was cleaned in hot KNO_3 + H_2SO_4 acid, placed in a hydrogen plasma at high temperature for 10 min to remove any remaining contamination, and, finally, the diamond surface was ozone treated to obtain a clean oxygen terminated surface. A 10 nm thick layer of Mo, Ru or Pt covered by a 100 nm thick Au capping layer was evaporated by an e-beam evaporation system (Leybold-Heraeus) to realize the Schottky contact of the diode. In the case of Mo and Ru, the same metallic bi-layer (single metallization) was used as the ohmic contact, while Ti/Au ohmic contact was used for Pt pVSBDs. After the deposition, circular (100 or 60 µm in diameter) Schottky contacts on the mesa and the ohmic contact ring on the p^{++} layer were defined using a laser lithography system (Microwriter ML) and wet chemical etch [10]. Top view of a typical realized diamond chip containing Ru pVSBDs is shown in Fig. 3.

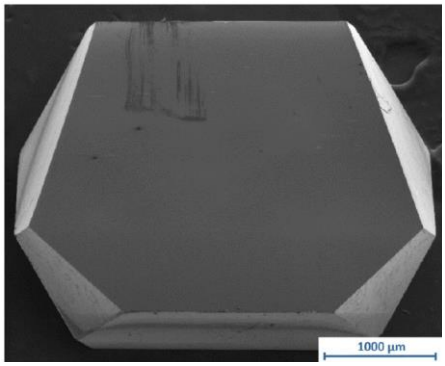

Fig.2 Low magnification SEM image of a (113) epitaxial boron-doped diamond layer deposited on HPHT grown Ib synthetic diamond crystal.

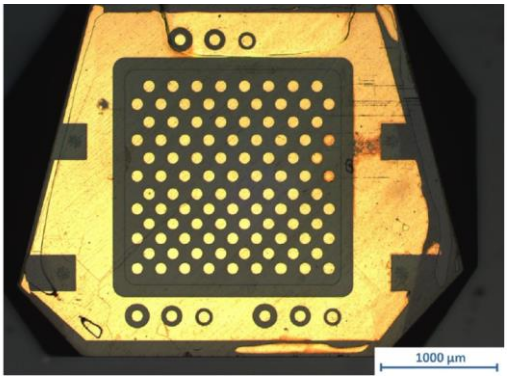

Fig.3 Top view on the diamond chip containing Ru/Au pVSBDs on the central mesa and the Ru/Au contact ring with c-TLM structures.

The four-point (Kelvin) method, a Cascade Microtech M150 probing system and an Agilent 4156C analyzer were used for the measurement of current to voltage (I-V) characteristics. The barrier of Schottky contacts was first stabilized by 20 min annealing at 300 ˚C and then forward and reverse I-V characteristics were recorded at temperatures ranging from room temperature to 180 °C. Contact resistances R_{Csp}, of the ohmic contacts were measured using the circular transfer length method (c-TLM) structures [11] located at the outer contact ring (see Fig.3).

RESULTS AND DISCUSSION

First, the quality of ohmic contacts on the contact p^{++} layer was investigated. Fig. 4 compares the measured values of the specific contact resistance R_{Csp} as a function of annealing temperature for all metallic systems used (Mo/Au, Ru/Au, and Ti/Au). The contacts were deposited on an ozone treated (113) homoepitaxial BDD layer with boron concentration of 8×10^{20} cm^{-3}. As mentioned in the experimental section, for Ru and Mo pVSBDs, the same metallization was used for the ohmic as for the Schottky contact. For Pt diodes, due to the higher work function (barrier) of the Pt contact, Ti/Au was used for an ohmic contact. As one can see, at very high boron concentrations, very low values of R_{Csp} (~10^{-6} Ω·cm^2) can be achieved for all types of contacts.

The as-deposited contacts show a very low specific contact resistance due to the tunneling of holes through the Schottky barrier from highly doped p^{++} contact layer. Increasing the annealing temperature gradually improves R_{Csp} and all contacts keep excellent quality up to 850 °C, at which we observed a significant degradation of the Au capping layer [11]. Fig.4 also shows that after annealing at 300 °C, which was used to stabilize the characteristics of the realized diodes, the specific contact resistance of all types of ohmic contacts should be more or less identical (~10^{-5} Ω·cm^2).

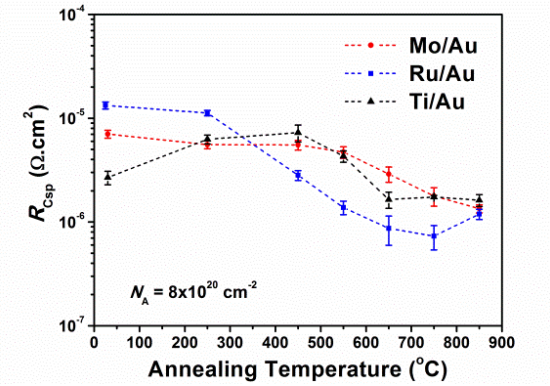

Fig.4 Annealing characteristics of Mo/Au, Ru/Au and Ti/Au contacts deposited on an ozone treated highly conductive (113) epitaxial BDD layer ($N_A = 8 \times 10^{20}$ cm^{-3}; ρ = 3 Ω·cm).

The quality of ohmic contacts on the contact p^{++} layer of the realized pVSBDs was compared after their stabilization by 20 minutes of annealing at 300 °C. Measurements made on c-TLM structures placed on the outer contact ring (see Fig. 3) showed the following values of the specific contact resistance: Mo/Au (R_{Csp} = 0.95 μΩ·cm^2), Ru/Au (R_{Csp} = 6.2 μΩ·cm^2), and Ti/Au (R_{Csp} = 17.8 μΩ·cm^2). This confirms that Mo and Ru can also be used to create a stable ohmic contact on heavily doped contact p^{++} layer.

Figs. 5-7 compare room temperature *I-V* characteristics of typical Mo, Ru, and Pt pVSBDs fabricated on equivalent BDD bi-layers recorded after 20 minutes annealing at 300 °C. The insets then show forward characteristics which were measured subsequently at temperatures ranging from 30 to 180 °C. Results show that all three metals can be used to realize Schottky diodes with sufficient forward and blocking capability. The characteristics of Mo and Ru pVSBDs are very similar. Both diodes were fabricated on equivalent BDD bi-layers and the maximal forward current densities thus achieve almost identical values. Due to the lower Schottky barrier of Ru, the built-in voltage of Ru diodes is lower V_{bi} = 1.40V compared to Mo pVSBDs V_{bi} = 1.65V. On the other hand, the forward *I-V* characteristics of Pt pVSBDs are significantly worse: the built-in voltage is high (~ 5.5 V) and the ideality factor *n* is far from one. This may be due to the high barrier of the Pt Schottky contact and its inhomogeneity.

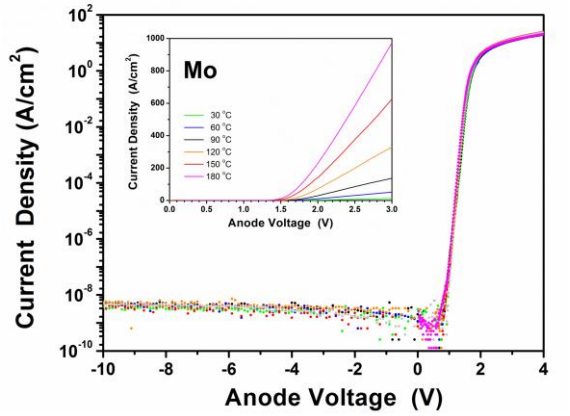

Fig.5 Room temperature I-V characteristics of pseudo-vertical Mo/Au Schottky diodes prepared on (113) oriented diamond. The temperature dependence of the forward characteristic of a typical diode is shown in the inset.

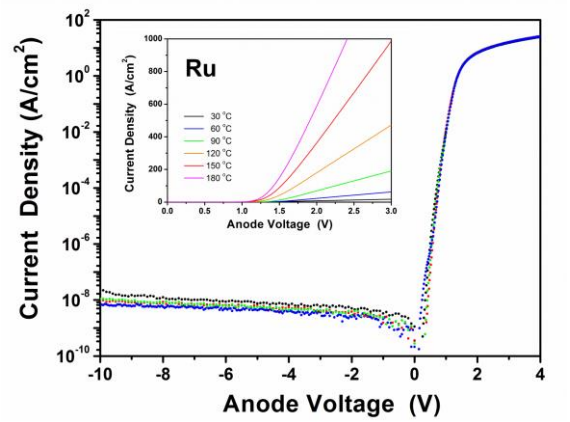

Fig.6 Room temperature I-V characteristics of pseudo-vertical Ru/Au Schottky diodes prepared on (113) oriented diamond. The temperature dependence of the forward characteristic of a typical diode is shown in the inset.

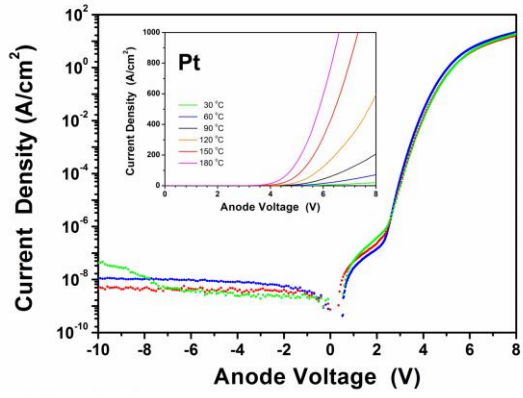

Fig.7 Room temperature I-V characteristics of pseudo-vertical Pt/Au Schottky diodes prepared on (113) oriented diamond. The temperature dependence of the forward characteristic of a typical diode is shown in the inset.

At room temperature, the reverse current of all measured diodes is close or below the resolution limit of our measuring station (10^{-15} A). This results in an excellent rectification ratio I_{ON}/I_{OFF} defined as the ratio of the diode current at V_F = 3 V (Mo and Ru diodes) or V_F = 8 V (Pt diodes) to that at V_R = 10 V. The room temperature I_{ON}/I_{OFF} value is of the order of 10^{10}, which is fully comparable to the values reported for the best Schottky diodes prepared on diamond with (100) orientation [6,8]. The reverse current of Mo and Pt pVSBDs increases only slightly with temperature and at 150 °C the reverse current density $J_R@V_R$ = 10 V is still of the order of 10^{-7} A/cm^2. As a result, the I_{ON}/I_{OFF} ratio of Mo and Pt pVSBDs increases with temperature. On the other hand, the leakage of Ru pVSBD increases rapidly with temperature due to the lower barrier of the Ru/Au Schottky junction.

The standard model for thermionic emission [1] of the current conduction including the influence of the diode specific on-resistance R_{on_sp} was used to extract values of the zero-bias Schottky barrier height Φ_{B0} and the ideality factor n, and to characterize the temperature behavior of fabricated pVSBDs:

$$J = J_S\left[e^{\frac{q(V-R_{on\_sp}J)}{nk_BT}} - 1\right] \qquad (1)$$

where n is the ideality factor, k_B is the Boltzmann constant and T is the temperature. The saturation current density J_S is given as

$$J_S = A^*T^2e^{-\frac{q\Phi_{B0}}{k_BT}} \qquad (2)$$

where A^* is the Richardson's constant. Using the theoretical value of A^* for holes in diamond (A^*=90 A·cm^{-2}K^{-2}), J_s, n, and R_{on_sp} values at different temperatures were determined by fitting of forward *I-V* characteristics. The values of J_s, n, and Φ_{B0} obtained are presented in Table I where we also included the values of the rectification ratio I_{ON}/I_{OFF} subtracted from the *I-V* characteristics. We can see that the ideality factor n

TABLE I
PARAMETERS OF PSEUDO-VERTICAL SCHOTTKY BARRIER DIODES WITH MO, RU, AND PT CONTACTS ON (113) ORIENTED BORON DOPED DIAMOND

Contact	J_S (A/cm^2)	n	Φ_B (eV)	I_{ON}/I_{OFF}
Mo 30 °C	1.1×10^{-21}	1.35	1.68	3×10^{10}
Mo 150 °C	4.8×10^{-14}	1.24	1.70	1×10^{11}
Ru 30 °C	1.6×10^{-15}	1.41	1.31	8×10^{9}
Ru 150 °C	2.9×10^{-9}	1.28	1.33	7×10^{5}
Pt 30 °C	8.0×10^{-16}	3.25	1.32	3×10^{9}
Pt 150 °C	2.8×10^{-13}	2.60	1.66	2×10^{11}

decreases with temperature while the Schottky barrier height Φ_{B0} increases for all types of contacts. This behavior is characteristic for SBDs realized on wide-bandgap semiconductors (SiC [12], GaN [13], and diamond [14]) and is due to inhomogeneity of the barrier height. This effect is the most pronounced for the diode with Pt contact which exhibits the worst forward *I-V* characteristic.

The room temperature specific on-resistance R_{on_sp} of our pVSBDs is relatively high (~ 90 mΩ.cm^2). This is due to incomplete ionization of the boron acceptors in the drift region. However, as temperature rises, it drops sharply to 1 mΩ.cm^2 at 180 °C. Fig.8 shows the temperature dependence of the hole concentration in the drift region of the Mo pVSBD, which was calculated from the values of R_{on_sp} (full boxes) established for different temperatures and the mobility data obtained on the equivalent p$^-$ epilayer [9]. The temperature dependence of the hole concentration

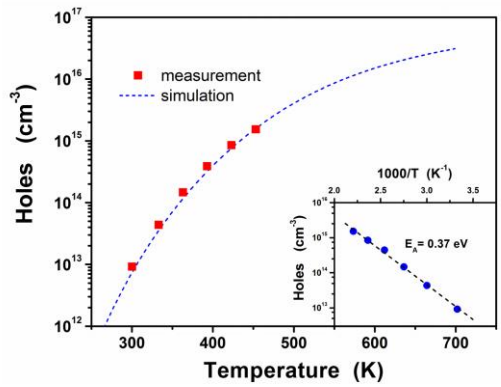

Fig.8 Measured (boxes) and simulated (dashed) temperature dependence of the concentration of holes in the drift region of a diamond pVSBD diode. The dependence on the reciprocal temperature then shows the boron acceptor's activation energy (inset).

in the diode drift region was fitted by the functional dependence, which assumes that the drift region is a non-degenerate p-type semiconductor containing an acceptor concentration N_A and compensating, fully ionized donors with a concentration N_D. The hole concentration p at temperature T was calculated using the relation [15]:

$$\frac{p(p+N_D)}{N_A-N_D-p} = \frac{2}{\beta}\left(\frac{2\pi m^*k_BT}{h^2}\right)^{3/2}e^{-\frac{E_A}{k_BT}} \qquad (3)$$

where β is the spin degeneracy of acceptors, m^* is the effective density of state hole mass and E_A is the acceptor ionization energy. The best fit of the measured data provided E_A = 0.37 eV, which agrees well with the boron activation energy in diamond [1], the acceptor concentration $N_A = 1.3 \times 10^{17}$ cm^{-3}, and the concentration of deep donors $N_D = 3 \times 10^{16}$ cm^{-3}. The donor compensation, which is due to residual contamination of the MWPECVD reactor, should be eliminated because it causes considerable uncertainty in setting the hole concentration in the drift region, which is critical for the proper operation of the diode.

In principle, Mo and Ru Schottky contacts can be operated up to 400 °C without substantial breaking of the oxygen termination of the diamond surface [6]. At

this temperature, it can be expected that the hole concentration in the drift region of our diodes will increase to 2.6 × 10^{16} cm^{-3}. At the same time, the mobility of holes drops to 115 $cm^2V^{-1}s^{-1}$ as determined by the Hall measurement on an equivalent p^- epilayer. Thus, at 400 °C, the R_{on_sp} of the drift region can be expected to fall below 100 $\mu\Omega.cm^2$, which is lower than the R_{on_sp} value of the pVSBD contact layer. Various improvements in the layout of the diode that decrease the distance between anode and cathode contacts can then be used to further reduce the ON-state resistance of the diode.

Room temperature reverse *I-V* characteristics of different Mo pVSBDs measured up to the point of diode destruction (breakdown) are shown in Fig.9 (bottom). As can be seen, the breakdown field of the diodes vary and its maximum 0.8MV/cm (diode G21) is far below the value expected for the diamond device. The breakdown (destruction of the diode) does not occur at the edge of the contact, where the highest electric field strength can be expected, but at various locations inside the contact. Evidence is provided by optical images of the anode contact taken before and after destruction (see the top of Fig. 9).

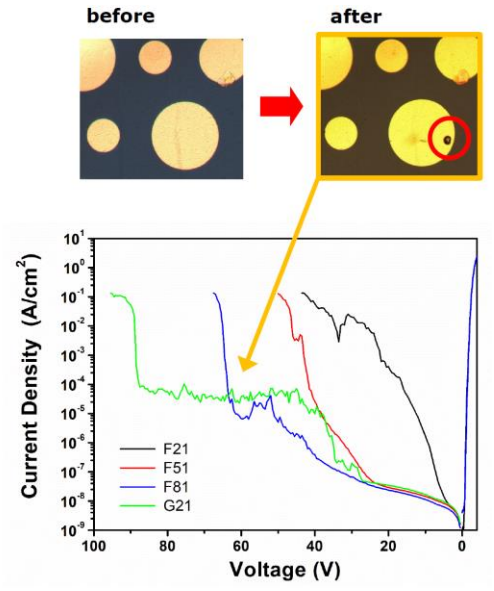

Fig.9 Room temperature reverse I-V characteristics of Mo pVSBDs measured up to the destruction/breakdown (bottom) and the optical image of the anode contact recorded prior to and after the destruction (top).

In general, the breakdown field of diamond Schottky diodes is degraded by number of defects (namely threading dislocations [16]) appearing in the MWPECVD grown low-doped p^- drift region. These defects cause a local increase in the reverse current, which can lead to charge carrier multiplication when the electric field increases with reverse bias. This is shown in the reverse *I-V* characteristics of diodes F51, F81, and G21 in Fig.9. Their characteristics have a regular shape at first, but after exceeding the reverse voltage of approx. 20 V a gradual uncontrolled increase of the leakage occurs, which is followed by a breakdown. High number of defects in the drift region leads to loss of blocking capability of the diode (G21). Fig.10 shows a detail SEM image of the mesa structure (taken before the metal deposition) of the diode chip with (the presented Ru pVSBDs) and without (not presented) blocking capability. On the right, one can register etch pits appearing in the p^+ contact layer after the removal of the p^- epilayer by oxygen plasma. The etch pits are connected with different types of crystal defects (threading and egde dislocations, stacking faults). In the bottom image, the etch pit density reaches a value of 10^8 cm^{-2} and none of the diodes realized on this chip showed blocking properties. The etch pit density corresponding to the top image was two orders of magnitude lower, but still did not guarantee the regular blocking characteristics of 100 µm diameter diodes. In summary, the reduction of crystal defects is necessary to achieve the expected breakdown voltages for larger devices.

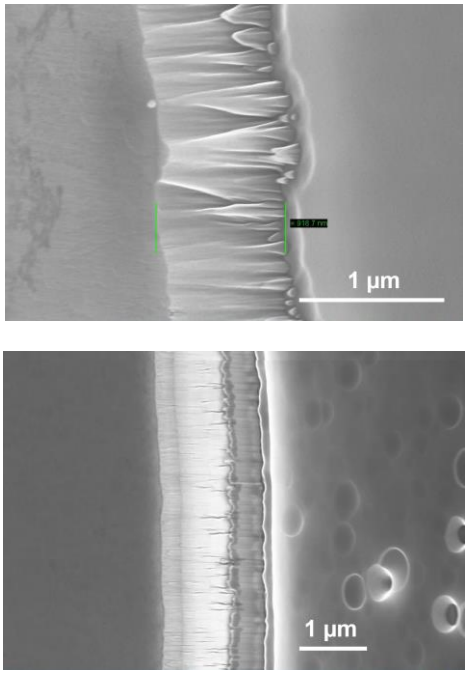

Fig.10 Detail SEM image of the mesa structure (taken before the metal deposition) of the diode chip with (top) and without (bottom) blocking capability. The top p^- layer is on the left, the edge of the mesa is in the middle, and the surface of the p^{++} layer exposed by oxygen plasma etching is on the right.

CONCLUSIONS

Mo, Ru, and Pt contacts covered by the gold capping layer were used for preparation of pseudo-vertical Schottky barrier diodes on (113) oriented homoepitaxial boron-doped diamond. Results show that all three metals can be used to realize Schottky diodes with sufficient forward and blocking capability. Moreover, molybdenum and ruthenium can also be used to

simultaneously create a stable ohmic contact on heavily doped contact p^{++} layer. Molybdenum provides optimum properties: a sufficient Schottky barrier height providing low leakage (< 10^{-8} A/cm^2) and an acceptable forward voltage drop of 3.80V@J_F=1kA/cm^2 at operation temperature of 150 °C. The rectifying ratio of Mo pVSBDs stays at 10^{11} over the entire temperature range from 30 to 180 ºC. pVSBDs with ruthenium contacts exhibit lower Schottky barrier, their forward voltage drop is thus lower (2.85V@J_F=1kA/cm^2@150 °C), but their leakage increases rapidly with temperature and rectification ratio drops to 7×10^5 at 150 °C. Platinum provides the highest Schottky barrier and guarantees the lowest level of the leakage (<10^{-8} A/cm^2). However, the diodes have poorer forward characteristics: their ideality factor and forward voltage is high (7.35V@J_F=1kA/cm^2 at 150 °C). The maximum achievable breakdown field (0.8MV/cm) of realized pVBDs is then given by the number of crystal defects (namely threading dislocations) in the low-doped drift region.

ACKNOWLEDGEMENTS

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Low forward voltage gate controllable diode for 6.5 kV HVDC application

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Abstract

Gate-Controllable Diode (GCD) allows charge carrier modulation at the anode region, by gate terminal biasing, to gain plasma control. This is used to achieve low-saturation mode and high-speed mode of the diode. Apart from the two operating modes, the anode side plasma control can also be utilised to desaturate the diode during commutation, to lower the overall switching losses. This paper is continuation work of earlier demonstrated GCD. The diode is designed as Si bi-polar power diode for 6.5 kV HVDC applications. In the current paper, a design consideration depending on various doping profiles of GCD was made. Thereby, a detailed study of switching behaviour with the switching pattern were conducted, to reduce the overall switching loss and improve the efficiency.

Keywords: Controllable diode, low-saturation, high-speed, desaturation, reverse recovery

Introduction

The diode is critical part in Modular Multilevel Converter (MMC) sub-module of a HVDC system, which is used as a free-wheeling diode (FWD) for the IGBT. A lot of research has been made towards improvement in the performance of the IGBT. To increase the overall efficiency of the total converter, the diode must compliment the IGBT. For 6.5 kV modules, a better performing Si pin-diode is required for free-wheeling application. Apart from improved efficiency, a FWD must have a soft turnoff during reverse recovery, better over current and over voltage peak, better performance at low current and low temperature.

Typically, in an HVDC system the inverter and rectifier operations demand different diode characteristics to have better efficiency. Switching losses dominate the high side diode operation in both rectifier and inverter mode, whereas conduction losses dominate the low side diode in rectifier mode and switching losses on the low side diode during inverter mode. To improve the overall converter performance, a low on-state voltage diode must be equipped as FWD on low side of the rectifier. A high-speed diode must be equipped on the high side of the rectifier, and on both high side and low side of the inverter. This requirement demands two separate characteristic pin-diodes which can be adapted to achieve both low-saturation and high-speed mode or a single controllable diode. This requires reducing the on-state voltage drop, meanwhile lowering the switching losses as well.

Although various controllable diode ideas have been studied before, literature [1],[2], exhibit a planar gate approach where it gets difficult to lead the diode to low forward voltage behaviour, hence not suitable for above mentioned requirement. Paper [3] demonstrates a difficult diode design for realization in practicality. Previously a gate controllable diode [4], was proposed based on submicrometric trench technology similar to literature from [5],[6], which is a robust technology and enables efficient on-state and commutation behaviour.

Controlling charge carriers on the anode side by variation in gate potential allows the operation of low-saturation and high-speed modes, as discussed in [4]. This is helpful in defining the diode operations on high side and low side of the MMC submodule. The aim of this paper is

to further improve the properties, by realizing even lower on-state voltage drop, and optimize switching losses of GCD. A Sentaurus TCAD based, numerical device level simulation of GCD is demonstrated in this paper.

Design considerations of new GCD

The p-n junction of the diode is parallel to the MOS channel area, which will be created beside the oxide of the gate in the vertical direction. With the positive potential, less than V_{bi} or with a negative potential applied to the gate, channel remains closed, and the diode behaves as a normal pin-diode. To reduce the on-state voltage of GCD from [4], the doping of p^+ layer is increased to a higher value of 1e18 cm^{-3} from the earlier value of 5e16 cm^{-3}. Instead of a flat charge carrier profile of [4], this creates a negative gradient of charge carrier density. Typically, with negative potential on gate, an enhancement of charge carriers from the highly doped p^+ layer is seen increasing the plasma on the anode side, leading to low-saturation mode.

Increasing V_{GA} to a positive potential, an electron channel is induced beside the oxide layer, creating a current path parallel to the p-n junction. By keeping the resistance components of this current path lower than set-in voltage, p-n junction is nearly shorted allowing external current to flow. To have a wide spread of plasma range between the low-saturation mode and high-speed mode, an additional high doped thin n^+ layer or n-buffer layer of doping 2.5e17 cm^{-3} is added beneath the p^+ layer, which is kept under the influence of the gate trench. The n-buffer layer lays a small resistance, thus, increasing the electron current and decreasing injection efficiency as described by the Eq. 1 [7]. Applied positive potential, doping of p^+ layer and n-buffer define the anode emitter efficiency and hence the plasma associated with the anode side. Therefore, the diode could be operated either in bi-polar mode with lower plasma on the anode side, or in the uni-polar mode like a MOSFET.

$$\gamma = 1 - \frac{j_n}{j} \qquad \text{Eq. 1}$$

Homogeneous approach

Fig. 1, gives a schematic representation of modified GCD, similar to the design from [4]. A submicrometric trench structure is designed with a mesa width of 0.4 µm (X_{MOS}) and a carefully selected mesa width to cell pitch ratio as in [8]. The model is simulated as a 4-cell model with an X_{MAX} of 6 µm. A 1.5 µm thick p^+ anode region and a 2 µm thick n-buffer region was realised into the sub-µm mesas between the trench gates. A homogeneous doping is maintained at the anode side. A very thin, highly doped p^+ layer is formed near the anode contact to make the region low ohmic. A 0.5 µm n^+ cathode layer of doping density 5e17 cm^{-3} is diffused into the n^- intrinsic base region, along with the field stop layer.

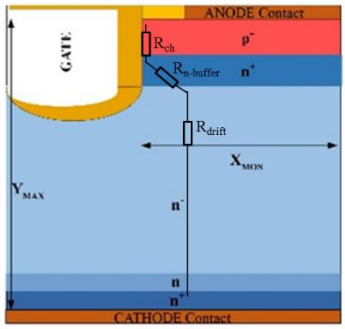

Fig. 1. Schematic cross section of a single cell homogeneous gate controllable diode.

Inhomogeneous approach

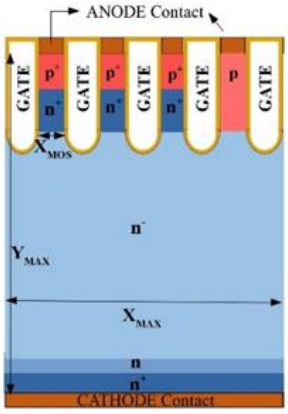

Fig. 2. Schematic cross section of a four cell inhomogeneous gate controllable diode.

A second approach to the design is considered with inhomogeneous doping in the cell level as shown in Fig. 2. The doping of p^+ layer and n-buffer layer, of the left part of the three cells are kept like the homogeneous model, whereas the right-side single cell's p layer doping is reduced to 6e16 cm^{-3} with a thickness of 4 µm and the n-buffer layer is removed. The ratio between high doped cells and low doped cell is kept in the

order of 3/1 for a total X_{MAX} of 6 µm. The principle remains similar to homogeneous approach, except for the right cell, where a free path for holes is created. Static on-state characteristics of homogeneous and inhomogeneous GCD compared with reference pin-diode is shown in Fig. 3 and corresponding charge carrier distribution is shown in Fig. 4.

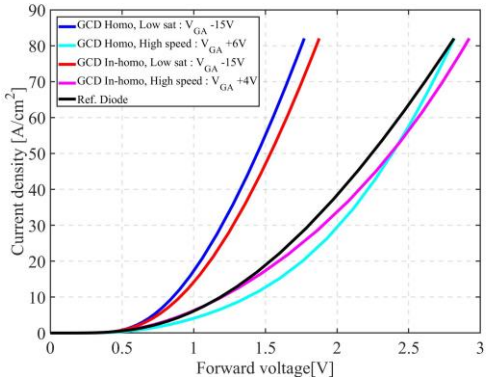

Fig. 3. Static on-state characteristics of homogeneous and inhomogeneous GCD at low-saturation and high-speed modes compared with reference diode. j_{nom} = 82 A/cm^2, T = 150 °C.

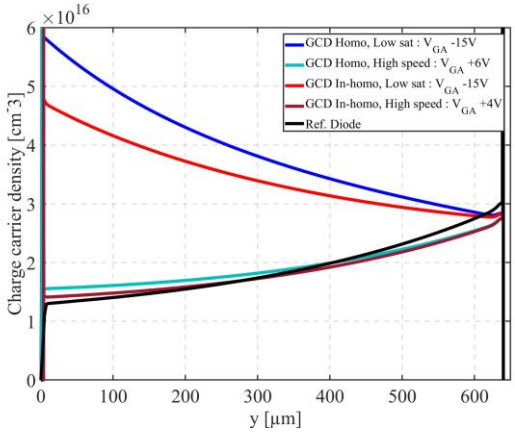

Fig. 4. Charge carrier density across the cross-section of homogeneous and inhomogeneous GCD at low-saturation and high-speed modes compared with reference diode under static condition. j_{nom} = 82 A/cm^2, T = 150 °C.

With the closed channel, at V_{GA} -15 V, anode terminal is flooded with charge carriers leading to lower on-state voltage drop of 1.8 V for homogeneous GCD and 1.85 V for inhomogeneous GCD. Auger recombination limits the reduction of forward voltage lower than 1.5-1.6 V for 6.5 kV device. With controlled anode injection efficiency, at a slightly low positive gate voltage of V_{GA} +6 V for homogeneous GCD and V_{GA} +4 V for inhomogeneous GCD, the charge carriers are brought to level equivalent to the reference pin-diode, which operates as high-speed mode with on-state voltage around 2.8-2.9 V. In this case, the current is established by both diffusion and drift current.

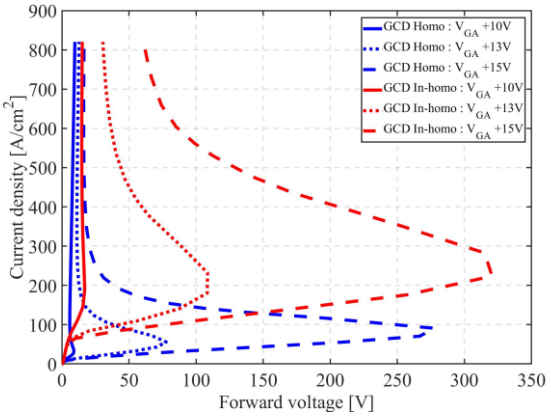

Fig. 5. Static on-state characteristics of homogeneous and inhomogeneous GCD. j_{nom} = 410 A/cm^2, T = 150 °C.

In the homogeneous approach, at higher gate voltages, for forward current densities lower than critical current, a MOSFET kind of behaviour is triggered. This leads to majority carrier mode and anode current mainly constitutes electron current with injection of holes being stopped. The current (I_{crit}) is determined by the resistance offered by the channel and the n-buffer (refer Fig. 1), which is given by Eq. 2 [9]. A snap back in the voltage is observed. In the inhomogeneous approach, due to opening of a path for holes to flow, a bi-polar behaviour prevails until twice the nominal current density, avoiding a snap back during nominal operating condition. Due to low doping concentration and smaller area distribution of the low doped p-region, snap back occurs at higher current densities. Fig. 5, shows the behaviour of homogeneous and inhomogeneous GCD at 5*j_{nom}, and higher gate voltages, +10 V, +13V, +15V.

$$I_{crit} = {V_{bi}}/{(R_{ch} + R_{n-buffer})} \qquad \text{Eq. 2}$$

Blocking behaviour of new GCD

The thickness (Y_{MAX}) of the model and doping concentration of the drift region is designed to handle a reverse blocking voltage of 6.5 kV. The static blocking characteristics of homogeneous and inhomogeneous GCD is simulated at 150 °C as shown in Fig. 6, where

the diode is seen to block the nominal blocking voltage of 6.5 kV.

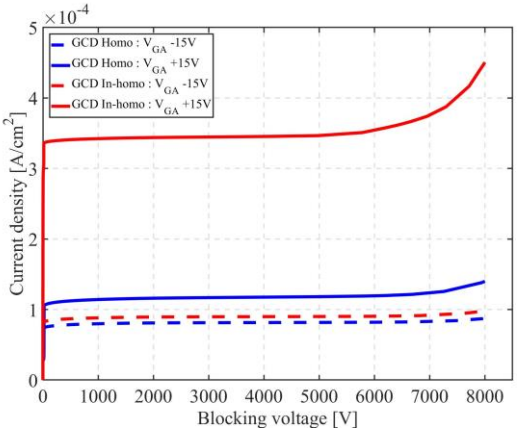

Fig. 6. Static blocking simulation of 6.5 kV homogeneous and inhomogeneous GCD, T = 150 °C.

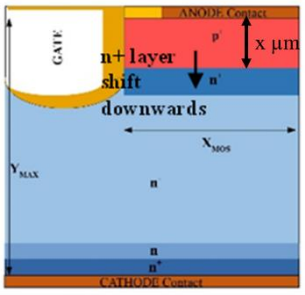

Fig. 7. Schematic cross section of a single cell GCD with n-buffer layer shift downwards by 'x' µm.

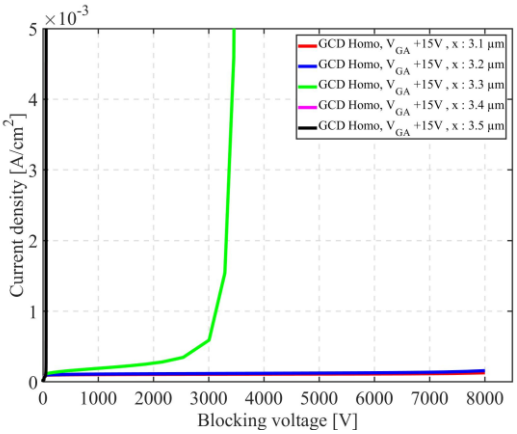

Fig. 8. Static blocking simulation of 6.5 kV homogeneous GCD dependent on 'x', T = 150 °C.

The placement of n-buffer layer underneath the p^+ layer has an influence on the blocking capability of the diode [7]. Fig. 7, shows the shift of n-buffer layer downwards by 'x' µm from the anode contact. This shift was simulated for both homogeneous and inhomogeneous GCDs. It is observed, if the n-buffer layer is placed out of the trench, i.e., when the peak doping concentration of n-buffer layer is outside the influence of the gate terminal, the current flows to the anode contact with loss of the 6.5 kV blocking capability. Fig. 8 and 9, show the static blocking characteristics of homogeneous and inhomogeneous GCDs respectively, at 150 °C for various 'x' from 3.1 µm to 3.5 µm. At 3.3 µm, homogeneous diode blocks only 3 kV, whereas inhomogeneous diode blocks almost 6 kV. Both the diodes, block only several 100 V past 3.4 µm.

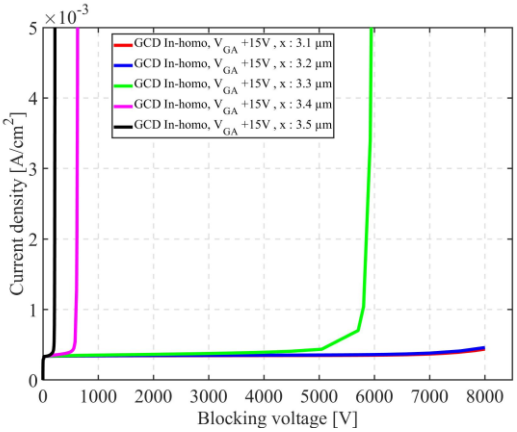

Fig. 9. Static blocking simulation of 6.5 kV inhomogeneous GCD dependent on 'x', T = 150 °C.

Dynamic behaviour

Low-saturation mode diode produces higher switching losses due to the amount of charge carriers and high-speed mode is equivalent to the reference diode. Significant improvement from the reference diode is only seen when the switching losses are reduced. Implementing the desaturation pulse concept described in [4], switching losses are reduced effectively, increasing the overall efficiency of the network.

Fig. 10 shows the static charge carrier distribution, taken across the cutline in y-direction at various V_{GA} for inhomogeneous device, simulated at nominal current density. Plasma on the anode side at V_{GA} +10 V has reached a low point in bi-polar operation with high voltage drop of around 7 V. A slightly higher V_{GA} of +13 V is used in the duration 'tdsat', during commutation. The doping of the GCD is set in such a way as to achieve a uni-polar characteristics at V_{GA} +15V, for study purpose. This approach of doping could be modified for practical applications.

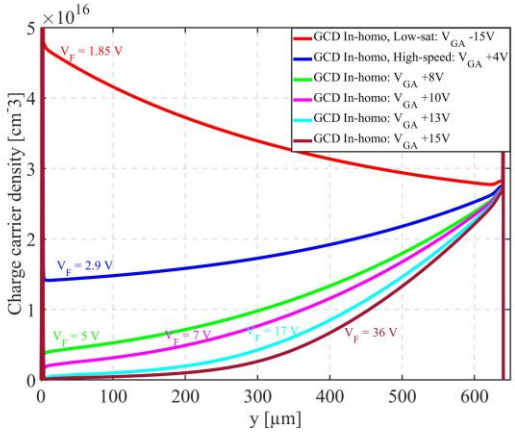

Fig. 10. Charge carrier density across the cross-section of inhomogeneous GCD at varying V_{GA}. j_{nom} = 82 A /cm^2, T = 150 °C.

It is to be noted that, the gate drive for such diodes gets complex. For HVDC applications with 150 Hz switching frequency, a gate drive demanding such desaturation times could be implemented with PWM controller. But for the gate drivers using hysteresis controller, the desaturation time is limited by shorter duration within the order of 20 µs.

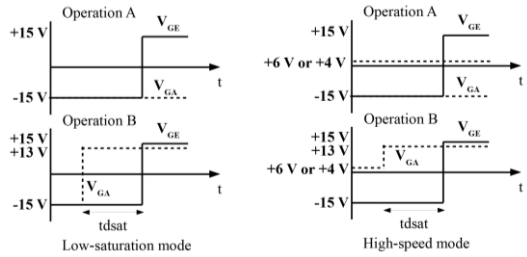

Fig. 11. GCD and IGBT, gate drive condition.

To understand the control strategy of the GCD and to reduce the overall losses, the driving condition of both diode and IGBT are considered as shown in Fig. 11. Operation A shows switching of IGBT alone from -15 V to +15 V, without any control of GCD. Operation B shows how the tdsat is applied for GCD while switching between conducting state (V_{GA} -15 V, +6 V or +4 V) to desaturation state (V_{GA} +13 V). Dynamic behaviour of GCD and IGBT were obtained with a boost circuit configuration. The simulations are performed for a nominal current density of 82 A/cm^2, a DC-link voltage of 3.6 kV, with a stray inductance of 1.6 µH, at a temperature of 150 °C. A 6.5 kV submicrometric trench IGBT was used similar to a model scaled from [4],[5],[8], where IGBT was simulated for half the current density of the diode. For standardization under nominal switching condition, the peak power on single diode was kept at a maximum of 150 kW.

Due to effects of recombination, diode takes at least 10 µs [7] to start reducing the reverse recovery charge during commutation. With introduction of tdsat, the switching time difference between IGBT and GCD, overall turn on losses reduces by a great margin. As seen from [4], operation A produced slowest dj_F/dt with highest switching loss on both IGBT and GCD, as there is not enough time for plasma desaturation. With increasing tdsat, we notice the loss reduction on both diode and IGBT.

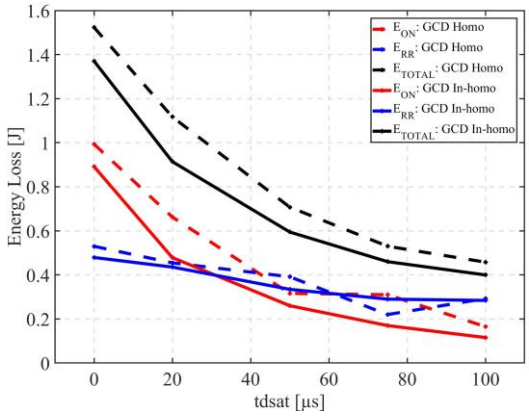

Fig. 12. Overall turn on loss comparison of low-saturation mode, distinguishing homogeneous and inhomogeneous GCD's E_{RR}, E_{ON}, E_{TOTAL} for tdsat= 0µs, 20µs, 50µs, 75µs, 100µs. V_{DC} = 3.6 kV, j_{nom} = 82 A/cm^2, T = 150 °C, L_S = 1.6µH, P_{RR} = 150 kW.

Fig. 12. shows the energy loss reduction (E_{TOTAL}, E_{ON}, E_{RR}) dependency on tdsat in low-saturation mode, for both homogeneous and inhomogeneous GCD. As the static I-V characteristics of homogeneous and inhomogeneous GCD is kept similar, their loss profile appears similar. A 70 % overall reduction in loss is observed between 0 µs and 100 µs. For a 6.5 kV voltage class bi-polar device, irrespective of IGBT or diode, the desaturation time required for optimal loss reduction is about 50-100 µs.

Similarly, Fig. 13, shows the tdsat dependency of loss reduction on both homogeneous and

inhomogeneous diode in high-speed mode. The stored charge during conduction in high-speed mode is considerably less than in the low-saturation mode, which is reflected in loss distribution at 0 µs, with around half the losses of low-saturation mode. Even in high-speed mode, loss reduction is observed with increasing tdsat, though not as significant as in low-saturation mode. With tdsat application, round about 50 % reduction in overall losses in noted in both homogeneous and inhomogeneous diode in high-speed mode.

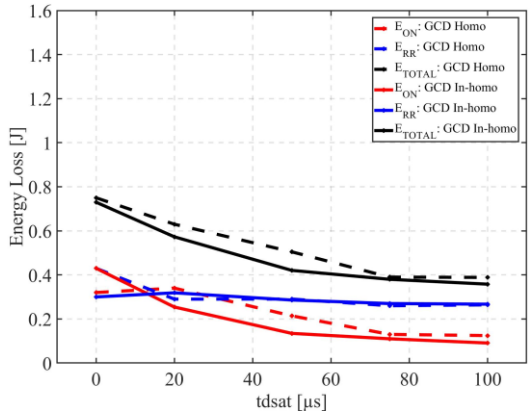

Fig. 13. Overall turn on loss comparisonin of high-speed mode, distinguishing homogeneous and inhomogeneous GCD's E_{RR}, E_{ON}, E_{TOTAL} for tdsat= 0µs, 20µs, 50µs, 75µs, 100µs. V_{DC} = 3.6 kV, j_{nom} = 82 A/cm^2, T = 150 °C, L_S = 1.6µH, P_{RR} = 150 kW.

It is noted that after tdsat of 50 µs, the reverse recovery losses of diode saturate, but losses on IGBT keeps lowering. To keep better softness of diode during turn-off, the charge carriers on the cathode side is kept high like in a reference diode. There is no control on cathode to remove this stored charge. Irrespective of any tdsat application, the cathode side plasma cannot be reduced further, and this is reflected on E_{RR} curve which stagnates around 0.3 J. A similar behaviour is observed in low-saturation mode. After about 75 µs, E_{RR} saturates around 0.3 J and loss reduction occurs only on the IGBT.

The characteristics of GCD at higher positive V_{GA} and longer tdsat pulse range has a negative influence on the dj_F/dt. From the Fig. 10, we notice the GCD at V_{GA} +15 V, runs into uni-polar mode with a high forward voltage drop. It is observed that during uni-polar mode, with application of longer tdsat times, dj_F/dt increases to high value reducing only the losses on IGBT drastically with minimal change in Q_{RR}. Fig. 14, shows variation in dj_F/dt and effect on Q_{RR} and E_{ON} for different gate drive conditions in low-saturation mode of inhomogeneous GCD. The last points on the right of the figure shows high dj_F/dt, in the order of 300 A/µs. The driving conditions for the three scenarios are higher tdsat and higher V_{GA}. The driving condition with either higher tdsat of 150 µs at V_{GA} +10 V or 100 µs at V_{GA} +13 V have a moderate dj_F/dt, and loss reduction is in the similar range of extreme dj_F/dt cases. Both homogeneous and inhomogeneous GCD behaves the same way. To infer from this, application of longer tdsat time in uni-polar mode of GCD must be avoided.

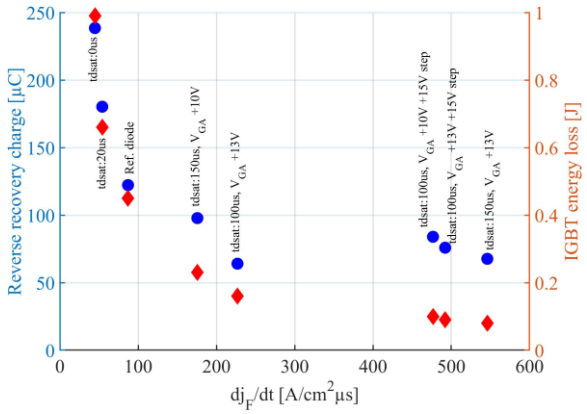

Fig. 14. dj_F/dt vs Q_{RR} vs Losses comparison of inhomogeneous GCD in low-saturation mode at different driving condition. V_{DC} = 3.6 kV, j_{nom} = 82 A/cm^2, T = 150 °C, L_S = 1.6µH, P_{RR} = 150 kW.

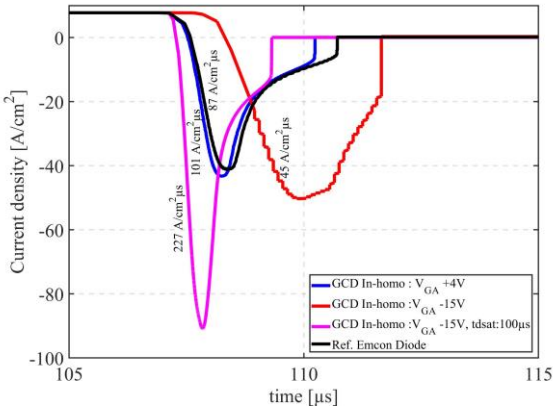

Fig. 15. Reverse recovery behaviour of inhomogeneous GCD, L_S = 1.6 µH, V_{DC} = 4.5 kV, j_{nom} = 8 A/cm^2, T = 25 °C.

As seen from the charge carrier density in Fig. 10, GCD at V_{GA} -15 V is designed for -dn/dx. This will lead to a snappy reverse recovery

behaviour. This is evident from the Fig. 15, where simulated reverse recovery waveforms are shown at 0.1*j_{nom} at 25 °C. The reverse recovery waveforms for GCD at V_{GA} +4 V or GCD V_{GA} -15V with 100 µs tdsat shows a soft turn-off behaviour like the reference diode.

The influence of changing diode current on tdsat was studied in previous paper, the same analysis can be extended in this case. Robustness of the submicrometric trench, in terms of shielding the electric field from reaching anode contact was also shown in paper [4]. The effect of p-cathode for ease of holes extraction, its effect on softness and the GCD short-circuit dependency was also studied in previous paper.

Conclusion

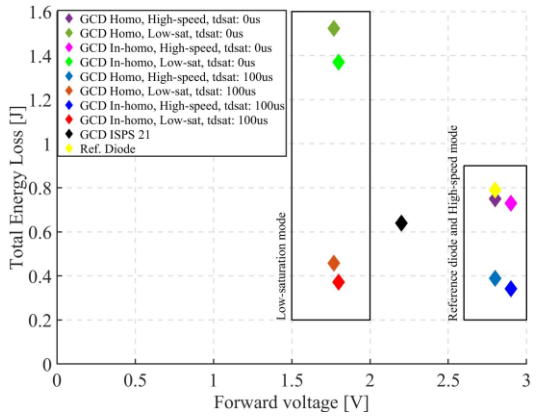

Fig. 16. Trade-off behaviour of homogeneous and inhomogeneous GCD, V_{DC} = 3.6 kV, j_{nom} = 82 A/cm^2, T = 150 °C.

A gate controllable diode concept was proposed in the previous paper. The static and dynamic characteristics of GCD is further improved in this paper, which can be seen from trade-off curve shown in Fig. 16. Along with that, the effects of n-buffer and inhomogeneity in doping of GCD were studied. Desired low-saturation mode and high-speed mode were established for an efficient operation of MMC sub-module in 6.5 kV HVDC system. It can be seen; a massive 70 % reduction of overall losses is seen in low-saturation mode. Around 50 % reduction in losses is seen in high-speed mode. This holds good wrt., reference diode as well, because both high-speed mode and reference diode have similar characteristics. Thus, a low forward voltage diode is designed, and homogeneous and inhomogeneous GCD is established.

Acknowledgments

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High-Voltage Thyristors with Enhanced Dynamic Robustness

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Abstract

Two cathode design concepts of phase control thyristor (PCT) are compared for 6.5 kV class in the housing with 47mm pole piece (5STP 08F6500). For the same technology curve V_T-Q_{rr}, the achievement of different combination of dynamic parameters like commutation turn-off time t_q, dV/dt and di/dt capability are discussed. This work expands the know-how on the cathode emitter engineering previously presented for 1.8, 2.8 and 8.5 kV voltage classes.

Keywords: PCT, high-voltage thyristors, dynamic parameters, dynamic robustness

INTRODUCTION

As the device with the lowest ON-state losses from all available switching concepts, thyristors maintain their application importance by providing cost efficiency in energy saving technologies of high societal impact. More specifically, high-power hockey puck types, discussed in this paper, are expected to show the compound annual growth rate (CAGR) about 3 % till 2030. Continuous improvement and cost reduction of silicon technology provide new opportunities for further improvement, especially in the high-voltage classes like that of 6.5 kV class demonstrated below.

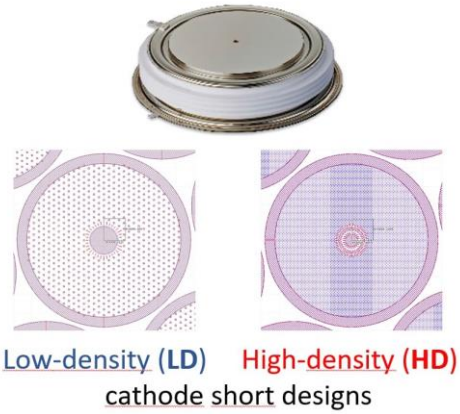

Fig. 1 Device under test: 5STP 08F6500 rated to V_{DRM} = 6.5 kV, I_{TAVmax} = 850 A. Two cathode designs: low-density (LD) and high-density (HD) cathode short pattern.

The aim of this paper is to show that one can further improve device ratings using improved technology means, like for example the better resolution of photolithography for masking the fine cathode shorting pattern. The dimension of the shorts can be significantly reduced while their density can be increased at the same time. The resulting device performance can change beyond the usual know-how and relevant electrical parameters can be improved. Last, but not least, some processing steps could be omitted, and production cost reduced.

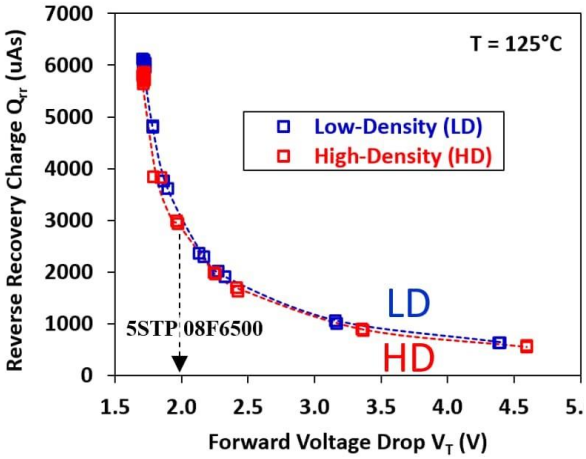

Fig. 2 Technology curve V_T-Q_{rr} for LD and HD designs. Individual doses of electron irradiation are equal for both designs. V_T-Q_{rr} point for existing product 5STP 08F6500 is highlighted.

EXPERIMENTAL RESULTS AND DISCUSSION

Phase Control Thyristors of 6.5 kV class for housings with the pole piece diameter of 47 mm were produced using classical low-density (LD) and high-density (HD) cathode shorting pattern. The distance between shorts for the HD design was reduced 3 to 4 times (Fig. 1). The doses of electron irradiation were chosen to carry out the points at the technology curve Q_{rr}-V_T which expand the range of possible variants over that of the standard product 5STP 08F6500 with the aim to cover all possible power electronics applications (Fig. 2). In spite of higher consumption of cathode area by cathode shorts of the HD design, the technology curves Q_{rr}-V_T are identical. The effect of denser shorts of the HD design manifests itself only in a slightly lower Q_{rr} for the same irradiation

dose – see the distance between the individual points on Fig. 2. Contrary to the low-voltage PCTs, the HD design of the 6.5 kV class cannot be used to control the Q_{rr} without the usage of electron irradiation (EI) similarly to the 8.5 kV class presented in [1]. As will be shown below, some relevant dynamic parameters can still be improved.

Fig. 3 shows the dependence of the circuit-commutated turn-off time t_q on the dose of EI. The t_q was measured at T_{jmax} = 125 °C from the ON-state current of 2 kA with di/dt = –1.5 A/µs, and V_R = 200 V according to the industrial standard up to 0.67×V_{DRM} = 4.4 kV with dV_D/dt = 20 V/µs. While the LD design requires a reasonable dose of EI to satisfy the datasheet specification, the HD design provides sufficiently low t_q already on as-processed wafers.

The t_q of the HD devices is reduced to less than 50 % and this trend holds up to relatively high V_T. Moreover, the sensitivity of t_q on the EI is much lower with the HD design. The efficiency of the HD design is also manifested by much better trade-off curve between the turn-off time t_q and ON-state voltage V_T as presented in Fig. 4. We do not need to sacrifice the low magnitudes of V_T to achieve good dynamic parameters.

Also, the critical rate of rise of the forward blocking voltage (dV/dt capability) is improved using the HD devices. It is illustrated on Fig. 5 for the dV/dt test up to the full blocking voltage V_D = 6500 V, where dV/dt is shown nearly doubled for the HD design in the full range of EI doses. This is in a good agreement with the testing of t_q above, where dV/dt test is part of the t_q test. The dV/dt capability of industrial thyristors is usually specified for 0.67×V_{DRM} = 4.4 kV likewise the t_q. For this condition, both designs reached the limit of our tester. Consequently, we have chosen harder test conditions up to full V_D to show the strength of the HD design.

The penalty for the improved t_q and dV/dt can be found in the reduced critical rate of rise of the ON-state current di/dt (di/dt capability) measured at frequency of 1 Hz as shown in Fig. 6. The LD design passed the 4× nominal magnitude of standard product representing the limit of our tester (4 kA/µs). On the other hand, the HD design has been found to reach di/dt = 2.5 kA/µs, which is 2.5× the requested datasheet value. This means that the di/dt margin has been reduced at HD design. This result follows the general relation between the thyristors with easier triggering and higher di/dt capability and the ones with protracted triggering and higher dV/dt capability and

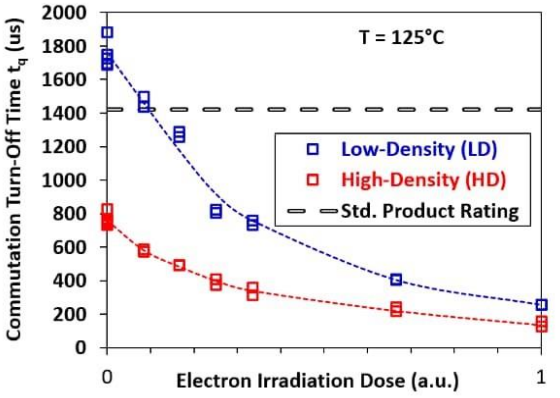

Fig. 3 Commutation turn-off time t_q vs. electron irradiation dose. Measured at T = 125 °C. The horizontal dashed line shows the datasheet limit.

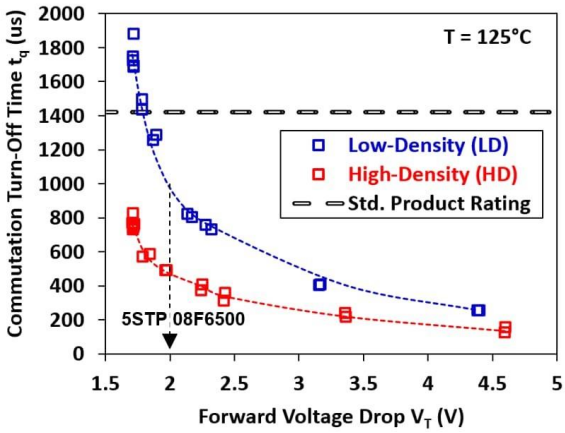

Fig. 4 Commutation turn-off time t_q vs. ON-state voltage V_T. V_T was measured at I_T = 1 kA and T = 125 °C. The horizontal dashed line shows the datasheet limit.

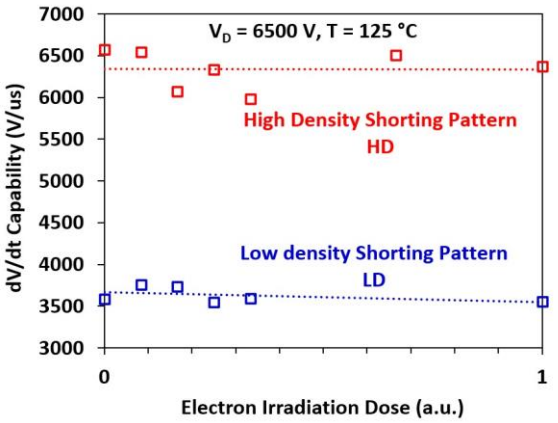

Fig. 5 dV/dt capability measured up to full blocking voltage V_D = 6.5 kV vs. electron irradiation dose at T = 125 °C.

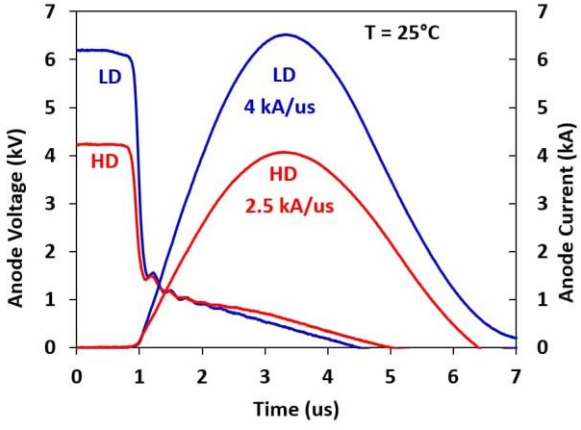

Fig. 6 di/dt capability measured at room temperature and frequency of f = 1 Hz.

lower commutation turn-off time t_q. Further improvement of the di/dt capability of the HD design would require a further optimization of the gatecathode structure.

The difference between the LD and HD designs manifests itself in significantly different static IV curves at low currents. This difference is illustrated for two device designs on devices with the same ON-state voltage V_T at 125 °C in Figs. 7 and 8. The close proximity of cathode shorts bringing the high dV/dt and t_q increases the ON-state voltage V_T at low currents and low operation temperature. Consequently, the crossing point current of the HD design is increased by 35 %.

It has been shown that the electron irradiation changes the crossing point current of P-i-N diodes in a complex way [2, 3]. At very low electron irradiation doses, the crossing point current is lowered compared to the unirradiated diode. From certain dose level, the crossing point current grows to disappear at high doses. The dependence of the crossing point current vs. electron irradiation dose of P-i-N diode is therefore U shaped [3]. We can see similar U shape dependence for the thyristor LD design (Conventional) in Fig. 9. However, for the HD thyristor design, the U shape is missing. The local minimum of the crossing point current is replaced by the region of constant crossing point current which is

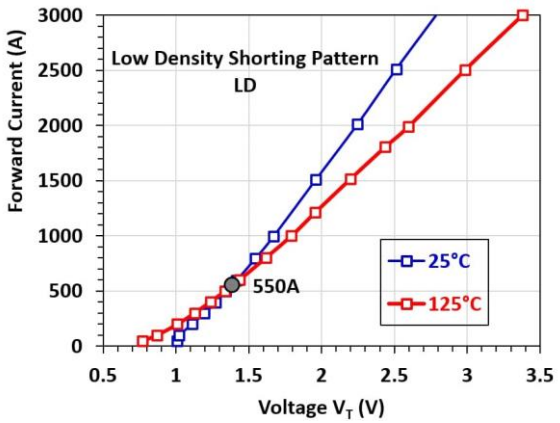

Fig. 7 Forward IV curves of LD design at 25 °C and 125 °C for the device with V_T = 1.8 V, dV/dt = 3.5 kV/µs, t_q = 1500 µs.

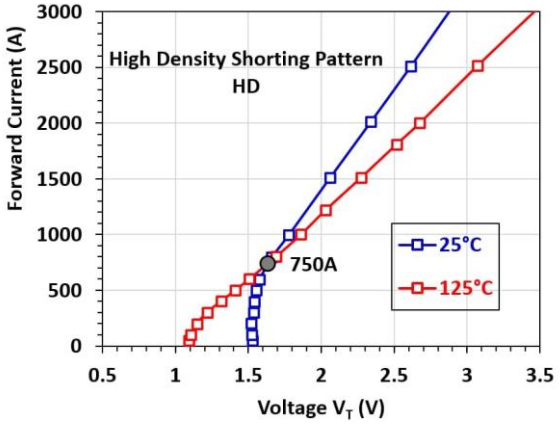

Fig. 8 Forward IV curves of HD design at 25 °C and 125 °C for the device with V_T = 1.8 V, dV/dt = 6.5 kV/µs, t_q = 600 µs.

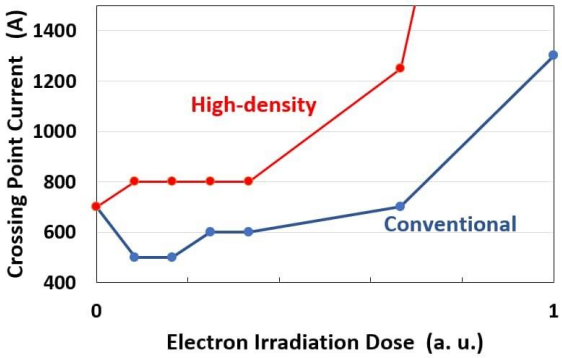

Fig. 9 Crossing point current between forward IV curves vs. electron irradiation dose. Measured at 25 °C and 125 °C for the LD and HD designs.

followed by steep increase at higher doses of electron irradiation. The flat region takes place up to V_T = 2.5 V measured at I_T = 1 kA and T = 125 °C. As we can see in Fig. 5, such HD device shows t_q at about 300 µs. The same magnitude of t_q can be reached with the LD design only by using very high dose of electron irradiation, which results in V_T about 4.0 V measured at the same current and temperature. For this electron irradiation dose, the crossing point current of the HD design is increased only by 25 % over the LD design.

Consequently, by choosing an optimal dose of electron irradiation, one can minimize the drawback of the HD design, which is the higher crossing point current. Eventually, one can omit the electron irradiation of thyristors according to the HD design, if the t_q at about 800 µs is acceptable. The benefit of this choice is the magnitude of the crossing point current around the maximum average ON-state current I_{TAVmax} and reduced production cost [4].

SUMMARY

Two cathode designs of 6.5 kV industrial phase control thyristor with the low (LD) and high density (HD) of cathode shorts were presented with the aim to improve the device ratings and optionally reduce the production cost. The trade-off relations between Q_{rr} and V_T, t_q and V_T, and dV/dt and di/dt were demonstrated for the two distinct designs. While the trade-off curves Q_{rr} and V_T of both the designs are equal, the trade-off between the t_q and V_T shows significant improvement in favor of the HD design. The HD design shows the higher dV/dt capability and worse di/dt capability compared to the classical LD design.

Last, but not least, the increase of the crossing point current with increasing dose of electron irradiation shows much stronger dependence for the HD design. The advantage of the HD design is much lower electron irradiation dose needed for reduction of the commutation turn-off time t_q down to 300 µs and hereby negligibly increased ON-state voltage drop V_T compared to the LD

design. Eventually, the electron irradiation of the thyristor with the HD design can be skipped with the benefit of reduced production cost. Hereby the paper provides all information necessary for optimization of device design to satisfy specific conditions of different industrial applications.

ACKNOWLEDGEMENT

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Comparison of IGBT Junction Temperature Determination using an On-Chip Sensor and the $V_{CE}(T)$ Method

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Abstract

This paper investigates the factors responsible for the differences in the IGBT virtual junction temperature $T_{vj,max}$ determined using the established $V_{CE}(T)$ method and the temperature recorded using an on-chip temperature sensor (T_j sensor) mounted in the centre area of the IGBT chip. The impact of each of the influential factors are quantified using experimental and analytical methods. Increase in power loss density was found to cause an increase in the difference between the two temperatures at a rate of 2 Kelvin per W/mm² as per measurement results. The selection of the measurement delay was found to additionally contribute to the deviation between the estimated $T_{vj,max}$ by the two methods in the range of a few Kelvin. Furthermore, increase in thermal resistance contributes to an increase in the deviation. By adding several influential factors, an impact of up to 50% difference in power cycling lifetime estimation is possible depending upon the operating conditions.

Keywords: IGBT Junction Temperature, T_j sensor, Power Cycling, On-Chip temperature sensor.

INTRODUCTION

Accurately determining the IGBT junction temperature is an essential precondition for establishing an accurate load cycling lifetime model as well as for defining parameters such as those required for setting the over temperature protection function. The junction temperature of the IGBT (T_j) can be determined using several methods which chiefly fall under two major categories – indirect measurement and direct measurement. Indirect measurement methods refer to the utilization of temperature sensitive electrical parameters (TSEP) for estimating the junction temperature. Several TSEPs exist [1] and each TSEP presents an opportunity to estimate the IGBT junction temperature. The $V_{CE}(T)$ method [2] is one such indirect method which is standard for T_j estimation especially for the purpose of life time estimation. Direct T_j determination refers to methods where temperature as the input parameter is acquired directly from the IGBT chip. One such direct measurement method is to utilize an on-chip temperature sensor (T_j sensor) which is integrated in the centre area of the chip [3]. An example of one such IGBT chip is shown on Fig. 1.

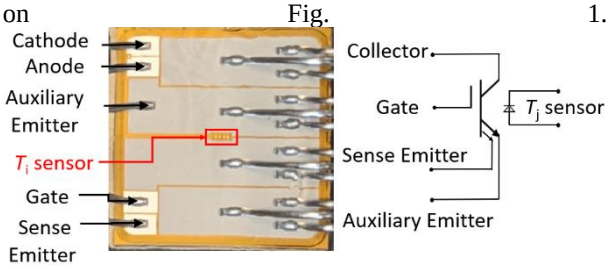

Figure 1: The IGBT die with the T_j sensor

As evident in the IR camera image in Fig. 2, when the IGBT chip (in healthy condition) conducts current, there is a lateral temperature gradient over the chip. The hotspot is located on the centre of the chip and the periphery is cooler. According to the automotive qualification guideline AQG324 the temperature registered using the $V_{CE}(T)$ method is the so-called virtual junction temperature (T_{vj}). In this paper, the maximum temperature determined through an on-chip sensing diode will be referred to as hotspot temperature $T_{hotspot}$ and the maximum temperature determined through $V_{CE}(T)$ method will be called maximum virtual junction temperature $T_{vj,max\text{-}VCE}$. The difference between the two is an indication of the overall temperature gradient on the chip and will be called $T_{difference}$.

$$T_{difference} = T_{hotspot} - T_{vj,max\text{-}VCE} \quad (1)$$

In this study, the experiments were conducted where either the thermal resistance from junction to ambient ($R_{th,j\text{-}a}$) was measured or the thermal resistance from junction to heatsink ($R_{th,j\text{-}s}$) was measured. The measured

quantities are described accordingly. Unless otherwise mentioned, the junction temperature for the thermal resistance measurement uses the standard $V_{CE}(T)$ method.

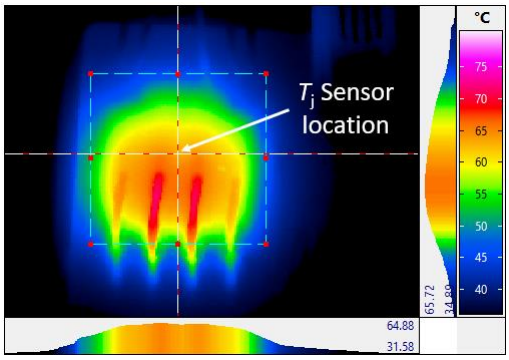

Figure 2: IR Camera image of the DUT. I_C = 100 A, ton = 5 s.

The typical profiles and location of these temperatures are shown in Fig. 3.

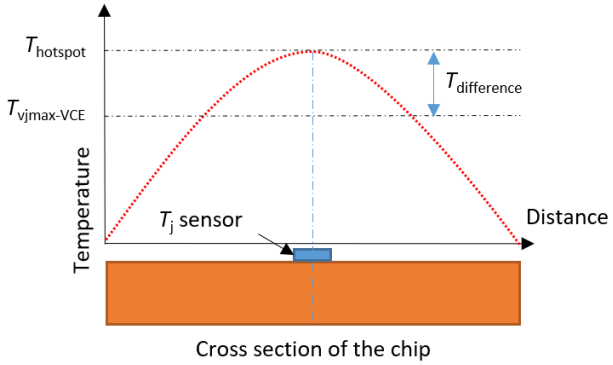

Figure 3: An example of the temperature profile over the chip

The study in [4] has analysed the suitability of the T_j sensor for determining the T_j during power cycling tests. This paper analyses the differences between the IGBT junction temperature established using the $V_{CE}(T)$ method and the T_j sensor method. The motivation is to understand the utility of the T_j sensor method as a means to achieve on-line monitoring of the T_j and to understand the impact of using the T_j sensor method in estimating load cycling lifetime. In power cycling tests, the maximum virtual junction temperature is measured using a TSEP method such as the $V_{CE}(T)$ method and is considered as an important stressing factor. However, the sensing diode integrated on the IGBT chip only determines the hotspot temperature (at the centre of the chip). It is therefore important to determine how these two temperatures compare and which parameters influence their difference. Three important parameters are identified and analysed in this paper: power density (P_V), overall thermal resistance ($R_{th,j-a}$) and delay time (t_{md}) in the $V_{CE}(T)$ measurement method. The absolute value of $T_{difference}$ is found to increase with increasing P_V, $R_{th,j-a}$ and t_{md}. The first part of this paper introduces the two junction temperature measurement approaches and highlights the fundamental differences between them. The second part presents the measurement results and analysis of the dependency of $T_{difference}$ with the above mentioned parameters.

TEMPERATURE CALIBRATION AND KEY DIFFERENCES BETWEEN THE T_J SENSOR AND THE $V_{CE}(T)$ METHOD

Calibration using the on-chip temperature sensor

The on-chip temperature sensor (T_j sensor) consists of a series of diodes manufactured/processed on the top surface (emitter side) of the IGBT die. As seen in Fig 1, the T_j sensor is located in the centre area of the IGBT chip. The forward characteristics of this string of sense diodes was measured at different temperatures for sense current currents in the range of 1 µA to 300 µA.

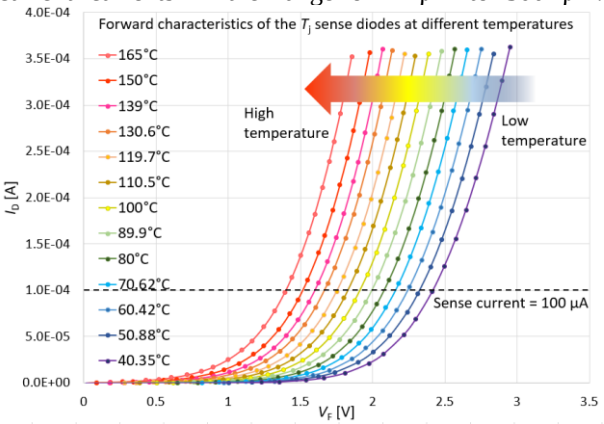

Figure 4: Forward characteristics of the T_j sense diodes at different temperatures

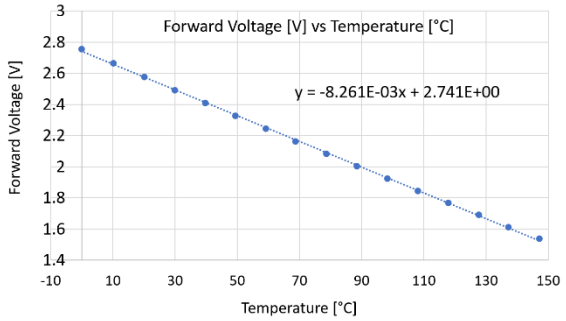

Figure 5: Calibration of the T_j sensor

As evident from Fig. 4, the T_j sensor has a negative temperature coefficient. A sense current has to be selected for measurement. At high sense currents, the impact due to self-heating of the sense diodes will be higher. At low sense currents, the impact due to noise in the measured signal will be higher. A sense current of 100 µA was selected and the T_j sensor has been calibrated at 16 points between 0 °C and 150 °C. As seen in Fig. 5, a first order linear interpolation of the forward voltage versus temperature reveals a slope of about -8.26 mV/ K.

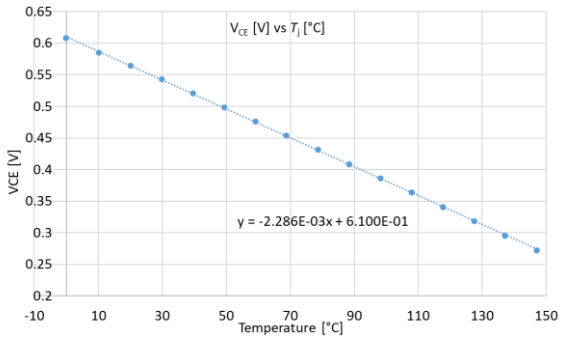

Figure 6: Calibration of the DUT using $V_{CE}(T)$ method

Differences in measurement method: T_j sensor method and $V_{CE}(T)$ method

Established guidelines for calibration and measurement using the $V_{CE}(T)$ method are available in [2] and [5]. The DUT which is a 1200 V/ 150 A (single die) IGBT was calibrated using a 100 mA sense current. A first order linear interpolation of the forward voltage versus temperature reveals a slope of about 2.28 mV/K (refer Fig. 6). The following are some key differences between the T_j sensor and the $V_{CE}(T)$ method:

1. **Nature of data acquired** – the data acquired by the T_j sensor method corresponds to the local temperature at the centre of the chip where the T_j sense diodes are located. On the other hand, the $V_{CE}(T)$ method uses the IGBT chip itself as a temperature sensor and as described in [2] the data acquired are close to the area related average temperature of the IGBT chip.

2. **Sensitivity and temperature resolution** – the calibration curves of the T_j sensor and the $V_{CE}(T)$ method indicate that the T_j sensor has about 4 times higher temperature sensitivity or temperature resolution for a given probe sensitivity.

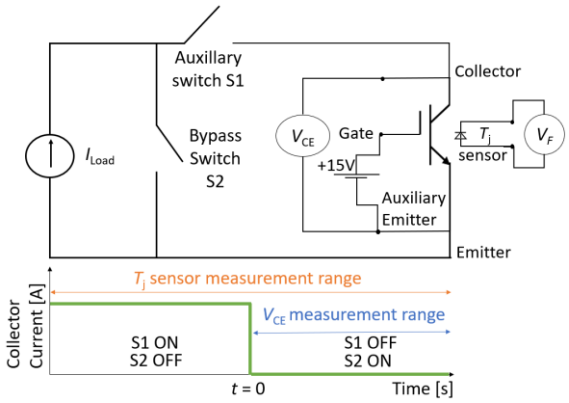

Figure 7: $V_{CE}(T)$ and T_j sensor measurement setup.

3. **Online temperature monitoring** – the $V_{CE}(T)$ method is not suitable for online temperature monitoring as the collector-emitter voltage drop is measured using the sense current after the load current has been cut-off. There exists a certain minimum recombination time of the carriers in the IGBT chip after the collector current of the IGBT has been passively turned off [6]. Therefore, a certain measurement delay (t_{md}) is maintained after the turn-off of the collector current through the IGBT. For the T_j sensor method, the temperature measurement method is decoupled from the electrical path of the chip as the anode and cathode terminals of the sense diodes are isolated from the terminals of the IGBT. Therefore, data from the T_j sensor is available for online monitoring. Fig. 7 shows the test setup for IGBT junction temperature measurement using the T_j sensor as well as using the $V_{CE}(T)$ method (load current turned off at t = 0 s, t_{md} = 300 µs for $V_{CE}(T)$ data). The results are shown in Fig. 8.

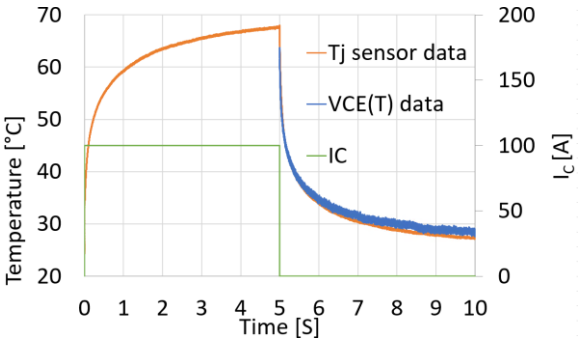

Figure 8: T_j sensor and $V_{CE}(T)$ data. I_C = 100 A and t_{on} = 5 s.

MEASUREMENT RESULTS AND ANALYSIS OF DEPENDENCIES

Motivation for estimation of $T_{vj,max}$: Power cycling lifetime models for IGBT modules can be expressed in terms of number of cycles (N_f) versus the junction temperature ripple ΔT_j [7] as proven by statistical analysis shown in [8]. Fig. 9 is an example of the power cycling lifetime model as per [8].

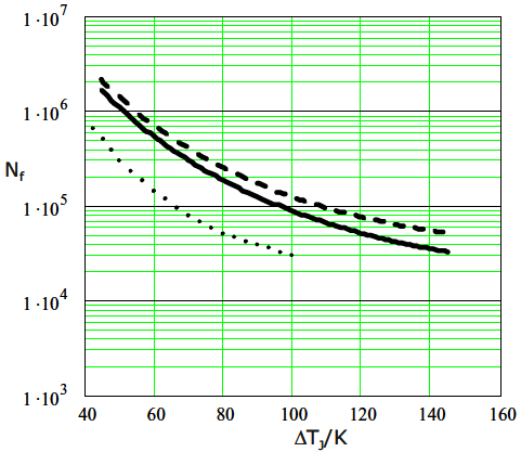

Figure 9: N_f -ΔT_j curves from the CIPS'08 model [8]. Lower dotted trace: former curve (LESIT model) of modules for industrial application at $T_{j,max}$ = 125°C. Solid line: Estimated N_f according to a new model for modules with IGBT4/1200V at $T_{j,max}$ = 150°C, ton = 1.5 s, I = 10 A; dashed line – same as solid line but $T_{j,max}$ = 125°C.

Since the junction temperature ripple ΔT_j is the difference between the maximum ($T_{j,max}$) and minimum junction temperatures ($T_{j,min}$), determination of the maximum junction temperature assumes a significant role in power lifetime analysis of IGBT modules.

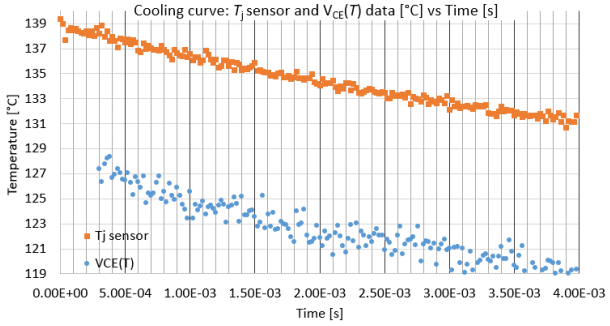

Figure 10: Plot of $V_{CE}(T)$ and T_j sensor data using I_C = 200 A, ton = 5 s, t_{md} = 300 µs. Total chip area = 134. 56 mm². Power dissipated per unit area (active area) P_V/A during heating = 3.53 W/ mm².

$T_{j,max}$ estimation method: Fig. 10 is an example for the maximum junction temperature determination using the T_j sensor and the $V_{CE}(T)$ method. In this experiment, a collector current I_C of 200 A was applied for 5 s. A difference of about 11 Kelvin is seen in the maximum temperatures measured using the T_j sensor versus the $V_{CE}(T)$ method. The DUT utilised for this study is a 1200 V/ 150 A IGBT chip which is packaged in an IGBT module. The cross section of the IGBT module is represented in Fig. 11. The IGBT chip is mounted on a ceramic substrate which is soldered to a copper baseplate. The IGBT module is mounted on a water cooled heatsink via thermal grease.

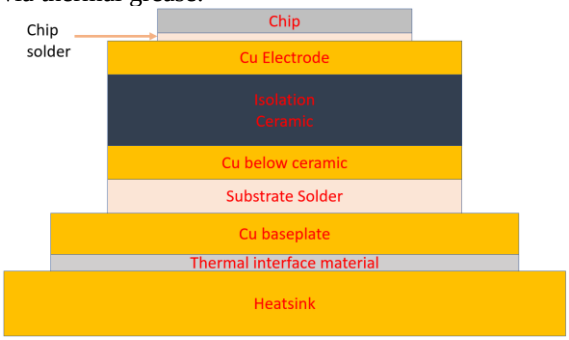

Figure 11: Cross section of the power module

Factors influencing the $T_{difference}$: The $T_{difference}$ can be resolved into two time-dependent spatial components:
$T_{difference}$ = Lateral temperature gradient (t) + Vertical temperature gradient (t)
The lateral and vertical temperature gradients depend upon the input parameters such as power density (P_V), overall thermal resistance ($R_{th,j-a}$) and delay time (t_{md}) in $V_{CE}(T)$ measurement method. Additionally, the thickness of the chip influences the vertical temperature gradient and therefore the $T_{difference}$. Fig. 12 represents the relationship between the key factors and $T_{difference}$.

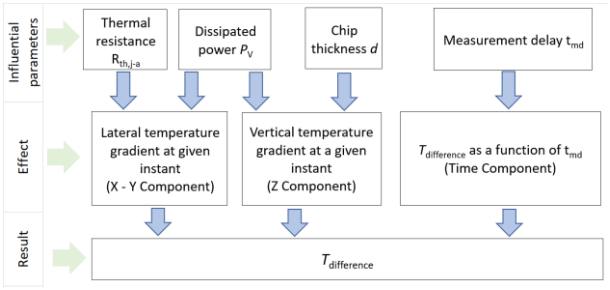

Figure 12: Summary of factors influencing $T_{difference}$

Interrelationship between P_V, T_j and $R_{th,j-a}$: The rise in junction temperature from ambient ΔT_{j-a} depends on the dissipated power (P_V) and the thermal resistance from junction to ambient ($R_{th,j-a}$).

$$\Delta T_{j-a} = P_V \cdot R_{th,j-a} \quad (2)$$

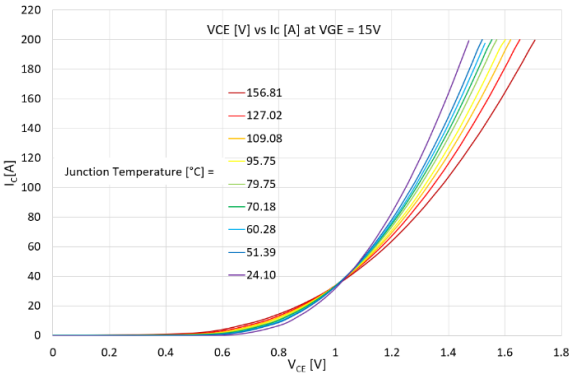

Figure 13: V_{CE} versus I_C of the DUT at different temperatures showing positive temperature coefficient of the DUT above the temperature compensation point (TCP) which is 38 A.

In order to study the impact of P_V and $R_{th,j-a}$, the interdependency of these two parameters must be understood. As per (2), when the P_V of the DUT is increased (for example by increasing the I_C), the ΔT_{j-a} of the DUT must increase resulting in the increase of the absolute T_j of the DUT.

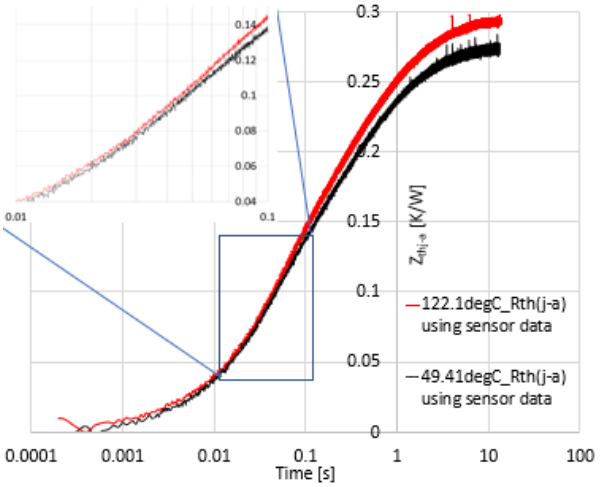

Figure 14: Measuremen of $Z_{th,j-a}$ using T_j sensor data and different heatsink temperatures. I_C = 38 A (TCP).

The R_{th} of the constituents of the IGBT module has a positive temperature coefficient [6]. As a result, overall $R_{th,j-a}$ increases when the absolute temperature increases. On the other hand, higher $R_{th,j-a}$ leads to higher ΔT_{j-a} and

results in an increase of the absolute T_j of the DUT. Since the IGBT has a positive temperature coefficient as seen in Fig. 13, the P_V is expected to increase for any given I_C. In order to confirm the temperature dependency of the $R_{th,j-a}$, an experiment was conducted at the TCP of the DUT (I_C = 38 A) by setting the heatsink to different temperatures. At the TCP, the power loss of the chip does not depend on the applied temperature, so the resulting $R_{th,j-a}$ is purely a function of the temperature coefficient of the constituents of the IGBT module. In this experiment, the data from the T_j sensor was utilised. The ΔT_{j-a} and the $Z_{th,j-a}$ were calculated accordingly. As it can be seen from Fig. 14, the overall $R_{th,j-a}$ increases with increase in temperature. Additionally, the deviation starts at the time domain between 0.01 s and 0.1 s which generally corresponds to the R_{th} variation of the chip solder plus substrate layers. An FEM simulation with ANSYS was conducted using a model of the DUT to understand the impact of the R_{th} variation of only the substrate isolation sheet. The thermal conductivity of the isolation ceramic layer was varied and the $Z_{th,j-a}$ was plotted using the maximum junction temperature. Fig. 15 confirms that when the thermal conductivity of the substrate layer is modified, a variation is expected in the time domain between 0.01 s and 0.1 s.

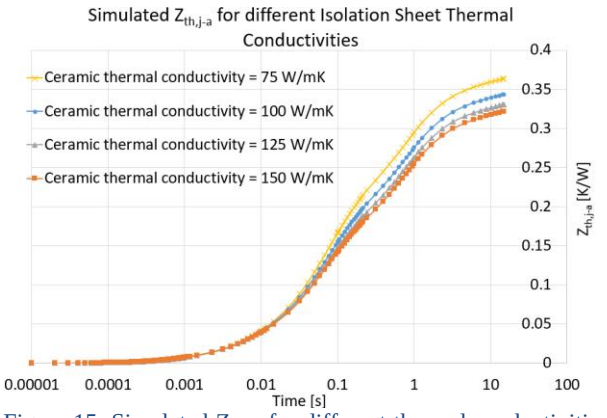

Figure 15: Simulated $Z_{th,j-a}$ for different thermal conductivities of the isolation sheet.

In Fig. 16, the $Z_{th,j-s}$ has been plotted utilising the T_j sensor data and the heatsink temperature data to confirm the hypothesis that when the P_V increases, the T_j increases and as a result the $R_{th,j-s}$ of the power module increases.

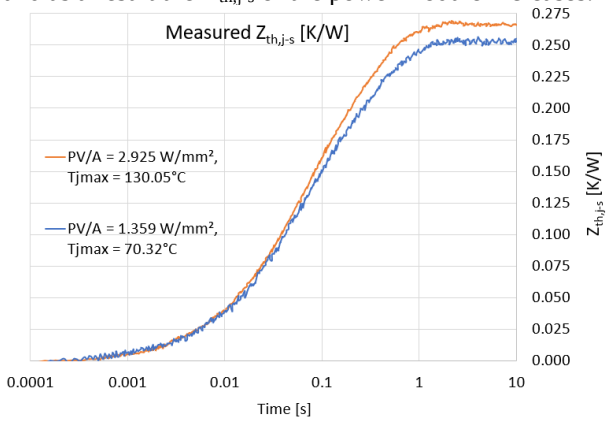

Figure 16: Measured $Z_{th,j-s}$ for different P_V/A using T_j sensor data

A summary of the relationship between the P_V and the $R_{th,j-a}$ is presented in Fig. 17.

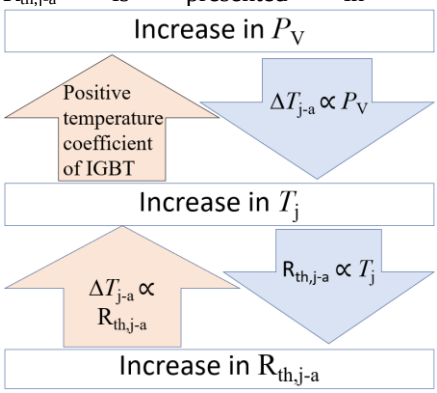

Figure 17: A summary of the interrelationship between P_V , T_j and $R_{th,j-a}$

Impact of dissipated power P_V on $T_{difference}$

For a given absolute value of P_V, the $T_{difference}$ also depends on the active area (A) of the chip. Therefore, the parameter to be considered for this analysis is the power density P_V/A in W/mm². A measurement was conducted where the I_C through the DUT was increased in steps to increase the P_V/A. As explained via Fig. 17, the $R_{th,j-s}$ (thermal resistance to sink) of the system is expected to have a positive correlation with P_V/A. The $T_{hotspot}$ was the highest temperature occurring immediately at turn-off of I_C and T_{vj,max_VCE} was acquired for different t_{md}. The measurements were repeated with different thermal interface materials to obtain different $R_{th,j-s}$ of the set-up. The $T_{difference}$ has been plotted for points having similar $R_{th,j-s}$ and same t_{md}.

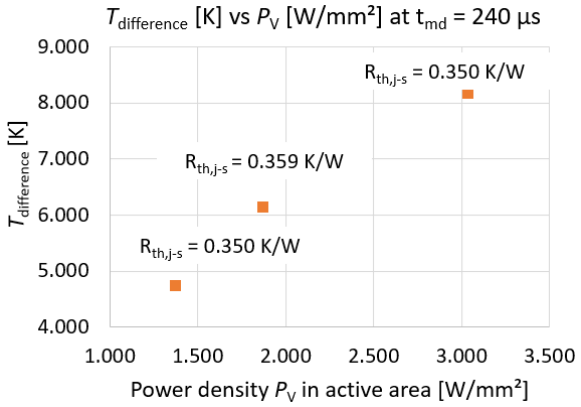

Figure 18: $T_{difference}$ versus P_V/A for points having similar $R_{th,j-s}$

Referring to Fig. 18, at $R_{th,j-s}$ = 0.35 K/W, the analysis shows a slope of about 2 Kelvin increase for an increase of 1 W/mm².

Impact of thermal resistance $R_{th,j-a}$

While (2) is true for the overall ΔT_{j-a}, the difference between the $T_{hotspot}$ and the T_{vj,max_VCE} is to be analysed with respect to the effective $R_{th,j-a}$. Measurements were conducted where the thermal interface material between the power module and the heatsink was modified in 3 steps. In this experiment, the $R_{th,j-s}$ was measured. At each

step, the $T_{difference}$ was registered for different t_{md}. The initial measurements were conducted using a thermal grease as the thermal interface material. By adding one layer of a thermally conductive foil, the overall $R_{th,j-s}$ increased by about 42% and by placing two layers of the same thermally conductive foil, the overall $R_{th,j-s}$ increased by about 66%. Fig. 19 shows the $T_{difference}$ versus $R_{th,j-s}$ for different t_{md} at similar P_V/A.

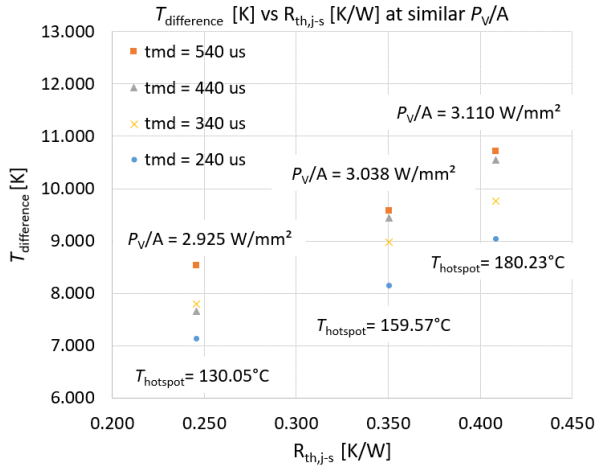

Figure 19: A plot of $T_{difference}$ versus $R_{th,j-s}$ for similar P_V/A and various t_{md}

As per the results seen in Fig. 19, a positive correlation of $T_{difference}$ versus $R_{th,j-s}$ is established. Additionally, an FEM simulation with ANSYS using the mechanical model similar to that of the DUT was conducted. The R_{th} of the TIM in the simulation was modified and its impact was analysed. The explanation for the positive correlation observed in Fig. 19 is as follows:

1. The higher R_{th} of the TIM impacts the R_{th} not only in the vertical direction (Z direction - from junction to heatsink), but also on the lateral (X-Y) plane affecting the temperature profile. This hypothesis has been verified using an FEM simulation with ANSYS where the thermal resistance of the TIM was changed and the difference between the maximum temperature and the average temperature on the surface of the chip was measured (Fig. 20). However, the effect is not too big.

2. As observed in Fig. 14, the R_{th} of the interconnections is temperature dependent. Fig. 21 shows the thermal profile in the cross section of the module. Fig. 22 shows the temperature profile on the substrate isolation layer. A lateral temperature profile exists on the interconnections such as the substrate. The result is a higher thermal resistance directly below the centre of the chip versus the periphery of the chip.

The FEM simulation does not include the temperature coefficient of R_{th} of the materials. Additionally, the simulation does not consider the positive temperature coefficient of IGBT power loss since this is not easy to implement in ANSYS. The simulation results in Fig. 20 are based on a simplified model.

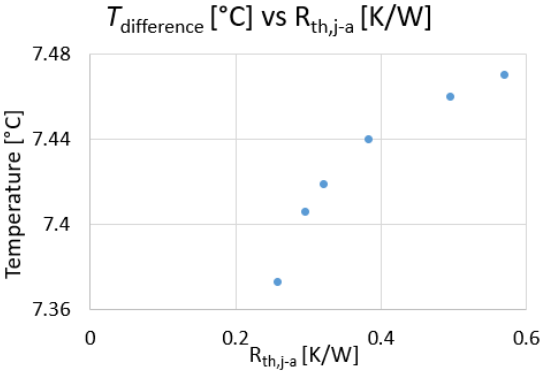

Figure 20: Simulation showing $T_{difference}$ for different $R_{th,j-a}$ by changing the thermal resistance of the TIM

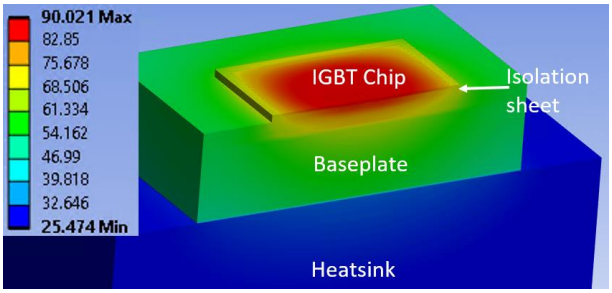

Figure 21: FEM simulation result showing the cross section of the module and the internal temperature profile

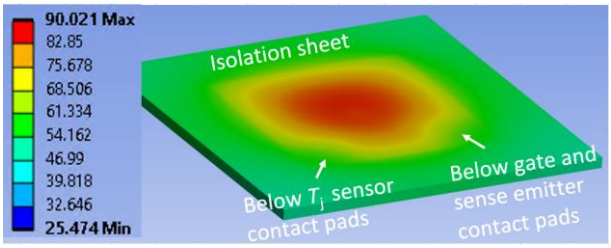

Figure 22: FEM simulation result showing the temperature profile over the ceramic isolation sheet. The regions below the contact pads (cathode and anode pads of the T_j sensor, gate pad, sense emitter pad,) are roughly indicated. The pads are inactive regions on the IGBT chip and their locations influence the appearance of the temperature profile.

Conclusion: Based on several measurements, the slope of the $R_{th,j-s}$ versus $T_{difference}$ indicates the following: an increase of 1 K/W in $R_{th,j-s}$ would result in an increase in $T_{difference}$ of around 15 Kelvin for a chip with area of 134.5 mm². This experiment was able to achieve up to 66% increase in $R_{th,j-s}$ and record a maximum of about 3 Kelvin variation in $T_{difference}$. Further analysis with a wider range of $R_{th,j-s}$ is necessary to confirm the correlation factor. In addition, the impact due to the absolute temperature should be considered if a temperature independent correlation factor is to be applied.

Impact of the chip thickness *d*

The $V_{CE}(T)$ method is based on the voltage drop occurring at the p-n junction of the IGBT chip (refer Fig. 23). The p-n junction side (bottom side) is cooled better

than the top side where the T_j sensor is located.

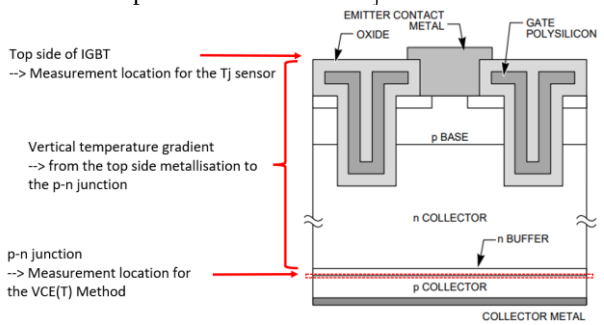

Figure 23: A cross section of a typical IGBT chip from [12]

The study in [9], has analysed the top side average temperature versus the p-n junction temperature ($V_{CE}(T)$ method). The factors influencing the vertical temperature gradient are the chip thickness d and power loss density P_V. The temperature difference was found to be 4.1 Kelvin for a 600 V IGBT (d = 70 um) at P_V/A = 2.827 W/mm². For P_V = 2.021 W/mm² the 4.5 kV IGBT (d = 470 µm), the temperature difference was found to be 8.9 Kelvin. As explained in the study, a linear approximation can be applied to estimate the temperature difference using the data points at P_V = 1.271 W/mm² and 2.021 W/mm². Thus the 4.5 kV IGBT is estimated to have a temperature difference of 10.727 Kelvin at P_V/A = 2.827 W/mm². By increasing the thickness from 70 to 470 µm, the temperature difference increases from 4.1 Kelvin to 10. 7 Kelvin. For a linear interpolation between 70 to 470 µm chip thickness, it can be roughly considered that at P_V/A = 2.827 W/mm², every 100 µm in additional thickness adds about 1.65 Kelvin in temperature difference.

Impact of the Measurement Delay (t_{md})

As discussed in the previous section, when the $V_{CE}(T)$ is applied, a certain measurement delay t_{md} has to be maintained. It has been explained in [2] and in [10] that the t_{md} should be in range of 300 µs for 1200V IGBTs. Additionally, the t_{md} selection plays a role in the maximum temperature estimated using the $V_{CE}(T)$ method [11]. The focus of this study is to analyse the impact of t_{md} on $T_{difference}$. Definition: $T_{difference}$ = $T_{hotspot}$ (occurring t = 0) - $T_{vj,max\text{-}VCE}$ (function of t_{md})

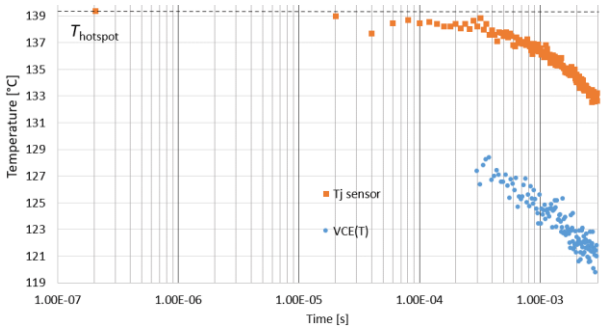

Figure 24: T_j sensor data and $V_{CE}(T)$ data for I_C = 200 A, ton = 5 s, t_{md} = 300 µs. Definition of $T_{hotspot}$ is shown.

Fig. 24 indicates that $T_{hotspot}$ is about 139 °C whereas the $V_{CE}(T)$ data begins from about 128 °C after the t_{md} of 300 µs. The same figure shows the $V_{CE}(T)$ for the first 3 ms after turning-off the load current. In this example, if the selected t_{md} is 600 µs the difference with respect to $T_{hotspot}$ is around 12.5 to 13 Kelvin.

Cooling down of active area until 1 millisecond: Fig. 25 is an FEM simulation showing the cool-down of the top surface of the active area of the chip until 1 ms.

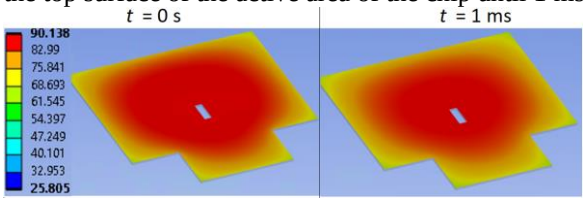

Figure 25: FEM simulation result showing the cool-down of the active area in the interval 0 < t < 1 ms.

The T_j sensor data occurring at t = 0 s is the relevant data for the $T_{difference}$ estimation. From t_{md} (300 µs) until about 1 ms, the $V_{CE}(T)$ in Fig. 24 indicates a temperature reduction in the range of 3 to 3.5 Kelvin. The average temperature of the chip is a time dependent parameter.

Quantification of $T_{difference}$ vs t_{md}: Fig. 26 shows the evolution of $T_{difference}$ versus time after tmd for measurements conducted with t_{md} = 200 µs. Data at different P_V/A and different $R_{th,j\text{-}s}$ were utilised for this analysis.

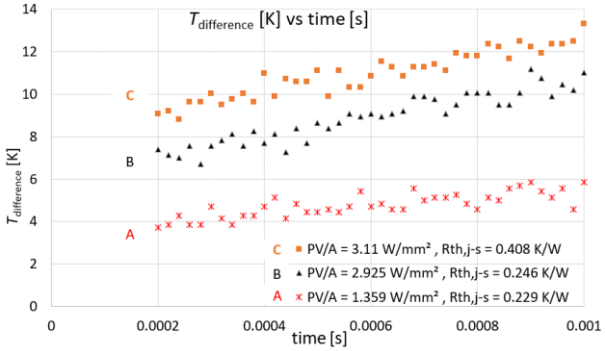

Figure 26: A plot of $T_{difference}$ for different $R_{th,j\text{-}s}$ and different P_V/A. Data from t_{md} = 200 µs onwards.

By comparing the curves A, B and C, the following tendencies can be observed:

1. Curves A and B: similar $R_{th,j\text{-}s}$ but different P_V/A. The slope for curve B is higher and it can be understood that higher P_V leads to higher slope in $T_{difference}$ versus time.

2. Curves B and C: similar P_V/A but different $R_{th,j\text{-}s}$. The absolute value of the $T_{difference}$ is higher for higher $R_{th,j\text{-}s}$. However, the slopes for both B and C are in the same range.

Summary: For higher P_V/A the increase in the slope of $T_{difference}$ has been established. At P_V/A = 2.925 W/mm², and $R_{th,j\text{-}s}$ = 0.246 K/W, the $T_{difference}$ increases by about 0.465 Kelvin per 100 µs.

CONCLUSION

Impact of the influential factors on $T_{difference}$:
This study has established the impact of the key factors on the difference in temperature between a dedicated temperature sensor and the virtual junction temperature method ($T_{difference}$). Power density P_V/A has emerged as a key parameter determining the $T_{difference}$ for a given DUT. At $R_{th,j-s}$ of about 0.35 K/W, the $T_{difference}$ would increase by 2 Kelvin for every W/mm². In addition, for a chip with a total area of 134.56 mm², the $T_{difference}$ has been found to increase with increase in $R_{th,j-s}$. The increase in $T_{difference}$ is estimated to be around 15 Kelvin for every K/W increase in $R_{th,j-s}$. Furthermore, the selection of the t_{md} has shown to have an impact of about 0.4 to 0.5 Kelvin per 100 µs. When a chip of higher voltage range (for example 3.3 kV or 4.5 kV) is used, in addition to the aforementioned factors, every 100 µm increase in chip thickness add about 1.65 Kelvin to $T_{difference.}$

Relevance of $T_{difference}$ confirmation in lifetime estimation: Higher $T_{difference}$ means higher deviation between the real $T_{vj,max}$ and the estimated $T_{vj,max.}$ The implication for power cycling lifetime estimation can be understood using two scenarios A and B.

A. Impact on lifetime consumption in a real application: For example, an application having P_V/A = 3 W/mm² could have a $T_{difference}$ of about 8 Kelvin when the $R_{th,j-s}$ is about 0.35 K/W. Due to load cycling stresses, progressive degradation is expected (such as substrate solder degradation or chip solder degradation), and the overall $R_{th,j-a}$ is expected to increase. Additional factors such as TIM degradation or reduction of cooler efficiency would contribute the overall increase in thermal resistance. As the lifetime of the DUT rapidly deteriorates, the $T_{difference}$ increases. An intermediate measurement (or estimation) of the ΔT_j performed using the $V_{CE}(T)$ would not reveal the real ΔT_j.

B. Impact on power cycling lifetime models: Power cycling tests are conducted typically at high P_V/A in order to achieve high ΔT_j. Under such circumstances, the $T_{difference}$ is high. Considering the solid line in Fig. 9 at ΔT_j = 70 Kelvin, the expected lifetime is 3 x 10^5 cycles, but at ΔT_j = 60 Kelvin the expected lifetime is between 5.5 and 6 x 10^5 cycles. Thus, if the $T_{difference}$ is about 10 to 15 Kelvin, depending up on how the ΔT_j is defined, ($V_{CE}(T)$ method or hotspot method) there could be difference of up to factor 2 in the estimated lifetime.

Limitations of this study:
1. The impact of $R_{th,j-s}$ was quantified with up to 66% variation versus initial condition. In addition, the TIM was modified to obtain different overall $R_{th,j-s}$. The impact of change in the R_{th} of the chip solder layer or substrate solder layer has to be verified.
2. The impact due to change in chip thickness was approximated based on the study in [9].

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Annealing behavior of Pt and PtH defects in fully process 1.2kV Si diodes covering the whole substrate thickness

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Abstract

We present an annealing study of the platinum-hydrogen (PtH) defect complex on fast recovery silicon (Si) high voltage diodes. These specially processed test diodes were annealed in nitrogen ambient at three different annealing temperatures for 30 min, respectively. Before and after this annealing step the substitutional platinum (Pt) and platinum-hydrogen concentration within the entire space charge region (SCR) were characterized using high-voltage current deep level transient spectroscopy. The annealing impacts the investigated trap levels as previously found in bulk Si samples. For annealing temperatures above 250°C the PtH starts to dissociate partly and at 330°C almost no PtH can be found anywhere inside the entire SCR. For the annealing at 300°C additionally an increase of the PtH concentration in the proximity of the pn-junction is observed which is most likely due to the presence of a hydrogen source located at the front side of the diodes. Furthermore, a clear correlation between the leakage currents and the PtH depth profiles suggests strongly that the PtH is the major carrier generation center in the investigated samples.

Keywords: Silicon, diode, Platinum, Platinum-Hydrogen, lifetime control, high voltage, DLTS

INTRODUCTION

In modern silicon (Si) fast-switching power diodes minority carrier lifetime control is inevitable for an efficient switching performance [1, 2, 3]. For this, additional energy levels within the band gap of Si are deliberately introduced by either high-energy particle irradiation [4, 5] or doping with noble metals as platinum (Pt) [1, 6] or gold (Au) [7, 8]. These trap levels act as recombination centers and hence reduce the carrier lifetime. Additionally, they increase the forward voltage drop V_F as well as the leakage current I_R [1]. As an increased leakage current of the diode adds to switching losses in a freewheeling diode application (e.g. with a parallel IGBT [9]) the smallest possible I_R is desired. Au and electron irradiation both result into higher I_R compared to Pt [1, 2, 10] and regarding switching behavior Pt and Au are the better choice compared to electron irradiation [1]. Therefore, Pt is often the choice for life time adjustment [1] as the low reverse currents also enable the increase of the junction temperature. For substitutional Pt (Pt_{Si}) in Si three electrically active charge transition levels are reported in literature with (E_C – 0.23) eV, (E_V + 0.09) eV and (E_V + 0.33) eV [11]. So, for an optimized minority carrier lifetime a precise control of the Pt_{Si} distribution within the space charge region (SCR) is crucial. The platinum-hydrogen (PtH_{Si}) defect complex is often observed in Pt doped devices [3], as hydrogen (H) is present in many process steps during device fabrication. As the energy of the $PtH_{Si}^{-/0}$ charge transition level (E_C – 0.5) eV [12] is close to the middle of the bandgap of Si, it acts as an efficient generation center and thereby is a main source for leakage currents. Hence, a detailed understanding of the spatial distribution and the temperature dependency of this defect level is key to optimize modern Pt doped Si diodes. Sachse et al. [11] studied the annealing behavior of four different PtH related trap levels in n- and p-type Si with Deep Level Transient Spectroscopy (DLTS) measurements via a Schottky contact. Their studies give a detailed picture of the transitions between the different PtH complexes as well as the dissociation of these complexes in Pt doped Si wafer. Rasinger et al. [13] used fully processed Si diodes for the investigation of the temperature stability of the PtH. In contrast to their studies we investigated the $PtH_{Si}^{-/0}$ and $Pt_{Si}^{-/0}$ concentration within the entire SCR whereas former DLTS measurements where limited to the proximity of the pn-junction.

EXPERIMENTAL PROCEDURE

For this study specifically processed Si high-voltage (HV) test diodes without a field stop (FS) implantation [14] were fabricated. The as such processed devices have a deliberately high contamination with H from several different process steps after the Pt doping and thus impact the Pt defect complexes significantly. During device fabrication the Pt is diffused by an annealing step after the Pt doping. This diffusion step has a significantly higher temperature budget than the additional annealing steps which were executed on the fully processed diced devices. For the additional annealing steps the diodes were placed inside a furnace with N_2 ambient and annealed at 250°C, 300°C and 330°C for 30 min, respectively.

Before and after the annealing depth profiles of the concentration of the $Pt_{Si}^{-/0}$ and the $PtH_{Si}^{-/0}$ within the entire SCR were measured using HV-Current Deep Level Transient Spectroscopy (HV-IDLTS) [14, 15]. For IDLTS [16] three voltages pulses are applied consecuitevely: the first pulse V_R sets the width of the SCR during which all traps inside the SCR are discharged. The second pulse $|V_F| < |V_R|$ reduces the volume of the SCR and hence some of the previously emptied traps are filled. After this the voltage is switched back to V_R, the traps emit the captured charge carriers and the resulting current transient is measured. As this emission process is strongly dependent on temperature, this pulse sequence is repeated over a large temperature range to characterize trap levels with different activation energies (E_a) and capture cross sections.

Our measurement setup [15] uses a Keithley 2636B with a voltage range of 200 V and a cryogenic probe station. For the measurement the temperature is ramped starting from 20 K up to 300 K and the current transients are measured continuously. The filling and the reverse bias for every IDLTS measurement is chosen to obtain the same measurement volume for each voltage pair. The measurement volume closest to the pn-junction uses $V_F = 0$ V and $V_R = 3$ V and the highest voltage pair is $V_F = 88$ V and $V_R = 107$ V. For $V_F > 107$ V the electric field reaches the backside of the investigated diodes. With these IDLTS measurements we can identify all electrically active defects before and after the annealling steps on the fully processed devices as well as their concentration throughout the entire substrate thickness.

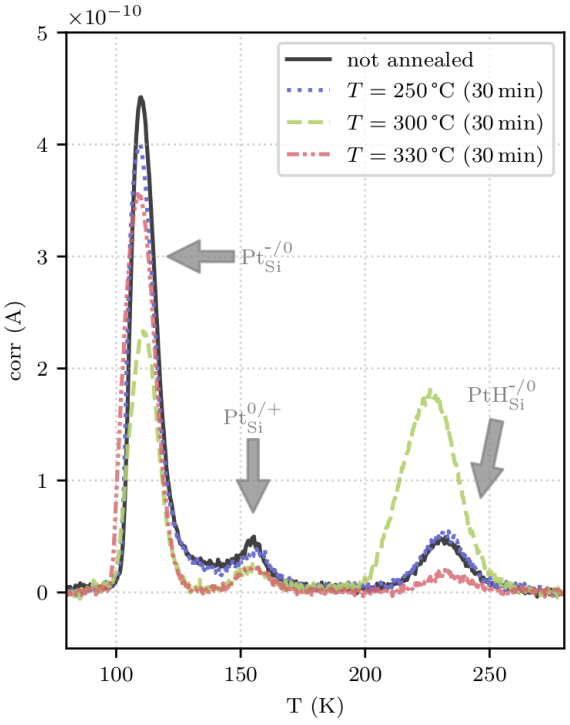

Figure 1: IDLTS of a not annealed sample and the samples annealed at T=250°C, 300°C and 330°C. All four IDLTS spectra show three peaks which are assigned to two different charge states of Pt_{Si} and one to PtH. The spectra were measured with $V_F = -3$ V and $V_R = -9$ V. The filling pulse was applied for $t_F = 100$ ms and the reverse pulse for $t_R = 500$ ms.

Assignment	E_a in eV	E_a in eV Literature values
$Pt_{Si}^{-/0}$	$E_C - 0.22 \pm 0.03$	$E_C - 0.23$ [11, 17]
$PtH_{Si}^{-/0}$	$E_C - 0.51 \pm 0.02$	$E_C - 0.5$ [11, 12]
$Pt_{Si}^{0/+}$	$E_V + 0.31 \pm 0.03$	$E_V + 0.33$ [11] $E_V + 0.314$ [17]

Table 1: Measured activation energies as determined by IDLTS measurment and literature values used for trap level identification.

EXPERIMENTAL RESULTS AND DISCUSSION

The IDLTS spectra close to the pn-junction show three different peaks which are assigned to the $Pt_{Si}^{-/0}$ (109 K), $Pt_{Si}^{0/+}$(157 K) and $PtH_{Si}^{-/0}$(243 K) as shown in Figure 1. The corresponding Arrhenius energies used for the trap level assignment are summarized in Table 1 together with the literature values. For the depth profile investigations, we focus on the majority carrier charge transition levels because the biasing is always in the reverse direction of the diode and hence this measurement procedure is not suited to investigate minority carrier trap levels.

In figure 2 the depth profiles before and after the annealing step at 330°C are shown. Before the annealing $Pt_{Si}^{-/0}$ is mainly located close to the pn-junction and especially in the middle of the SCR the $PtH_{Si}^{-/0}$concentration is highest. After the annealing at 330°C the $PtH_{Si}^{-/0}$ nearly vanishes while the $Pt_{Si}^{-/0}$ is now detectable in the entire SCR. The $Pt_{Si}^{-/0}$ and the $PtH_{Si}^{-/0}$ are the only majority carrier defect levels present in the investigated sample. Hence, the sum of $Pt_{Si}^{-/0}$+ $PtH_{Si}^{-/0}$before the annealing is compared to the depth profile of $Pt_{Si}^{-/0}$ after the annealing.

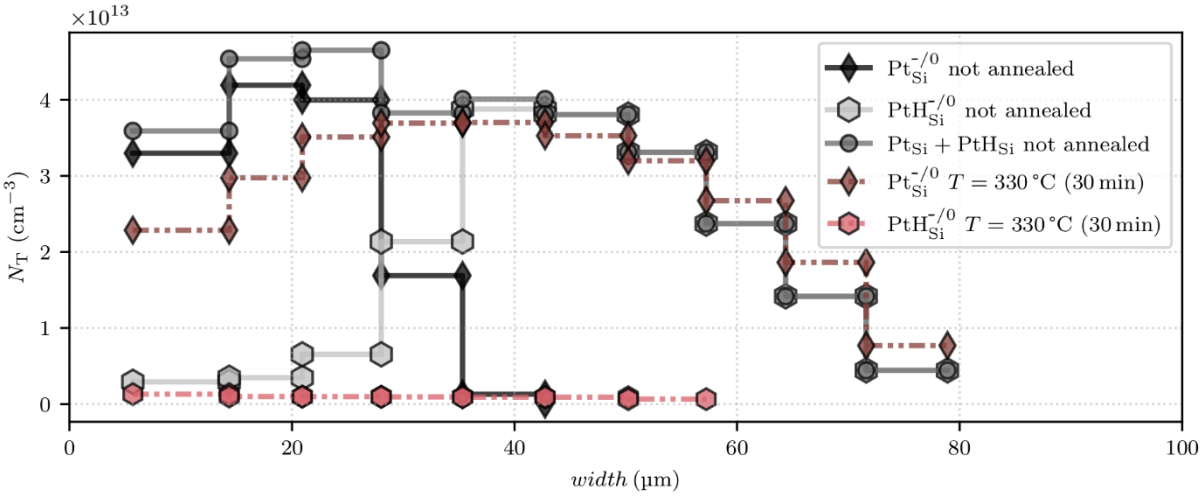

Figure 2: Depth profiles of the $Pt_{Si}^{-/0}$ and $PtH_{Si}^{-/0}$ before and after an annealing step at 330°C for 30 min using HV-IDLTS. For the not annealed sample also the sum of the two majority carrier traps is included. The depth profiles for the $Pt_{Si}^{-/0}$ as well as for the $PtH_{Si}^{-/0}$ change signifcantly by this anneal. After the anneal almost no $PtH_{Si}^{-/0}$ is detected and the $Pt_{Si}^{-/0}$ depth profile matches with the $Pt_{Si}^{-/0} + PtH_{Si}^{-/0}$ depth profile before the anneal.

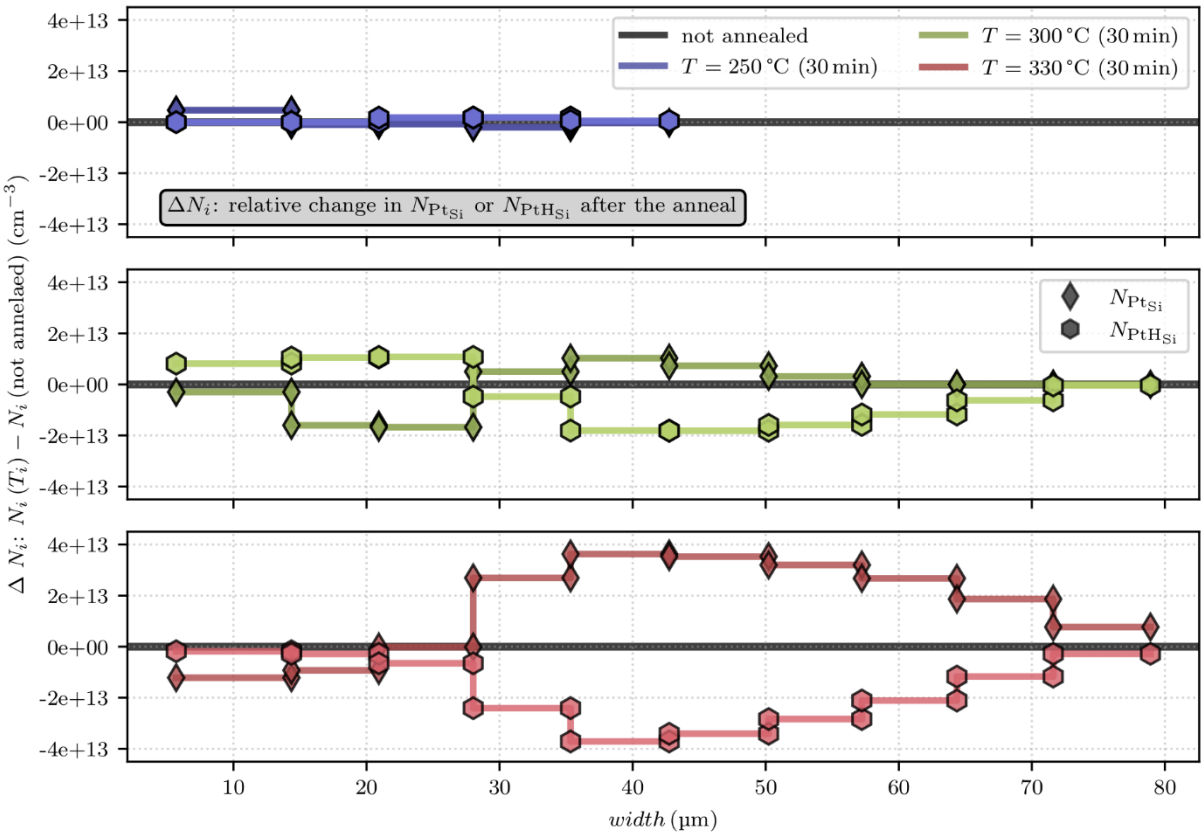

Figure 3: The difference of the $Pt_{Si}^{-/0}$(diamonds) and $PtH_{Si}^{-/0}$ concentration after the different anneals compared to the not annealed sample. A positive ΔN_i (eq. (1) and (2)) indicates a larger concentration of the defect level after the annealing step and vice versa for a negative ΔN_i. For the smallest annealing temperature of 250°C the concentration of both charge transition levels does not change. For the anneal at 300°C $N_{Pt_{Si}}$ decreases at the beginning of the SCR which is correlated to an increase of $N_{PtH_{Si}}$. In the middle of the SCR $N_{Pt_{Si}}$ is increased indicating a partial dissociation of the PtH. The increasing $PtH_{Si}^{-/0}$ concentration is suspected to be linked to a hydrogen source located at the frontside of the device. The annealing at T=330 °C clearly shows a dissociation of the $PtH_{Si}^{-/0}$ into $Pt_{Si}^{-/0}$ as the curves are almost symmetric around zero for a width > 27 µm. The decreased $Pt_{Si}^{-/0}$ concentration in the proximity of the pn-junction could possibly be linked to an out-diffusion of the Pt as described in [6, 18].

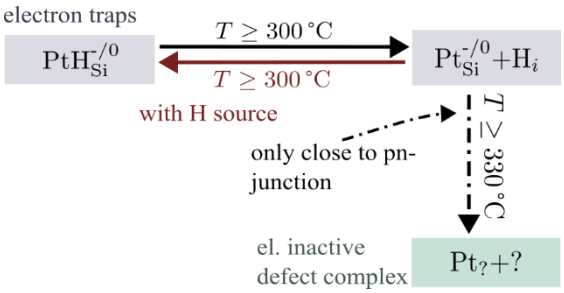

Figure 4: Summary of observed transitions of the $Pt_{Si}^{-/0}$ and the $PtH_{Si}^{-/0}$ for annealing temperatures $T \geq 300$ °C and $t = 30$ min. For smaller annealing temperatures no change of the $Pt_{Si}^{-/0}$ and the $PtH_{Si}^{-/0}$ defect concentration was observed. The reaction of $Pt_{Si}^{-/0}$ + H is only possible if H is available. In the investigated samples the frontside metallization is suspected to act as such a source for T ≥ 300 °C. For the anneal at 330 °C the dissociation of $PtH_{Si}^{-/0}$ outweighs and $N_{PtH_{Si}}$ is significantly reduced within the entire SCR. A decrease of the $Pt_{Si}^{-/0}$ concentration is observed for $T = 330$ °C in the proximity of the pn-junction. This indicates a transformation of the electrically active Pt_{Si} into an electrically inactive defect complex which could be interstitial Pt_i.

These two depth profiles match almost perfectly indicating a dissociation of the $PtH_{Si}^{-/0}$ to $Pt_{Si}^{-/0}$ + H over the entire SCR width/substrate thickness which is in accordance with previous annealing experiments [11, 13].
For a more detailed analysis of the different annealing temperatures T_i on the $Pt_{Si}^{-/0}$ and the $PtH_{Si}^{-/0}$ concentrations the difference in trap concentration is plotted with the not annealed sample as reference:

$$\Delta N_{Pt_{Si}} = N_{Pt_{Si}}(T_i) - N_{Pt_{Si}}(\text{not annealed}), \quad (1)$$

$$\Delta N_{PtH_{Si}} = N_{PtH_{Si}}(T_i) - N_{PtH_{Si}}(\text{not annealed}). \quad (2)$$

The depth profile of $\Delta N_{Pt_{Si}}$ and $\Delta N_{PtH_{Si}}$ is shown in Figure 3 for each annealing temperature, respectively. The annealing temperature of 250°C seems to not affect the two charge transition levels $Pt_{Si}^{-/0}$ and $PtH_{Si}^{-/0}$ as $\Delta N_{Pt_{Si}}$ as well as $\Delta N_{PtH_{Si}}$ is close to zero within the entire measurement volume.
For the two higher annealing temperatures both $\Delta N_{Pt_{Si}}$ and $\Delta N_{PtH_{Si}}$ depth profiles change significantly. For $T = 300$ °C the $Pt_{Si}^{-/0}$ concentrations decrease for the first three measurement volumes and is increased in the middle of the SCR and vice versa for the $PtH_{Si}^{-/0}$. These two contrary trends could indicate a hydrogen source located at the frontside of the chip which becomes active for $T \geq 300$ °C leading to an increase of $PtH_{Si}^{-/0}$ close to the pn-junction. A possible hydrogen source could be the frontside metallization. The assumption of the hydrogen source located at the frontside is supported by the decrease of $PtH_{Si}^{-/0}$ further inside the device. This suggest a partly dissociation of the $PtH_{Si}^{-/0}$ into $Pt_{Si}^{-/0}$ + H which is at slightly lower temperatures than previously described with T > 327 °C for a 60 min anneal [11].
For the highest annealing temperature of 330 °C an almost complete dissociation of the $PtH_{Si}^{-/0}$ into $Pt_{Si}^{-/0}$ + H is observed as discussed previously in Figure 2. Apart from this mechanism a decrease of $N_{Pt_{Si}}$ is observed in the proximity of the pn-junction. Thus, an additional minority carrier transient spectroscopy (MCTS) measurement was performed covering the first two measurement volumes with $V_F = +1$ V and $V_R = -7$ V. This spectrum does not show additional minority carrier traps for the sample annealed at $T = 330$ °C. These experimental results indicate a transformation of

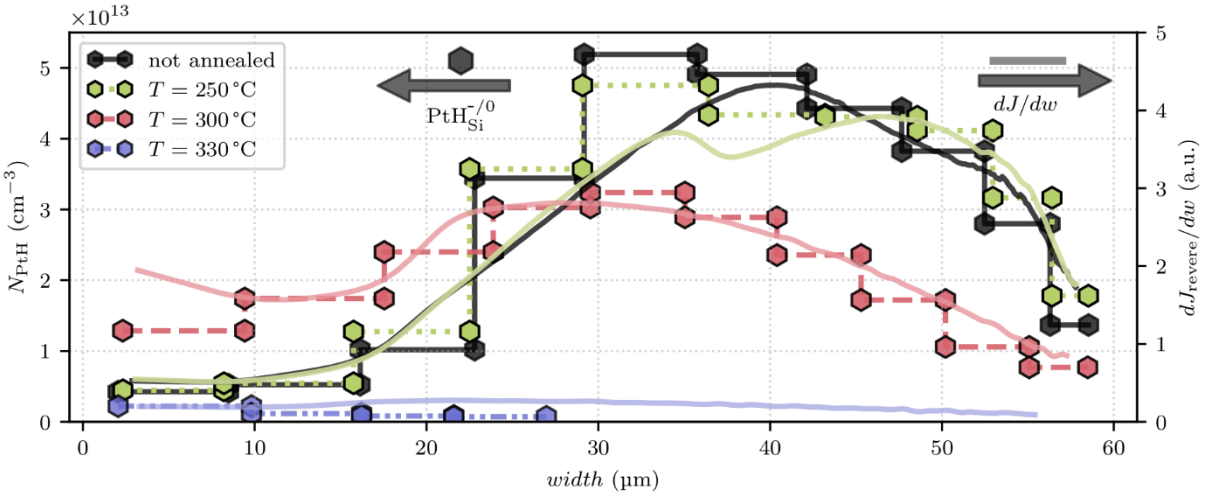

Figure 5: Depth profile of the $PtH_{Si}^{-/0}$ obtained from HV-IDLTS (hexagons and left hand-side y-axis) and the depth profile from the derivative dJ/dw from reverse IV measurements (solid lines and right hand-side y-axis). For each sample these two differently obtained depth profiles match almost perfectly which strongly suggest that the $PtH_{Si}^{-/0}$ charge transition level is the main source of leakage current in these devices. Furthermore, an increase of the $PtH_{Si}^{-/0}$ as well as for the leakage current close to the pn-junction is observed for the sample annealed at 300°C.

electrically active substitutional Pt_{Si} into an electrically inactive defect or defect complex during this anneal, as the temperature is well below the diffusion temperature of Pt [1]. In [6, 18] a reduction of the $Pt_{Si}^{-/0}$ concentration close to the pn-junction is described in dependence on the cool down rate of the Pt diffusion. They suggest an *out-diffusion* of the Pt due to a transition of substitutional Pt_{Si} into interstitial Pt_i (electrical inactive) by the reverse Frank-Turnbull and reverse kick-out mechanism. Even though the temperature budget of our annealing temperatures is significantly smaller we suspect a similar mechanism of the decreased $Pt_{Si}^{-/0}$ concentration.
A summary of the observed transitions for the different annealing steps is given in Figure 4.

Apart from the annealing behavior of the $PtH_{Si}^{-/0}$ we also investigated the correlation between the leakage current and the $PtH_{Si}^{-/0}$ depth profiles for each annealing step. For this we obtained the depth profile of the major generation center from reverse current voltage (IV) characteristic by calculating dJ/dw [9]. These two differently calculated depth profiles are both shown in Figure 5. For all different annealing temperatures, a strong correlation of these two differently obtained depth profiles is observed. This indicates that the $PtH_{Si}^{-/0}$ is the major generation center in all samples which is in accordance with previous reports on fully processed Pt doped HV-Si diodes [13, 19].

CONCLUSION

By using HV-IDLTS we could analyze the annealing behavior of the PtH on fully processed diodes throughout the complete substrate thickness. For the smallest annealing temperature of 250°C we did not see a change of the defect concentrations. For all higher annealing temperatures, we obtain different annealing results depending on the distance to the pn-junction as well as on the annealing temperature. For the anneal at 300°C we observe a partly dissociation of the $PtH_{Si}^{-/0}$ in the middle of the SCR and an increasing $PtH_{Si}^{-/0}$ concentration close to the pn-junction. This indicates a H source at the frontside of the fully processed diodes which becomes active during the anneal. For the highest annealing temperature of 330°C we obtain an almost complete dissociation of the $PtH_{Si}^{-/0}$ as the remaining $PtH_{Si}^{-/0}$ concentration is comparable small and the $Pt_{Si}^{-/0}$ depth profile after the anneal correlates strongly with the $Pt_{Si}^{-/0} + PtH_{Si}^{-/0}$ depth profile before the anneal. In the proximity of the pn-junction we observe a smaller $Pt_{Si}^{-/0}$ concentration after the anneal. We suspect a transformation of the electrically active substitutional Pt_{Si} into electrically inactive interstitial Pt_i as described in [6, 18]. Furthermore, the almost perfect match of the $PtH_{Si}^{-/0}$ depth profiles from HV-IDLTS with the depth profiles calculated from reverse IV measurements indicates strongly that the major generation center is the $PtH_{Si}^{-/0}$ in all samples.

ACKNOWLEDGEMENTS

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Surge-Current capability of the different voltage class IGBTs

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Abstract

In this work, the surge-current capability of 650 V, 1200 V, and 1700 V IGBTs has been investigated. This stress condition is important for the active short-circuit of motor loads. For all measurement conditions, the destruction of the devices is not determined by the onset of intrinsic conductivity. Instead, the failure signature indicates a temperature-driven destruction mechanism. For the applied gate-emitter voltages, the 650 V IGBTs show the highest surge-current density withstand capability in comparison to 1200 V and 1700 V IGBTs due to their higher saturation current density. The surge-current capability of 1200 V and 1700 V IGBTs is not influenced by the amount of emitter bond wires even at a gate-emitter voltage of 25 V, whereas it is reduced for 650 V IGBTs with a reduced number of bond wires.

Keywords: IGBT, surge-current, surge-current capability, robustness, bond wire, Al metallization.

INTRODUCTION

IGBTs are widely used power semiconductor devices in medium and high power switching applications. For many applications, short-circuit is a necessary chip requirement. However, there is typically no specification of a surge-current capability that determines the device's ability to withstand and operate under very high current transients or surges. This requirement is naturally in contradiction to the short-circuit ruggedness. Only in special cases, a surge-current operation of IGBTs is beneficial. It can be used to protect the load from alternating torques due to asymmetric short-circuit failures in IGBT converters as described in [1-4]. The active short-circuit of motor loads is one example of this case. Grid errors such as voltage spikes and overvoltage conditions can generate a surge-current for grid-side connected power semiconductor devices (e.g. PFC/rectifier diodes, rectifying switches).

Previous work has demonstrated that IGBTs can conduct high surge-currents at higher gate-emitter voltages by preventing the collector-emitter voltage (V_{CE}) desaturation [1–6]. The surge-current behaviour for different IGBT designs is discussed in [3,7]. Further details regarding the surge-current theory of bipolar devices can be found in [8–11]. The degradation of the chip solder by ageing has a strong influence on the surge-current capability of the IGBT and has been discussed in [12].

In the present work, single pulse surge-current measurements were performed for different voltage class IGBTs with trench technology using an open chip soldered on a direct copper bonded (DCB) substrate. All the measured IGBTs have a similar assembly and interconnect technology (AIT). The surge-current capability of all the IGBTs was measured at distinct gate-emitter voltages and for varying starting temperatures. Also, the influence of the pulse width on the 1700 V IGBT surge-current capability has been studied.

In power semiconductor devices, such as diodes or IGBTs, the bond wires play a crucial role in carrying electrical current. Hence, the impact of the number of emitter bond wires on the surge-current capability of the different voltage class IGBTs has been investigated in detail.

CURRENT LIMITATION OF THE IGBTS

The saturation current $I_{C,sat}$ of the IGBT limits the surge-current capability. Consequently, the IGBT must be prevented from channel pinch-off and V_{CE} desaturation during surge-current operation. Otherwise, it leads to higher losses and destruction. According to the simple MOSFET model the pinch-off voltage $V_{CE,pinch}$ of the MOS channel with a threshold voltage V_{TH}, is given by

$$V_{\mathrm{CE,pinch}} = V_{\mathrm{GE}} - V_{\mathrm{TH}} \qquad (1)$$

for a given gate-emitter voltage V_{GE}. The output characteristics of the different IGBTs are compared with each other by their normalized saturation collector-current density ($J_{C,sat}$). Each voltage class IGBTs was normalized by choosing the appropriate normalized current. The ratio of $I_{C,sat}$ by its active area of the IGBT chip is plotted as a function of gate-emitter voltages for two different temperatures as shown in Fig.1. As can be

seen for both temperatures, the 650 V IGBT shows the highest $J_{C,sat}$ compared to the other two voltage class IGBTs. The saturation current density of the 1200 V IGBT is only slightly higher than the 1700 V IGBT. For the IGBT saturation mode, $I_{C,sat}$ depends on V_{GE} by a quadratic function:

$$I_{C,sat} = \frac{1}{1-\alpha_{pnp}} \cdot \frac{k}{2}(V_{GE} - V_{TH})^2 \qquad (2)$$

where k is a channel-geometry parameter and α_{pnp} the bipolar current gain of the pnp transistor. The main temperature dependent parameters in Eq. (2) are the threshold voltage $V_{TH,}$ α_{pnp} and the electron mobility μ_n which is included in the parameter k.

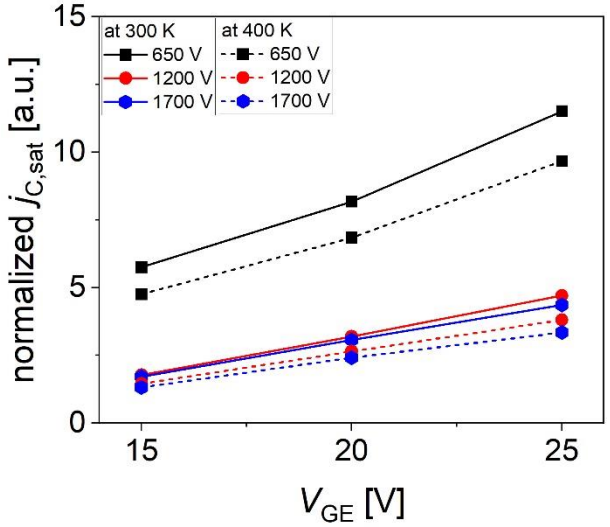


Fig. 1: Normalized saturation collector-current density of the different voltage class IGBTs with varying gate-emitter voltage.

SURGE-CURRENT MEASUREMENT

For investigating the surge-current capability of the IGBTs, a test setup described in [13] was used. During the measurements, a calibration current of 10 mA flowed through the device under test (DUT) IGBT to estimate the junction temperature before and after the surge-current pulse. The junction temperature was estimated using the $V_{CE}(T)$ – method. The V_{CE}(T) calibration curve is predetermined for the different DUTs at different V_{GE} for a temperature range from 295 K to 430 K. The surge-current capability was measured by gradually increasing the surge-current amplitude $\hat{\jmath}_{FSM}$ in steps until a destruction of the DUT occurs or a static electric parameter such as gate-leakage current or $V_{CE,sat}$ or blocking leakage current has changed. Further, the surge-current measurements were carried out at different gate-emitter voltages at varying starting temperatures (T_{start}). Additionally, the influence of the different surge-current pulse-width (t_p) was analyzed for the 1700 V IGBT. For all the surge-current density plots, the normalization was done by choosing the appropriate normalized current density for each voltage class IGBTs.

a) Surge-Current measurements at 10 ms

Initially, the surge-current measurements were carried out with half-sine pulses with t_p of 10 ms, which corresponds to the grid frequency of 50 Hz. The corresponding voltages across the collector and sense-emitter ($V_{CE,sense}$) and across the collector and load-emitter ($V_{CE,load}$) are recorded.

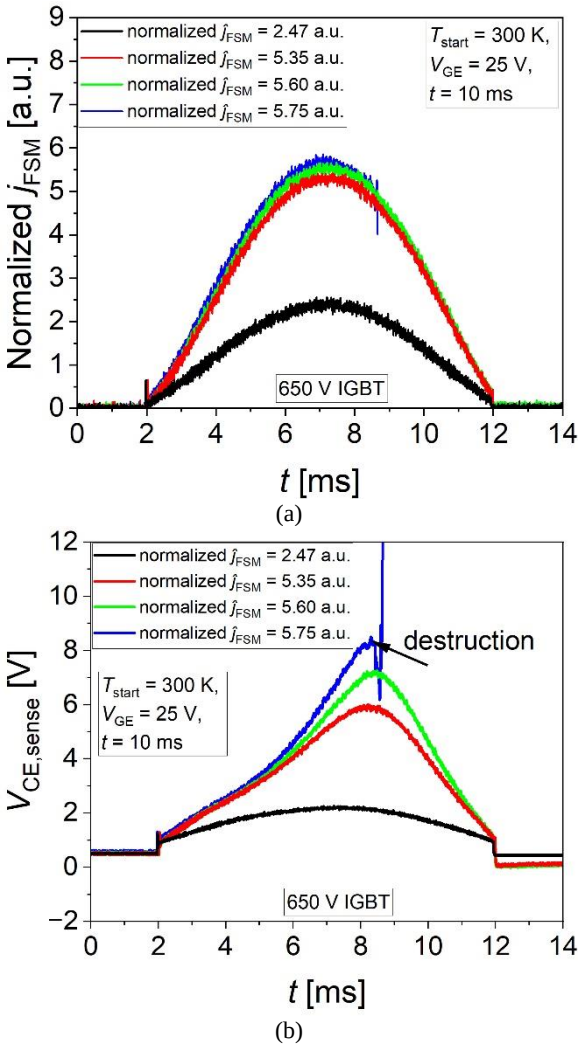


Fig. 2: (a) Measured normalized surge-current capability of the 650 V IGBT increasing the surge-current density amplitude $\hat{\jmath}_{FSM}$ (normalized) (b) measured $V_{CE,sense}$ across the IGBT. For measurement conditions: t_p = 10 ms, V_{GE} = 25 V, T_{start} = 300 K.

For the time interval between 0 ms and 2 ms, before the surge-current is applied [see, Fig. 2(a)], the V_{GE} is set to a high level and the calibration current of 10 mA is flowing. Hence, $V_{CE,sense}$ shows a voltage drop of approximately 0.6 V, which corresponds to the built-in potential of the backside pn-junction at room temperature as shown in Fig. 2(b). As the applied surge-current amplitude is increased across the IGBT, the $V_{CE,sense}$ voltage waveform has its peak after the surge-current

density peak and is strongly deviating from sine-shaped due to the temperature rise in the chip. Applying high currents close to the saturation current leads to a sharp increase in the voltage. After the IGBT has passed the surge-current pulse, the $V_{CE,sense}$ shows a lower voltage drop compared to the starting value, especially at increased surge-current amplitude [Fig. 2(b) after 12 ms] because the built-in potential of the pn-junction is decreased due to significant temperature increase. It is interesting that the falling branches have almost the same V_{CE} at t = 11.75 ms, although the dissipated losses are much different. However, the high V_{GE} compensates for a higher V_{CE}. When the surge-current density amplitude ($\hat{\jmath}_{FSM}$) was increased to 5.75 a.u., the 650 V IGBT failed due to the beginning of V_{CE}-desaturation and correspondingly a higher loss although the V_{GE} value was at 25 V. In contrast to the expected quadratic relation between $I_{C,sat}$ and V_{GE}, see Eq. (1). The measured surge-current capability of the 650 V IGBT at V_{GE} = 25 V and starting temperature of 300 K shows a more linear relation between surge-current and gate voltage. This is due to the self-heating of the device during the surge-current pulse which leads to a lower saturation current of the IGBT. Hence, the n-channel is pinched-off earlier [7]. For the last-pass pulse with $\hat{\jmath}_{FSM}$ of 5.60 a.u., the junction temperature at 12.2 ms is 506 K, estimated via $V_{CE}(T)$ method. It should be noted that the maximum junction temperature will be much higher during the pulse.

For the 1700 V IGBT, the measured last-pass pulse at different gate-emitter voltages at 300 K is shown in $j_{FSM}(V_{CE})$ characteristic in Fig. 3(a). At V_{GE} = 15 V, the MOS channel is pinched off earlier in comparison to V_{GE} of 25 V [Eq. (1) and (2)]. The spread between the rising and falling branches is smaller at V_{GE} = 15 V due to lower dissipated overall losses. However, with higher V_{GE} the thermal hysteresis increases because the IGBT reaches its critical saturation collector-current later and makes less losses from the beginning. The estimated junction temperature is 346 K at 15 V and 512 K at 25 V at t = 12.2 ms, i.e. 0.2 ms after the surge current pulse. At high currents, a positive temperature coefficient (PTC) is observed during the surge-current transient. At the descending branch and the lower currents, a negative temperature coefficient (NTC) is visible mainly from the reduced built-in voltage of the collector-side pn-junction. Furthermore, at such high temperatures, the charge carrier mobilities are strongly reduced. Consequently, the charge carrier concentration in the low doped drift region with a width w_B will change as can be estimated by the following simplified equation for the mean carrier concentrations $\bar{n}$, $\bar{p}$, in the drift region [5]:

$$\bar{n} = \bar{p} = \frac{j \cdot w_B}{V_{drift} \cdot q \cdot (\mu_n + \mu_p)} \qquad (3)$$

where V_{drift} is the voltage drop across the low doped drift region and j is the current density.

The influence of the starting temperature at V_{GE} = 25 V is illustrated in the $j_{FSM}(V_{CE})$ characteristic in Fig. 3(b). At 300 K, the thermal hysteresis between the branches is larger due to higher losses accompanied by the higher applied surge-current compared to 425 K. At the falling branch, the $V_{CE,sense}$ voltages are higher due to the higher starting chip temperature [2]. For the same V_{GE}, the saturation current decreases as the temperature increases, mainly due to reduced mobilities.

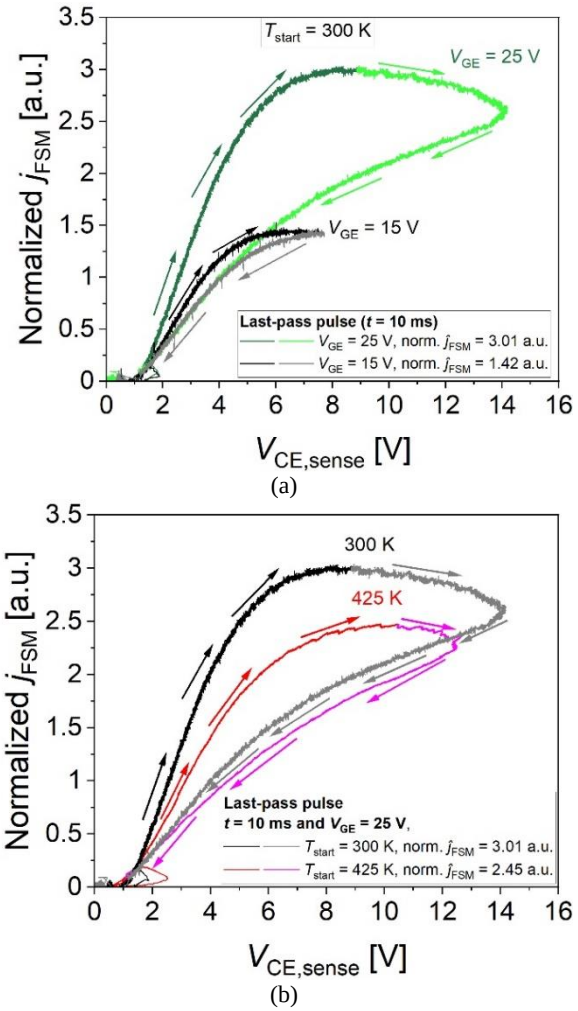


Fig. 3: Measured last-pass normalized surge-current pulse of 1700 V IGBT (a) for gate-emitter voltages of 15 V and 25 V at T_{start} = 300 K. (b) at different starting temperatures for V_{GE} = 25 V. Conditions: t_p = 10 ms.

The last-pass surge-current and energy density of the different voltage class IGBTs are compared at 300 K and 425 K, in Fig. 4. Two devices each of the 650 V and 1700 V classes and four devices of the 1200 V IGBTs were considered for room temperature measurements. At 425 K, only one device was used in the destructive test, except for the 1200 V class. At V_{GE} = 15 V and at both temperatures, 1200 V IGBTs do not show any failure since the current could not be increased further due to the limitation of the used DC-link capacitors in the test-bench. For both gate voltages and temperatures, the 650 V IGBTs show a higher surge-current density in than the 1200 V and 1700 V IGBTs, which is correlating with the respective nominal current densities of the IGBTs. It

is also visible, that the energy density of all the voltage classes is in the same range for V_{GE} = 25 V.

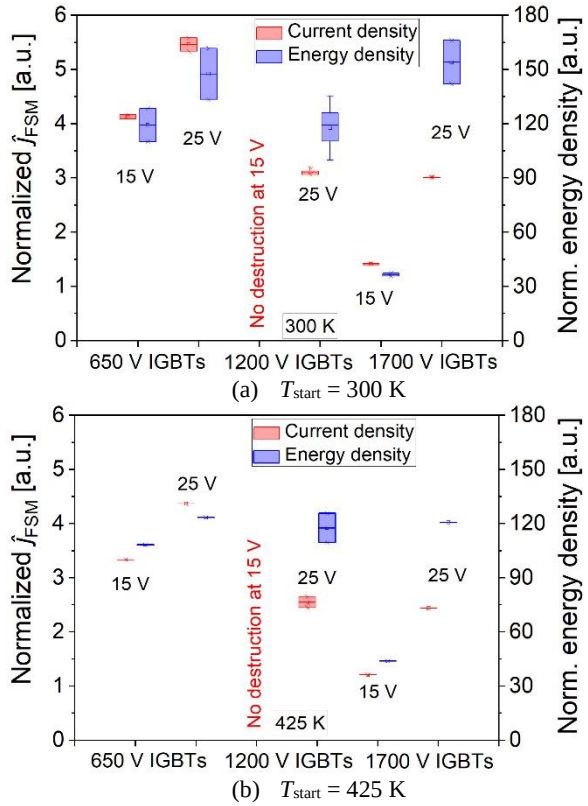


Fig. 4: Comparison of the last-pass maximum normalized surge-current density and corresponding normalized energy density of the different voltage class IGBTs for different gate-emitter voltages at t_p = 10 ms.

For all the measured IGBTs, $V_{CE,sat}$, gate leakage current and collector-emitter leakage current was recorded after each single surge-current event and compared with the initial values measured before. However, there was no drift in any of these analysed parameters.

b) Surge-Current measurements at 1 ms

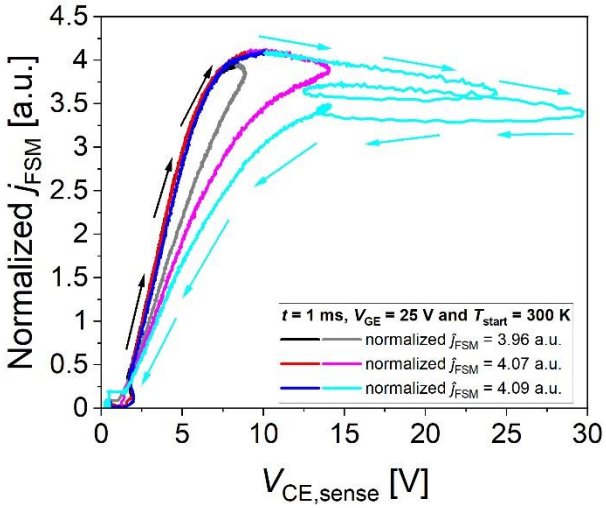


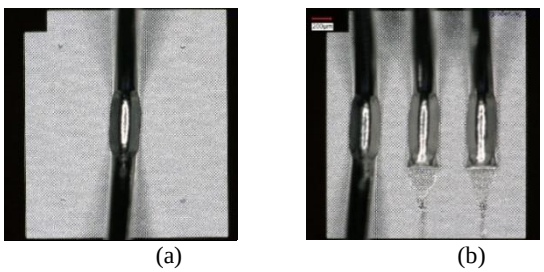
Fig. 5: Measured normalized $j_{FSM}(V_{CE})$ characteristic of a 1700 V IGBT with increased surge-current density at t_p = 1 ms. Conditions: V_{GE} = 25 V, T_{start} = 300 K.

A surge-current can appear in various waveforms depending e.g. on the actual output current frequency of an inverter. Standard tests and datasheet ratings typically use a half-sine wave with a duration between 100 µs and 100 ms [14]. For the results presented here, the surge-current pulse width was set to 1 ms. As shown in Fig. 5, at V_{GE} = 25 V, the 1700 V IGBT reached its saturation collector-current without any failure and a similar behaviour was observed at V_{GE} = 15 V. As the energy dissipation was 10 times lower as compared to 10 ms pulse, the junction temperature was lower as well (307 K at 15 V and 370 K at 25 V). Due to the limited capacitance of the DC-link capacitors in the test-bench further tests at even higher V_{GE} were not carried out.

INFLUENCE OF EMITTER BOND WIRE CONFIGURATION ON SURGE-CURRENT ROBUSTNESS

For all the measured IGBTs, the bond wires are made of aluminium and have a specific cross-sectional area with a diameter of 250 µm that determines their ampacity. During surge conditions, when a high current is flowing through the device, the bond wires will experience an increased current density and high temperatures as a consequence. For high temperatures, the wire resistance increases causing higher voltage drops and power dissipation and describes a positive feedback loop. Further, for a smaller amount of bond wires, the current imprint to the chip's metallization is more inhomogeneous. The typical failure signature for diodes reveals a weak area around the bond wires where the current density and the heat flow is high. Since the Al metallization and the bond wires act as a thermal capacity more bond wires and thicker Al metallization improve the surge-current robustness [11]. Cu metallization and Cu bond wires lead to a further improvement of surge-current ruggedness [15].

To study the influence of a different number of emitter bond wires, 1200 V IGBTs were equipped with 1 emitter bond wire (1EB) and 3 emitter bond wires (3EB) and were compared, see Fig. 6.

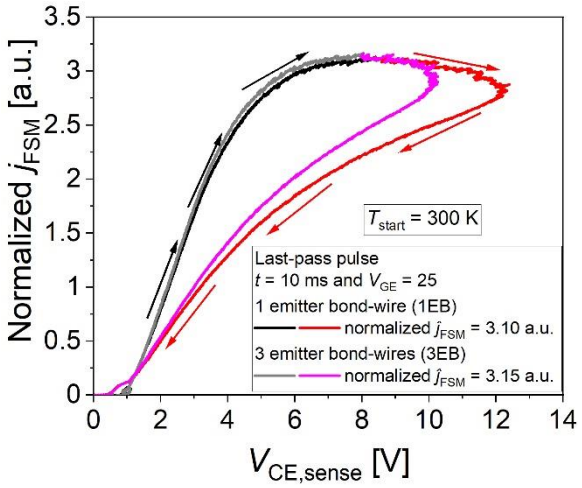


(a) (b)

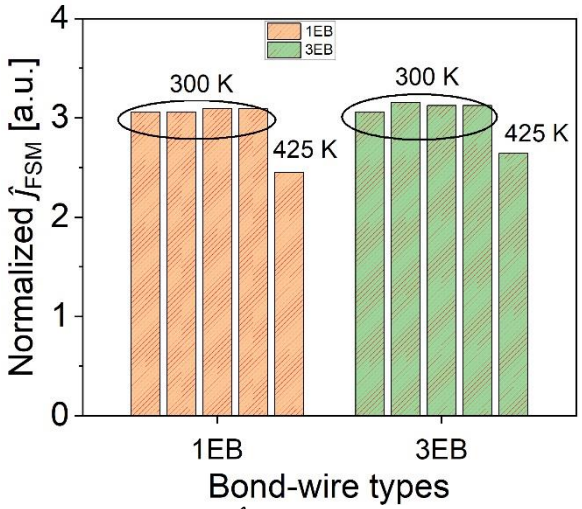
Fig. 6: 1200 V IGBTs used in surge-current measurements with (a) 1 emitter bond wire (1EB) and (b) 3 emitter bond wires (3EB).

The measured last-pass j_{FSM}-V_{CE} phase space diagram for 1EB and 3EB is shown in Fig. 7(a). The IGBT with 1EB shows a higher voltage drop as compared to the 3EB.

Correspondingly, the energy loss is 9% higher for the 1EB DUT for the same surge-current. With respect to the last-pass current, the surge-current capability of the 1200 V IGBT with 1EB and 3EB is the same as shown in Fig. 7(b), at least for V_{GE} = 25 V. The 1EB chip shows a deep crater within the active area due to a possible bond wire melting and open circuit after surge-current destruction with a subsequent arc, see Fig. 8(a). However, the IGBT with 3EB shows a surface melting of the top-side metallization and the bond wires were not yet lifted or melted, see Fig. 8(b). This is different to the findings on pin-diode structures, where a larger number of bond wires is beneficial. However, the observed failure seems to be more chip related due to the starting desaturation process and high intrinsic IGBT losses and is not yet caused by an overload of the bond wires. Hence, surge-current measurements were performed at higher V_{GE} to study the limiting factor of the bond wires.



(a)

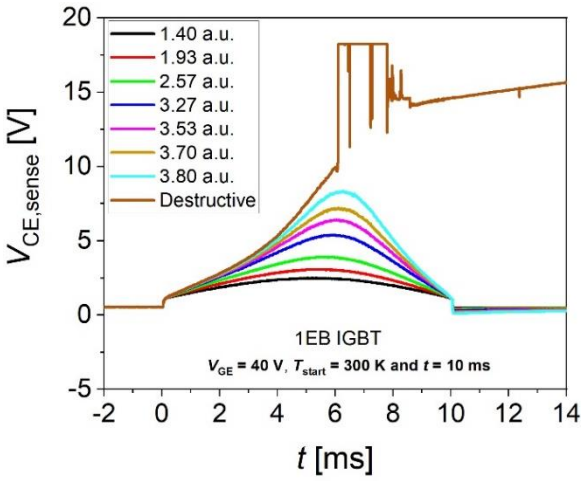


(b) $\hat{J}_{FSM}$ for 1EB and 3EB

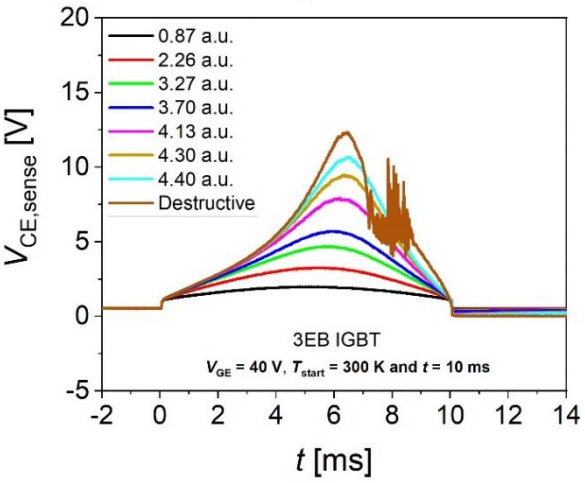
Fig. 7: (a) Measured last-pass normalized surge-current $j_{FSM}(V_{CE})$ characteristic of 1200 V IGBT for 1EB and 3EB. (b) Comparison of the 1EB and 3EB last-pass maximum normalized surge-current density of the 1200 V IGBT. For a given condition of t_p = 10 ms, V_{GE} = 25 V and T_{start} = 300 K.

(a) (b)

Fig. 8: Microscopic pictures of the failed IGBT chips during surge-current at V_{GE} = 25 V with (a) 1EB and (b) 3EB.



(a)

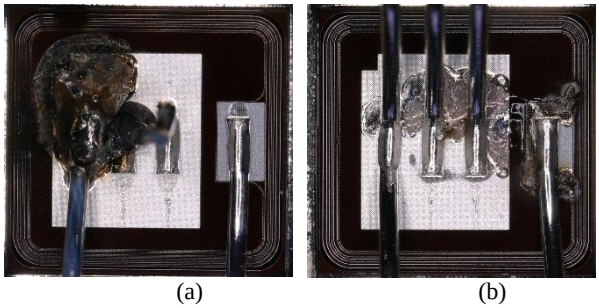


(b)

Fig. 9: Measured $V_{CE,sense}$ across the IGBT for increasing the surge-current density amplitude at V_{GE} = 40 V (a) 1EB (b) 3EB. For a given condition of t_p = 10 ms, and T_{start} = 300 K.

As already indicated above, multiple bond wires provide multiple paths for current flow, which can help to distribute the current more homogeneous across the IGBT. This can result in better heat dissipation and lower localized heating, potentially enhancing the surge-current capability. Thus, the overall current-carrying capacity of the 3EB IGBT is 16% higher at V_{GE} = 40 V as compared to 1EB IGBT, see Figures 9(a) and 9(b). During the destructive pulse, $V_{CE,sense}$ exceeds the measurement range as shown in Fig. 9(a). Here, both IGBTs fail as soon as the devices enter the current saturation regime

[7]. The failure signatures at V_{GE} = 40 V shown in Fig. 10 for 1EB and 3EB are similar to the Fig. 8. The last-pass surge-current of the 1200 V IGBTs for 1EB and 3EB at different V_{GE} are compared in Table 1.



(a) (b)

Fig. 10: Microscopic pictures of the failed 1200 V IGBT chips during surge-current at V_{GE} = 40 V with (a) 1EB and (b) 3EB.

1200 V IGBT			
V_{GE}	Emitter bond wire type	Last-pass surge-current density	I^2t
25 V	1EB	3.10 a.u.	9.25 a.u.
	3EB	3.15 a.u.	9.35 a.u.
40 V	1EB	3.80 a.u.	13.60 a.u.
	3EB	4.40 a.u.	17.50 a.u.

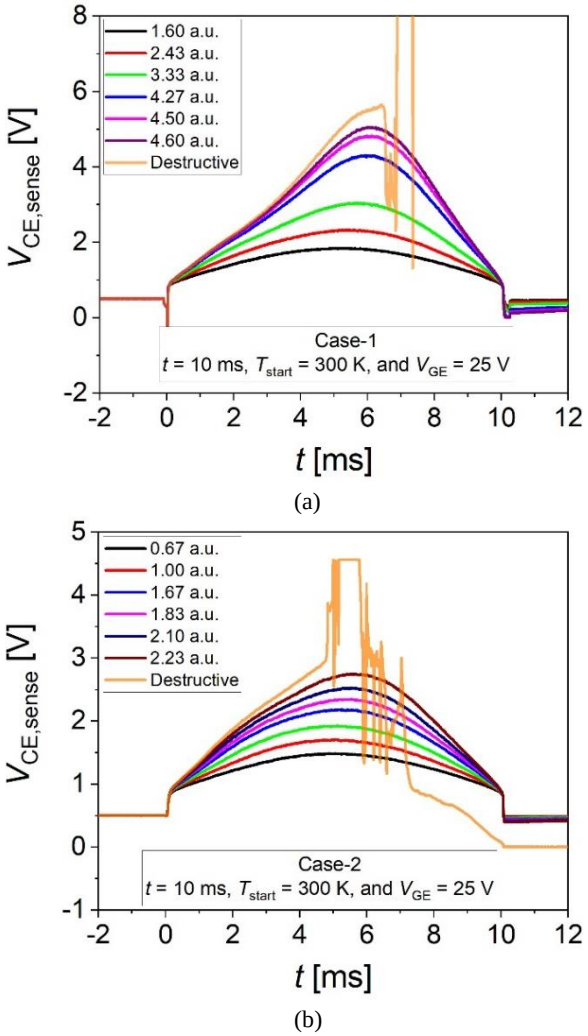
Table 1: Comparison of the last-pass surge-current capability of the 1200 V IGBT at different V_{GE} for 1EB and 3 EB.

Further, the impact of the number of emitter bond wires on surge-current capability was studied for 650 V and 1700 V IGBTs. For this, selected emitter bond wires were cut to reduce the number of bond wires. The 650 V IGBT consists of two segmented emitter pads and each pad has two bond wires. As shown in Fig. 11, for case-1 a single bond wire from each pad was cut and two bond wires from the same emitter segment were cut for case-2. The 1700 V rated IGBT consists of four segmented emitter pads and each pad has three bond wire connections. Here, for case-1, two bond wires were cut, which leads to 33% reduction in the effective wire diameter for the chip and 66% reduction for case-2 as shown in Fig. 14.

(a) (b)

Fig. 11: Surge-current measurements with cut emitter bond wires for 650 V IGBT (a) a single bond wire was cut from each pad (b) two bond wires were cut from same emitter segment.

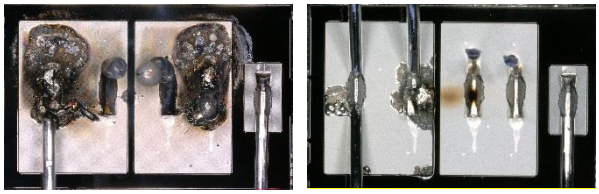
For case-1 (650 V) the measured $V_{CE,load}$ is plotted for the increased surge-current amplitude in Fig. 12(a). Here, the pristine devices refer to IGBTs without any emitter bond wire cut. At V_{GE} = 25 V, the surge-current capacity is reduced by 18% as compared to the pristine device [Fig. 2(b)] for the same measurement condition. This is because of the higher current density. Further, the surge-current capability is drastically reduced by 60% for case-2, see Fig. 12(b). In this case, all the current has to flow via the single emitter pad with two emitter bond wires. According to measurements and failed pictures, the destruction threshold is not determined by the onset of intrinsic conductivity. Due to the limited robustness of the front side contact against excessive heat, the failure signature indicates a temperature-driven destruction mechanism [11]. As shown in Fig. 13, the Al pad near the bonding wire has experienced thermal fatigue [16]. The last-pass surge-current and I^2t of the 650 V IGBT at different cases is summarized in the Table 2.



(a)

(b)

Fig. 12: Measured $V_{CE,load}$ across the 650 V IGBT for increasing the surge-current density amplitude at V_{GE} = 25 V with reduced emitter bond wires (a) case-1 (b) case-2. For a given condition of t_p = 10 ms, and T_{start} = 300 K.

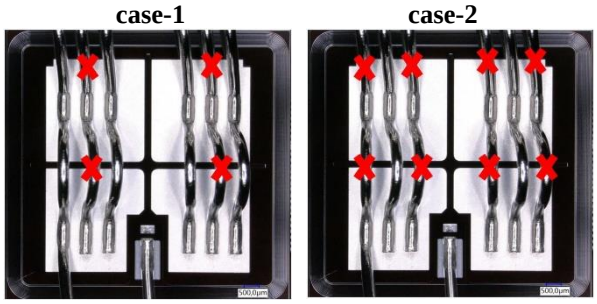


(a) case-1 (b) case-2

Fig. 13: Microscopic pictures of the failed 650 V IGBT chips during surge-current at V_{GE} = 25 V with reduced bond wires (a) a single bond wire was cut from each pad (b) two bond wires were cut from same emitter segment.

650 V IGBT			
V_{GE}	**Emitter bond wire type**	**Last-pass surge-current density**	I^2t
25 V	Pristine	5.63 a.u.	28.80 a.u.
	case-1	4.60 a.u.	17.50 a.u.
	case-2	2.23 a.u.	4.50 a.u.

Table 2: Comparison of the last-pass surge-current capability of the 650 V IGBT at different cases.



(a) (b)

Fig. 14: Surge-current measurements with cut emitter bond wires for 1700 V IGBT (a) 33% reduction in effective emitter bond wire diameters (b) 66% reduction.

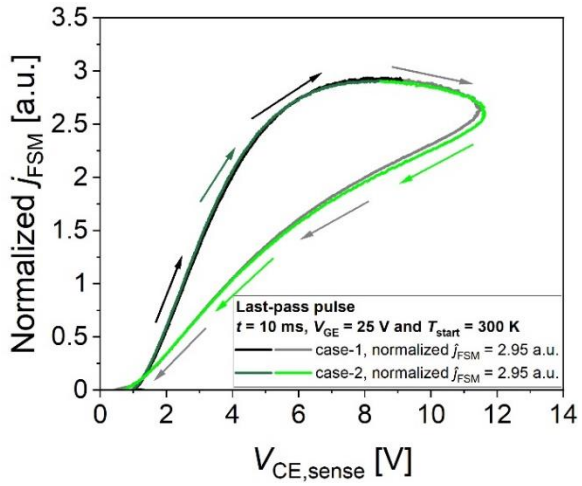
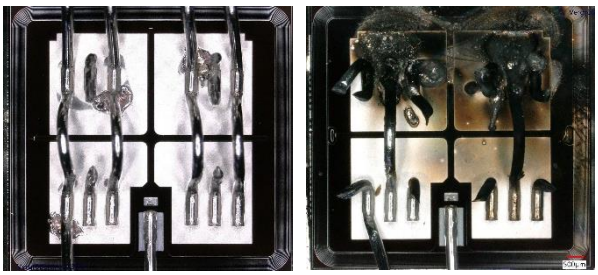


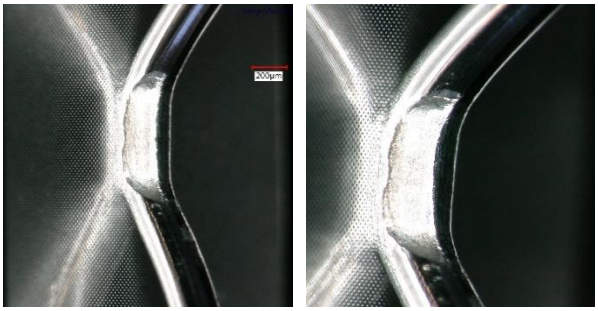
Fig. 15: Measured last-pass normalized surge-current pulse of 1700 V chip on DCB IGBT at V_{GE} = 25 V for case-1: 33% reduction and case-2: 66% reduction. Given conditions: t_p = 10 ms, and T_{start} = 300 K.

For 1700 V IGBT bond wire modification, the impact is not significant. For both cases, a similar surge-current robustness at V_{GE} = 25 V is achieved. There is a slight 3% reduction in the last-pass surge-current as compared to the pristine 1700 V device capability [Fig. 3(b)]. As can be seen from Fig. 15, the IGBT with 66% reduced bond wires shows slightly higher $V_{CE,sense}$ drop as compared to the IGBT with 33% reduction for the same current density. This can be due to the increased resistance of bond wires in combination with higher temperatures. The failure occurs around the bond wires as shown in Fig. 16. The failure signature becomes stronger with less number of emitter bond wires.



(a) case-1 (b) case-2

Fig. 16: Microscopic pictures of the failed 1700 V IGBT chips during surge-current at V_{GE} = 25 V with (a) 33% reduction in effective emitter bond wire diameters (b) 66% reduction.



(a) Before surge-current (b) Last-pass pulse

Fig. 17: Microscopic pictures of an 1EB IGBT(a) Before surge-current pulse and (b) Last-pass pulse with $\hat{j}_{FSM}$ = 310 a.u. Conditions: t_p = 10 ms, and T_{start} = 300 K.

For all different voltage class IGBTs, microscopic images were recorded during the intermediate single pulse surge-current event to study a possible change in Al metallization with a special focus on the bond foot areas. However, there was no distinguishing difference observed on the Al metallization surface between the new device and the same device before reaching the last-pass event. An IGBT with 1EB is displayed in Fig. 17 with a focus around the bond wire wedges area before the surge-current event and after the last-pass pulse.

CONCLUSION

The surge-current behaviour of IGBTs with different rated blocking voltages has been analysed in detail by measurements. For a fixed gate-emitter voltage, the surge-current capability of the IGBT is limited due to the channel pinch-off. For a V_{GE} of 25 V, the tested devices could withstand up to 6 ... 7 times the rated current at starting temperature of 300 K and 5 ... 6 times at 425 K,

respectively. The 650 V IGBT withstands a higher surge-current density as compared to 1200 V and 1700 V IGBTs. However, at V_{GE} of 25 V and 300 K, the 650 V last-pass surge-current density is noticeably reduced compared to its saturation current in the output characteristic at room temperature. For shorter surge-current pulse duration, a higher surge-current can be withstood. For that, the thermal impedance (Z_{th}) of the respective chip and interconnection technology in combination with the self-heating plays an important role.

The number of emitter bond wires does not show any influence on the surge-current capability of 1200 V and 1700 V devices up to gate-emitter voltages of 25 V. For V_{GE} = 40 V, the 1200 V device shows a surge-current capability difference of 16% between 1EB and 3EB IGBTs. On the other hand, the 650 V IGBTs surge-current capability is influenced by the number of bond wires already at 25 V due to its higher saturation current density.

For all the measured conditions, the different voltage class IGBTs fail due to strong V_{CE} desaturation. This confirms our initial statement that there is a trade-off relationship regarding the IGBT's surge-current capability and it's short-circuit capability.

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DIALOG SESSION

On the design of measuring circuit for OCVD method

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Abstract

The article deals with the matter that is often omitted by authors – design of measuring circuit. The most of publications describe theoretical background of the OCVD method or they interpret results obtained on modern SiC or 4H-SiC structures. But correct and relevant results are conditioned by corresponding measuring circuit. Even if the OCVD method is based "just" on recording of voltage response, measuring circuit must fulfill a lot of requirements from high-frequency techniques. Following article tries to explain these techniques.

Keywords: OCVD, lifetime, transient effects, damping, inductance-less sensing.

PRINCIPLES OF OCVD METHOD

In homogenous PN junction, where only one generation-recombination mechanism exists, can appear specific voltage response. This voltage response is detectable immediately after the forward current bias through the PN junction disappears [1]. Voltage response exhibits nearly linear decline and this slope can be used for the determination of so-called charge carrier lifetime [2]. With some simplification the voltage decline on the P-NN+ diode structure is given by the following expression:

$$V(t) = V_P(t) + V_N(t) - \int_0^w E(x;t)dx, \qquad (1)$$

where V_P is the decrease of voltage at PN junction, V_N is the decrease of voltage at NN^+ junction and E is the local electric filed in the basis according equation:

$$E(x,t) = -\frac{J(x;t)}{e(\mu_n+\mu_p)\Delta n(x;t)} - \frac{kT(\mu_n-\mu_p)}{e(\mu_n+\mu_p)\Delta n(x;t)}\frac{d\Delta n(x;t)}{dx}. \qquad (2)$$

Voltages on both junctions are described by Boltzmann's expressions:

$$\frac{p_N(0,t)}{N_A^+} = \exp\left\{\frac{-e[\varphi_P - V_P(t)]}{kT}\right\}, \qquad (3)$$

$$\frac{n_N(w,t)}{N_D^+} = \exp\left\{\frac{-e[\varphi_N - V_N(t)]}{kT}\right\}. \qquad (4)$$

Trash-hold voltages on both junctions P-N and NN^+ are given by the equations:

$$\varphi_P = \left(\frac{kT}{e}\right)\ln\left(\frac{N_A^+ N_D}{n_i^2}\right), \qquad (5)$$

$$\varphi_N = \left(\frac{kT}{e}\right)\ln\left(\frac{N_N^+ N_D}{n_i^2}\right). \qquad (6)$$

When we considered constant lifetime, the concentration of free charge carriers is reduced in time due to the recombination process according following expressions:

$$p_N(0;t) = p_N(0;0)\exp\left(-\frac{t}{\tau}\right), \qquad (7)$$

$$n_N(w;t) = n_N(w;0)\exp\left(-\frac{t}{\tau}\right). \qquad (8)$$

If we can neglect the internal electric field in the basis, we can obtain (based on Eq. 1, 3 and 4) the final equation for lifetime of free charge carriers:

$$\tau = -\alpha\frac{kT}{e}\left(\frac{dV}{dt}\right)^{-1}, \qquad (9)$$

where α is some constant near to 1 in the case of low injection conditions and near to the value 2 in the case of high injection conditions [3].

DESIGN'S ASPECTS OF MEASURING CIRCUIT

The OCVD method is on the most used method for the lifetime determination for most diode structures. The basis of the method is in the idealized theoretical analysis of the charge distribution in the PN junction region and related transient effects in semiconductor bulk. When the influence of measuring circuit on the transport and transient effects in semiconductor is omitted, measured values will deeply differ from the correct (real) values. Ideal waveform of forward voltage $V_F(t)$ on PN junction is marked on the Fig. 1a. The sample is supplied from the constant current source or from the voltage source with serial resistance through the switch S (near to ideal). The PN junction is biased by forward current and constant voltage drop can be observed. After the disconnection of forward current, the forward voltage drop immediately fall down and consequently we can observe linear voltage decline with the constant rate dV_F/dt.

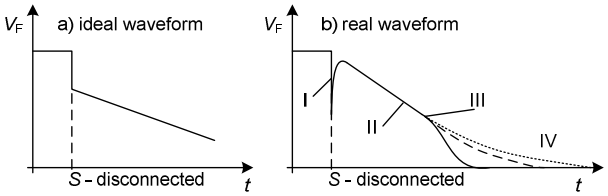

Fig. 1 Ideal and real voltage waveforms at PN junction.

Observed waveforms in real circuits are usually totally different as shown on Fig. 1b. The voltage waveform is (in the region I) distorted by the transient effect coming from the switch S disconnection. The root cause is the fact that the real voltage source is not ideal and has to be substituted at least by the RLC resonant circuit.
In the circuit there is a transient effect of the 2nd order which can be a quasi-periodic process. As the consequence we can observe short-term reversing of forward current in the PN junction and sharp decline of the voltage. Such situation leads to the fast reduction of free charge carriers in the PN junction. But this is a serious violation of theoretical conditions [4].
If the PN junction is biased by the current with dominant diffusion current, the voltage waveform differs at least from the ideal in the region II. The searched lifetime of carriers can be determined by the falling rate of dV_F/dt. The V_F waveform exhibits more slopes in this region if there are multiple generation-recombination processes in the PN junction with longer lifetimes. The derivation process applied during the evaluation of measurement will cause an increase of the noise and distortion; i.e. this effect must be minimized.
In the region III there is significantly visible deviation between real and ideal (linear) voltage decline. One of the possible explanations of this follows: The recombination current of charge carriers is not the dominant part of current flowing through the PN junction. The transient effect starts to be a discharging process of barrier capacity by the diffusion current or external admittance [5], [6].
In the region IV there is a voltage decline with exponential shape when the time constant is given by the total capacity and total conductivity of measured diode. If we considered a connection of external positive susceptance and small conductance, then we can obtain a time constant much bigger than in the region II. It is highlighted by dotted line on Fig. 1b. On the other hand, by connecting huge external conductivity or by the generation of photovoltaic current the time constant is significantly reduced as it is shown by solid line on the Fig. 1b.
When we think about real values of capacities and conductances that could be connected to the measured sample, we can say that specifications on power discrete devices are not strict too much. Externally connected conductance lower than cca 1 μS/cm^2 and capacity lower than 30−50 pF/cm^2 of the PN junction can not significantly affect the measurement and they can cause only the measurement error of percent units. Voltage waveform can be sensed directly by the DSO with sample rate higher than cca 1 GSa/s and with a high-impedance input or with the usage of passive probe [8].
The other important part of the OCVD tester determining its features is the current source. It provides impulses of forward current for the measured sample (DUT) which do not differ from the rectangular shape. Moreover, between pulses the source must have high impedance from the sample (DUT) point of view. The basic parameters of the source (often not specified) are:

- the amplitude of forward current and the di/dt falling slope at the end of pulse (turn-off time),
- damping of the current overshoot at the falling slope,
- duration of the pulse and repeating frequency,
- the generated noise-level and the impedance of the disconnected source.

The oldest and the simplest design of the source is the generator with the diode switch according the principal diagram on the Fig. 2a [1], [7]. The amplitude and the shape of pulses corresponds with the used impulse generator and they reach from 0.1 A to the maximum 1 A with the turn-off time about 10 ns. When the switch is disconnected, its conductance is typically lower than 1 μS and the capacity is in the range units or tens of pF. Such design is useful for the measurement of samples with the area of tenth up to tens of mm^2. For bigger samples it does not supply enough current.
The generator with the mercury (Hg) relay shown on the Fig. 2b presents idealized design [1], [9]. The generator can supply current of several amperes and it provides the fastest disconnection from all mechanical equipments in the order of tens of ns. In the OFF-state its capacity is only several pF and its conductance is several nS [11]. The main disadvantage of Hg-relay is to long time-delay between the coil current and the switching process. This delay significantly limits the maximum frequency of pulses up to several tens of Hz.

In addition, the time delay is random, i.e. the delays between individual processes are variable.

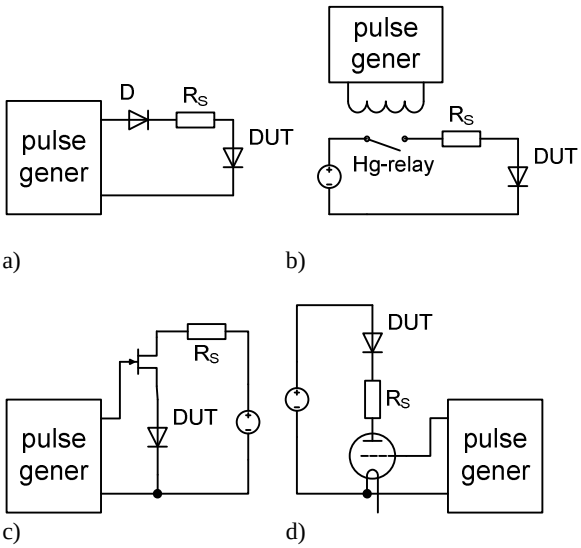

Fig. 2 Possible designs of generator for OCVD circuit.

This effect makes totally impossible synchronous evaluation of consecutive measurement; this technique is usually used by digital signal processing. Described Hg-relays are suitable – thanks to low admittance of disconnected contacts – especially for the measurement on smallest samples. Applying currents about 1 A declines the durability and reliability of contacts.

The generator with semiconductor switch [7] on the Fig. 2c enables very good matching between the circuit and measurement's requirements [5], [11]. With using of small-power switching transistors we can generate pulses with the amplitude of several amperes and turn-off time several ns. With the use of power MOSFETs the pulses with amplitude of 100 A and turn-off time of several tens of ns can be generate. The conductance of the disconnected switch is typically lower than 1 μS and the capacity is in the order units or tens of pF. The disadvantage of this switch is the possibility of current-overshoot generation during the turn-off process and the need to suppress this overshoot. The design of the switch can be adapted for the measurement of samples with the area of 10^{-2} cm^2 up to 10^2 cm^2 or for the measurement with the highest current.

The generator with vacuum tube shown on the Fig. 2d enables to generate pulses with the amplitude several tens of amperes and with the turn-off time tens of ns [7]. When it is disconnected it has negligible conductivity and the capacity units or tens of pF. The serial resistance 10 Ω effectively suppresses overshoots and oscillations during the turning-off process. The main disadvantage of vacuum tube is the need of high-voltage source and tube heating.

REALIZED CIRCUIT

The real switch of forward current can be simply analyzed by means of equivalent RLC circuit shown on the Fig. 3. V_{IN} is the supplying DC voltage source, C is the capacity of disconnected switch S, R is the resistor for current adjustment, L is the parasitic inductance of interconnection, C_D and R_D are components of the admittance of opened DUT. Due to the following relations ($R_D << R$ and $C_D >> C$) the diode in ON-state can be consider as a short circuit and the transient aperiodic effect during turning-off can be described as follows (10) and (11):

$$\frac{d^2 i(t)}{dt^2} + \frac{R}{L}\frac{di(t)}{dt} + \frac{i(t)}{LC} = 0, \tag{10}$$

$$\sqrt{\frac{L}{C}} < \frac{R}{2}. \tag{11}$$

The estimation $R \sim 1\ \Omega$, $C \sim 100$ pF can be used for currents in the circuit higher than 10 A. To keep the condition for aperiodicity (11) it is necessary to ensure $L < 0.025$ nH; that is practically impossible. The solution by increasing the resistivity R or the capacity C is not possible; the supplying voltage will increase too much, and voltage response will distort [9].

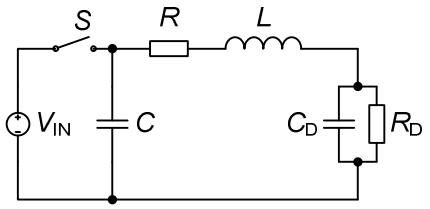

Fig. 3 Real switch presented as an RLC circuit.

The resonance can be damped by R_D that is connected to the inductance L in parallel [6]. The oscillations are minimized when the resistivity is closed to the reactance of the L at the resonance frequency of the circuit. For the real values from the circuit on Fig. 3 the reactance of L is about 3.16 Ω (R_S = 0.4 Ω; C_P = 400 pF; L_S = 4 nH; self-resonance frequency is 125 MHz). The voltage and current waveforms were simulated in LTspice according simplified circuit from the Fig. 4. Different parasitic inductances and different damping were reflected.

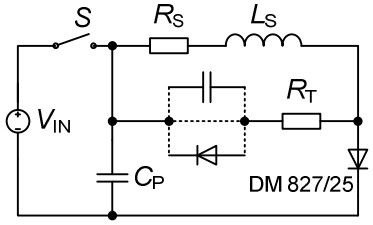

Fig. 4 Substitution circuit of the switch in LTspice simulation.

Waveforms on the Fig. 5 are shifted in time intentionally for better understanding. The first waveform from the left shows the real circuit with optimal damping. Waveforms are overshoots-free. The 2nd waveform shows the circuit with the same real inductance and low damping. There is no visible periodic oscillation. The 3rd waveform shows the circuit with big inductance and optimal damping. Both waveforms (voltage, current) show aperiodic overshoot. The last fourth waveform shows the circuit with big inductance and minimal damping. Both (voltage and current) waveforms show periodic damped oscillations. It is useful to connect the damping resistor with the main circuit through separating capacity or diode. Then the resistor is loaded by current only during overshoots. This solution will reduce power losses and does not affect forward current through the R_S except rising and falling slopes of the pulse.

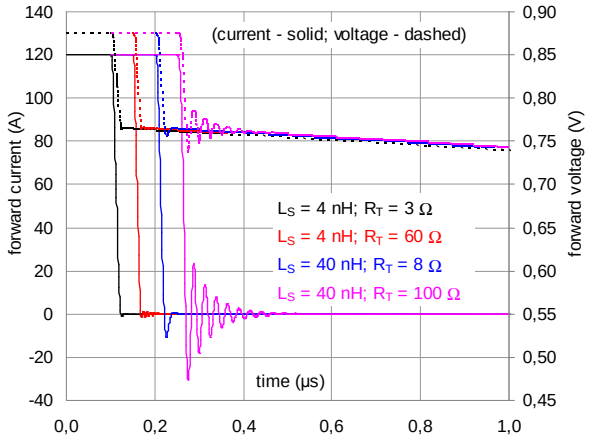

Fig. 5 LTspice simulation of the circuit on the Fig. 4.

Realized circuit with depicted real and parasitic parameters is shown on the Fig. 6. Two parallel connected SiC MOSFETs type C3M0075120 are used as a switch S. Both MOSFETs are controlled by trigger signal from galvanic-isolated generator. The maximum forward current I_F through DUT is limited by series resistance R_S (0.36 Ω). Resistor is made by three parallel connected power foil-resistors BDS100 produced by TE-Connectivity with the nominal value of 1 Ω and inductance 6 nH [12]. Thus, the maximum forward current I_F is set to 140 A with supplying voltage 52 V. The voltage source V_{SS} is equipped by blocking capacity C that consist from four electrolytic capacitors 10 mF/50 V type B41231 connected in parallel; 16 electrolytic capacitors 1 mF/50 V type WCAP-ASLI and four capacitors 10 µF/63 V type F161. Individual capacitors are interconnected "as a matrix" by means of parallel-plate transmission line with the dimension 100×120 mm and characteristic impedance about 3 Ω. The total capacity is cca 60 mF; ESR is cca 1 mΩ and self-inductances are lower than 1 nH. The layout of capacitor battery is on the Fig. 8. Elements L_{S1} and L_{S2} represent the inductances between tested diode and the measuring circuit. Both elements are realized as a "triplate stripline" with the characteristic impedance cca 2 Ω and with the length 100 mm. This connection shows the total inductance cca 2 nH plus the inductance of R_S. Two damping resistor R_{T1}, R_{T2} are 2.2Ω resp. 1.5Ω and are made by parallel combination of SMD thick-film resistors 22 Ω/1 W type CRCW1218.

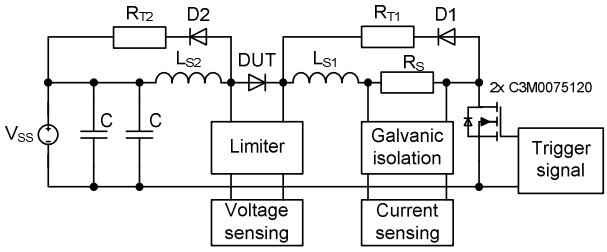

Fig. 6 Circuit design of the real OCVD tester.

Waveforms on PN junction $V_{DUT}(t)$ and $I_{DUT}(t)$ were observed by the oscilloscope KEYSIGHT DSOX2022A that provides bandwidth 200 MHz, sampling rate 2 GSa/s and 8bit resolution (see Fig. 7). Waveforms were recorded with the averaging function (64×). It makes better the S/N ratio by approx. of 20 dB in comparison with individual recording.

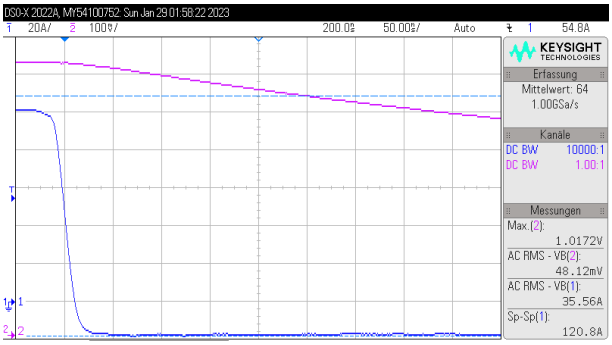

Fig. 7 Waveforms of $V_{DUT}(t)$ and $I_{DUT}(t)$ recorded by DSO.

The limiter protects the oscilloscope's input against overvoltage coming from the DUT's outlets when the circuit disconnect. The limitation voltage level is ±5 V; the time-constant is lower than 30 ns. Current waveform is evaluated as a voltage drop on the resistor R_S. To the R_S is as a shunt connected another resistor and its current (few hundred of mA) is sensed by the current probe Agilent N2774A. In this way the galvanic separation between the oscilloscope and current probe is ensured. The rate of falling slope dI_{DUT}/dt is cca 4 A/ns.

Fig. 8 Layout of the inductance-less battery of capacitors.

On the Fig. 9 there are really measured and simulated waveforms of $V_{DUT}(t)$ and $I_{DUT}(t)$ obtained during the measurement on soft commutated diode DM 827/25 and in the circuit with optimal damping. There are no significant differences between measured and simulated curves. The measuring circuit ensures forward currents in the range from 1 A up to 140 A and with the pulse length 100 µs up to 1 ms and repeating frequency 10 Hz. Proper combination of the pulse length and repeating frequency is assumed to keep the total power bellow 100 W.

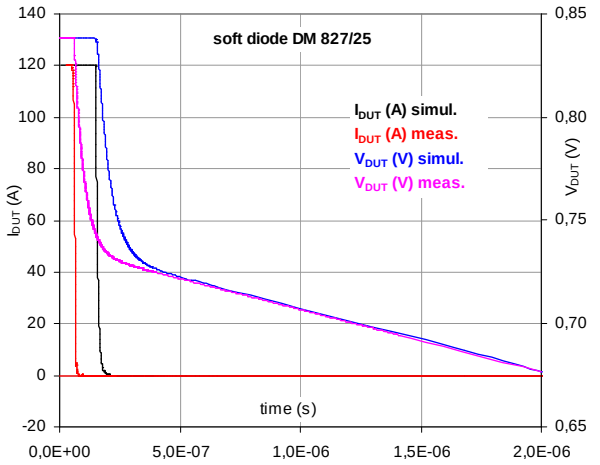

Fig. 9 The comparison of simulated and measured waveforms on soft commutated diode DM 827/25 (irradiated device).

MEASUREMENTS AND INTERPRETATIONS

The circuit shown on the Fig. 6a and described in previous chapter has been realized in the 2022 and beginning the 2023 the verification measurements started. The main goal of verification was to identify the lifetimes at high-injection conditions and compare them with expected values. The next task was to determine the influence of forward current I_{DUT} on the measured lifetime. The current was chosen in the set 1-10-100 A. Power diodes with totally different design and parameters were chosen as the samples to obtain results in a wide range of lifetimes. Three main types are described in the text bellow.

The samples' current I_{DUT} was controlled by supplying voltage V_{SS}. The waveforms of forward voltage drop V_{DUT} were sensed by the oscilloscope DSOX2022A as it is described in previous text. Waveforms were used for numeric calculation of lifetimes according (9). The importance of proper and noise-free sensing of voltage signals is obvious. Measured levels are hundred mV high and declines in time. The typical 8bit resolution of commonly used AD converters is often not enough for exact calculation. The adjacent samples differ just by the LSB value or less even they are the same. Then the calculation according (9) failed. This is the root-cause of quantization noise shown on the Fig. 13 and Fig. 15.

Measurement on 2' avalanche diode

Large avalanche diodes are mostly designed as P-i-N diodes with thick Si-wafer (750 µm) and with the initial bulk resistivity in the range 150-250 Ωcm. Lifetimes are long and not controlled. Values in the order of hundred µs are expected. This is given only by the cleanness of initial bulk and diffusion process.

In the area of linear decline of V_{DUT} (cca 1 ms on the Fig. 10) we can obtain from the Fig. 11 relatively constant and I_{DUT} independent two lifetimes ($\tau_{n0} \sim 300$ µs; $\tau_{p0} \sim 120$ µs). The quantization is given by sampling and following digital processing.

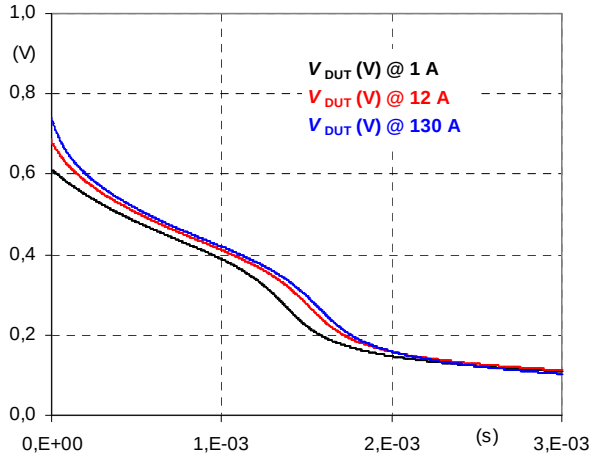

Fig. 10 Decline of forward voltage V_{DUT} on the 2' avalanche diode for three different forward currents I_{DUT} (not shown).

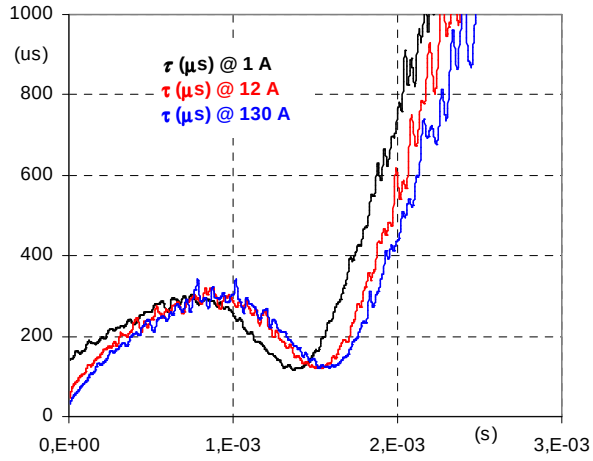

Fig. 11 Numerically counted lifetimes for the avalanche diode biased by the forward current density 0.05; 0.5; 5 A/cm^2.

Measurement on 40mm soft diode

Fast diodes with soft commutation are mostly designed as a junction with compressed electric field with the wafer thickness 400-500 µm and initial resistivity 100-150 Ωcm. The lifetime is reduced to units or tens of µs by electron beam irradiation or by accelerated protons or by the diffusion of heavy metals (like Au, Pt, etc).

In the area of linear decline of V_{DUT} (cca 50 µs on the Fig. 12) we can obtain from the Fig. 13 relatively constant and I_{DUT} independent lifetimes (τ_{n0} ~ 15 µs, τ_{p0} ~ 16 µs). The quantization is given by sampling and following digital processing (especially at the time above 100 µs).

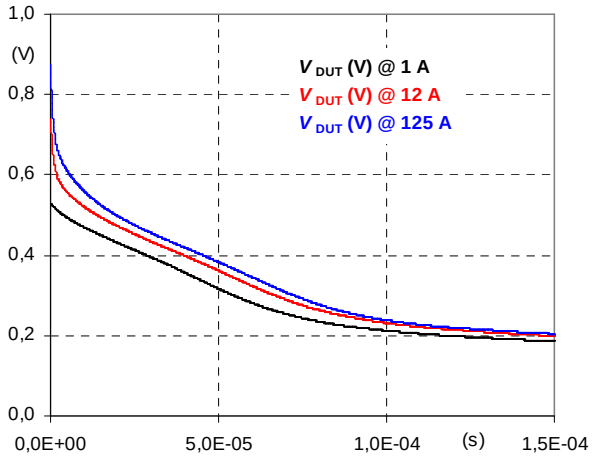

Fig. 12 Decline of forward voltage V_{DUT} on the fast (soft) diode for three different forward currents I_{DUT} (not shown).

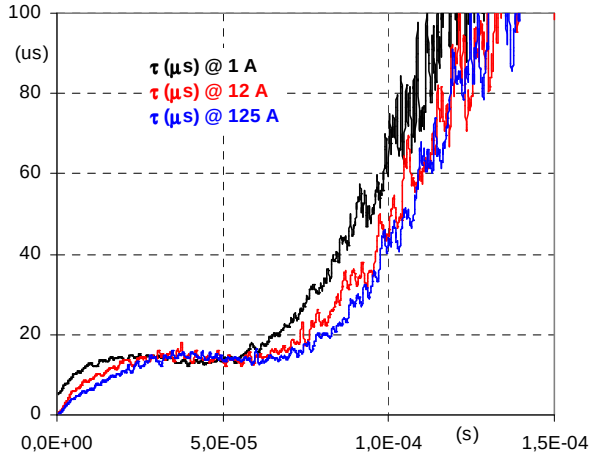

Fig. 13 Numerically counted lifetimes for the soft diode biased by the forward current density 0.1; 1.0; 10 A/cm^2.

Measurement on 2.5' welding diode

Welding diodes are very specific power rectifier diodes. Their design is optimized for extremely high forward current density (I_{FAV} ~ 10 kA). This is paid by very low reverse breakdown voltage; V_R is typically 400 V. Diodes are made from Si-wafer with the thickness about 200 µm and with very low initial bulk resistivity (10 Ωcm). The carrier's lifetime is not controlled and is generally very low. The typical value is units of µs.

In the area of linear decline of V_{DUT} (cca 50 µs on the Fig. 14) we can obtain from the Fig. 15 two values of lifetime (τ_{n0} ~ 14 µs, resp. τ_{p0} ~ 9 µs). They don't depend on the I_{DUT} current. The quantization is given by sampling and following digital processing.

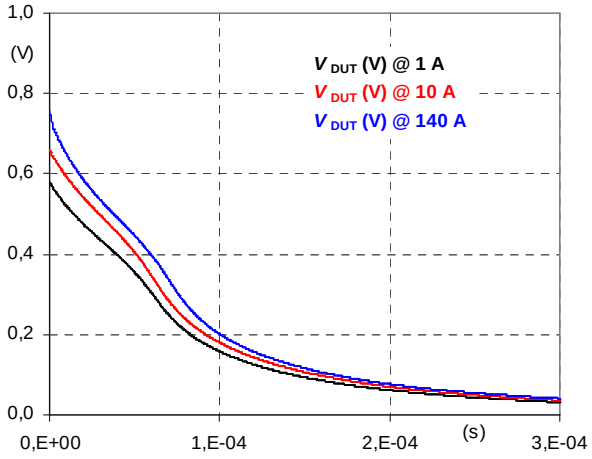

Fig. 14 Decline of forward voltage V_{DUT} on 2.5' welding diode for three different forward currents I_{DUT} (not shown).

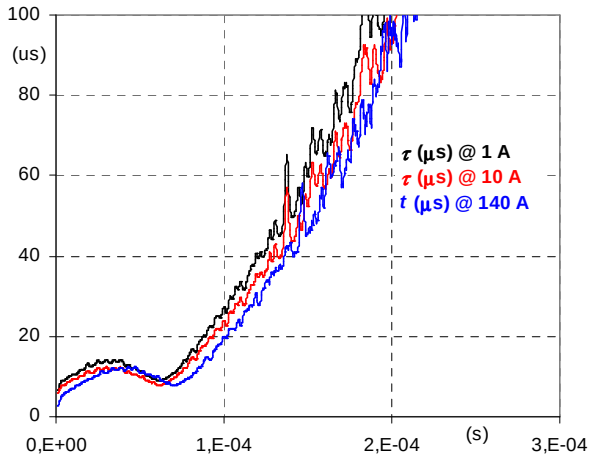

Fig. 15 Numerically counted lifetimes for the welding diode biased by the forward current density 0.05; 0.5; 5 A/cm^2.

SUMMARY

This article describes design's issues and main rules of the testing circuit for the OCVD method. The attention is paid especially to proper damping and suppressing of all undesired oscillation and transient effects that can influence measured waveforms and numerically processed lifetimes. The correctness of described recommendation is documented by the measurements of the set of different samples. They exhibit totally different lifetimes. The measurements were performed with the current density varying from 0.01 A/cm^2 to 10 A/cm^2. Expected lifetimes of electrons (τ_{n0}) and holes (τ_{p0}) at high-level injection were confirmed. Based on the Figs. 11, 13 and 15 we can say that the applied current density does not have any significant influence on the measured carrier's lifetime. Forward current affects only the very beginning of the voltage transient waveform.

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Sulphur Related Corrosion in Power Modules and its Impact on the Switching Performance

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Abstract

High power semiconductor modules, exposed to polluted (i.e. H_2S) and moist climates can experience corrosion at the packaging materials. Sulphur and copper will form Cu_2S-dendrites in the insulation trenches of the substrates, which are able to short the insulation distance. But, previous experiments pointed out, that modules with excessive dendrite growth are able to withstand high blocking voltages under DC-bias. While most IGBTs will operate under switching operation with fast transients, ohmic connections at insulation distances will change the situation tremendously. For this study, 1200 V silicon-IGBT-modules in a standard package were preconditioned in an accelerated corrosive gas test and will be operated in a switching test bench to verify corrosion related performance issues in active operation.

Keywords: IGBT, Power Electronics, Reliability, Corrosion, Robustness, H_2S, Hydrogen Sulphide, Humidity

INTRODUCTION

The extended usage of power electronic components in various applications has led to a wider spectrum of mission profiles and stressors within the useful lifetime of these parts. Especially frequency converters and power supplies are often exposed to harsh climatic conditions containing high relative humidity [1] or reactive pollutants like sulphur [2], which lead to a reduced service life. Many reliability investigations on power electronics are focused on silicone gel (Si-gel) potted power semiconductor modules and their degradation behaviour under harsh climates. Moisture induced aging of these devices is well studied and the failure mechanism as well as the influence on the electrical performance are documented [3].

For corrosion products related to ionic contamination, the situation is different and rather complex. If moisture and atmospheric pollutants like sulphur dioxide (SO_2) or hydrogen sulphide (H_2S) are present, copper-sulphide-dendrites are formed in the insulation trenches on the copper-ceramic-substrate [4, 5], leading to ohmic conduction paths between the copper pads. Under dry DC-conditions, the leakage current of the chip conceals the parasitic current through the dendrites and therefore, no sulphur related degradation can be measured [5]. Based on these experiments, standard industry silicon-IGBTs are preconditioned in accelerated tests and split into different groups to distinguish between degradation states and mechanisms. To verify critical operation conditions, an IGBT turn-off switching test at high currents is performed afterwards.

CLIMATE RELATED DEGRADATION OF IGBTS

Power modules are widely tested under accelerated conditions in lifetime tests with focus on environmental stressors such as temperature and relative humidity. Furthermore, a high voltage bias close to the nominal voltage (V_{nom}) increases the stress [6] and leads to a more application relevant testing scenario. While testing under high humidity, the chip interface is attacked and aluminium corrosion at the edge termination causes a reduction of the blocking capability [3, 6]. Beside the aluminium corrosion, electro-chemical migration (ECM) can be observed [6] due to contamination in the manufacturing process, where metals form a conductive path at areas of high electrical field. If the contamination level is low and the potting material shows a sufficient adhesion on the surface, aluminium corrosion is the predominant failure mechanism and no ECM can be found at substrate level.

If a reactive pollutant like H_2S is added to the test, the degradation mechanism changes dramatically and inflicts the copper-ceramic-substrate. To keep the explanation of the relevant reaction equations as basic as possible, a Cu-surface is used instead of a Cu_2O-layer on top of the substrates. Fig. 1 illustrates the situation in the power module with a direct bonded copper (DBC) substrate, covered with Si-gel [4]. Both, H_2S and H_2O are able to diffuse through the gel matrix and will react with the metallic packaging materials.

Similar to moisture, sulphur can be stored inside the gel and therefore, corrosion can occur much later than the actual contamination.

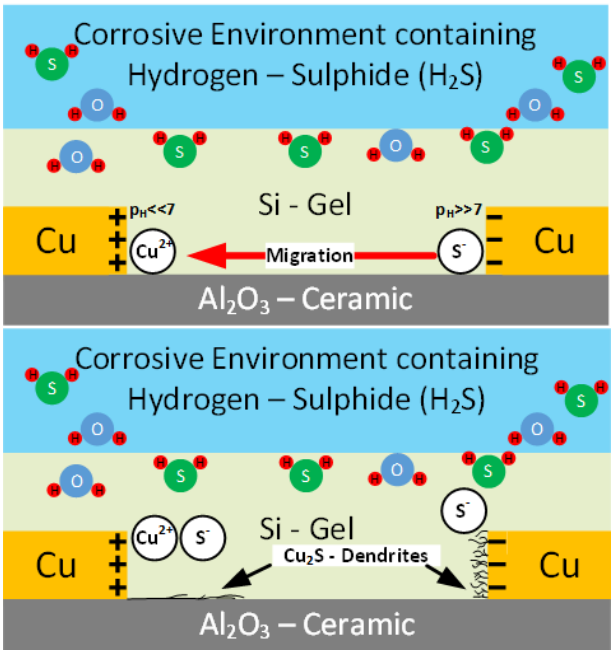

Figure 1: Mechanisms of H_2S-induced corrosion at a silicone-gel covered DBC-substrate, bias with high voltage

The Cu-surface is able to react with H_2S at high relative humidity and forms CuS/Cu_2S (copper sulphide) [7]:

$$2Cu + H_2S \rightarrow Cu_2S + H_2 \quad (1)$$

$$Cu + H_2S \rightarrow CuS + H_2 \quad (2)$$

The reaction to Cu_2S is thermodynamically more beneficial [7] and therefore, it is more likely to be found at the interface. The built-up surface layer will not cause major problems in the first place but the situation changes at the insulation trenches of the substrates, where a high electrical field is present and a galvanic cell can be formed. Referring to fig. 1, the H_2S molecule will reach the copper cathode through the gel and reacts to:

$$H_2S \rightleftarrows 2H^+ + S^{2-} \quad (3)$$

As a result of the high electrical field, the negatively charged sulphur ion will migrate to the anode:

$$Cu \rightarrow Cu^+ + e^- \quad (4)$$

$$2Cu^+ + S^{2-} \rightarrow Cu_2S \quad (5)$$

The positively charged anode will form Cu^+ (4) ions, which are attracted by the electrical field and will move towards the cathode. Due to the high concentration of sulphur ions in the anode area, the Cu-ions will react with the S-ions to Cu_2S (5). This leads to the growth of a dendritic structure from the anode to the cathode on top of the ceramic surface over time. These types of structures are able to grow over the full length of the insulation trench and reach the cathode [5]. The results from [5] indicated a secondary effect at the cathode, which is much faster than the anodic growth. In general, Cu_2O-dendrites on DBC-substrates covered with Si-gel are not reported as long as the adhesion is intact. Therefore, a classical ECM like described in [8] cannot explain the structure, because the Cu-ion itself is unable to reach the cathode to form a dendrite. Nevertheless, this secondary structure at the cathode is present after a short exposure to high relative humidity and high H_2S-concentrations. Furthermore, this effect saturates over time and inflicts the complete cathodic area [5] from bottom to top of the pad. It is not reported, that these structures can grow across the full trench and therefore, this will be handled as a testing artefact, which is able to reduce the insulation distance by a certain amount.

Discussion:

The documented corrosion effects, related to high humidity, are widely accepted and there are solutions available to avoid this degradation on chip level [9]. While the humidity driven failure mechanisms are understood, the influence of ionic contamination changes the situation. The primary corrosion mechanism forms an anodic dendritic structure due to the high level of ions around the anode. This effect faces a threshold due to the time constant of diffusion through the gel and the growth starts after H_2S reaches the metallic interface. ECM in the presence of ionic contaminants is well documented [10, 11], but these experiments are performed without insulation materials on top of the metallic contacts. If a surface coating is applied and the adhesion is intact, ECM like in [10] will not occur in that manner. First of all, Si-gel can store a much higher concentration of H_2O [12] than the surrounding air and the same might be valid for the H_2S-concentration. Therefore, the high concentration will lead to precipitates [10, 11] and this results in anodic, rather than cathodic growth. In this case, the mechanism is described as an anodic migration phenomenon (AMP) [13] and is closer to the formation of conductive anodic filaments (CAF) [14], than to ECM-based dendrite growth.
As stated in [5], the impact of the resulting copper structures on the electrical behaviour is not conclusively identified. Even after excessive growth, the power modules in [5] were able to withstand their rated blocking voltage and the chip leakage current still covered the parasitic current of the AMP completely.

DESIGN OF EXPERIMENT AND TEST SETUP

When it comes to accelerated testing of power semiconductor modules, a DC-bias is generally used to stress the devices in an easily controlled way. For applications, this operation and stress conditions are not reflecting the actual mission profile and therefore, a corrosion product, which is uncritical under DC-conditions, might be a problem when it comes to switching events at high currents.
For that purpose, 1200V IGBT-modules were preconditioned in an HV-H^3TRB- and a single corrosive gas test to have different states of degradation. These preconditioned devices were operated in a turn-off switching test, the same that is part of the post production

Split	Quantity	Test Conditions	Test Time	Degradation
HV-H³TRB	8	85°C/85RH/80%V_{Nom}	2000h	Not measurable
H_2S-400h	2	40°C/93%RH/80%V_{Nom}/ 50ppm H_2S	400h	Cathodic dendrites
H_2S-1000h	2	40°C/93%RH/80%V_{Nom}/ 50ppm H_2S	1000h	Anodic & cathodic dendrites
H_2S-1500h	3	40°C/93%RH/80%V_{Nom}/ 50ppm H_2S	1500h	Anodic & cathodic dendrites
Humidity Ref.	2	40°C/93%RH/80%V_{Nom}	1000h	Not measurable

Table 1: Overview of splits, quantities and test conditions. Split 1 (HV-H³TRB), will be just tested dynamically after the preconditioning.

testing to verify the influence of life time testing on the dynamic behaviour.

Devices under test

A 1200V/750A ED-Type IGBT-module (fig. 2) from *SwissSEM Technologies* was used for this investigation. These types of packages:

- ED-Type (SwissSEM)
- EconoDUAL (Infineon)
- LoPak (Hitachi Energy)
- Etc.

are preferable to use for this kind of testing due to the package design. First of all, these types come with a removable lit as well as a rather open package design. The removable lit, allows a sufficient monitoring of the corrosion state in intermediate measurements without damaging the devices. Furthermore, the corrosion rate can be enhanced by removing the lit in the corrosive gas test to expose the surface of the Si-gel directly to the environment [5].

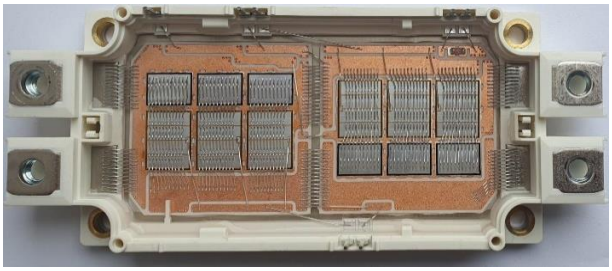

Figure 2: Device under test: ED-Type IGBT-module

Test procedure and setup

The corrosive gas testing is executed in a climate chamber according to IEC60068-2-43 at 40 °C, 93 % relative humidity (RH) and 50 ppm H_2S. Referring to [5], this climate shows a sufficient acceleration of the desired corrosion mechanism without triggering moisture induced degradation at the chip interface. Another interesting aspect is the calibration of the chamber with sensor elements. This is just useful, if the temperature is ≤ 40 °C, to allow the usage of chemical sensors directly in the chamber. The high relative humidity (> 90 %) will lead to an early degradation of the sensing element, but a measurement duration of at least 48 h is possible. Fig. 3 shows the calibration run for > 48 h with an analog gas- (measurement range up to 100 ppm), and a digital humidity sensor (RHT-sensor). While the temperature and relative humidity stabilises after ~ 1 h, the gas concentration is not fully stable over this test time. This can be explained by the critical relative humidity in this climate, which slightly exceeds the limit of the sensor and at 40 °C, this sensor operated at the maximum possible temperature. Using the gas sensor beyond this time frame leads to insufficient results and is not done for this experiment. In contrast, the RHT-sensor with protected interconnections can last for much longer time periods.
The climate verification was combined with a corrosion indicator calibration. Cu-stripes were prepared according to IEC60068-2-60 and the weight gain as well as the weight loss are used as an indication for the corrosion rate. As described in [5, 7, 15], a Cu_2S-surface is formed when exposed to the harsh climate inside the chamber. The gain in material leads to an increase in weight and this is measured by a high-resolution scale (10 µg) before and after the test cycle. Furthermore, the corroded indicators were cleaned according to EN ISO 9226:2012 and a weight loss measurement was executed additionally.
Dendritic growth, i.e. a directed growth, is just possible under the presence of a high electrical field at the

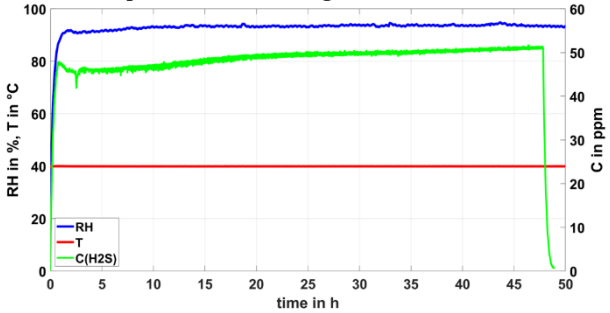

Figure 3: Calibration measurement of climatic conditions inside the chamber with H_2S- and RHT-sensor

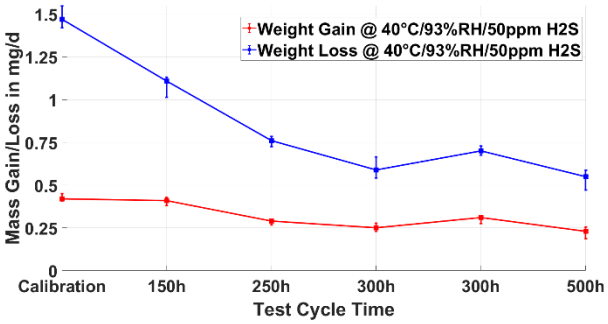

Figure 4: Corrosion monitoring with Cu-stripes exposed to 40 °C / 93 % / 50 ppm H_2S.

interface. Therefore, a high-voltage (80 % V_{nom}) data acquisition system with eight separate channels was used to monitor the status of the devices and to execute a turn-off procedure in case of a failure. For this experiment, just the high-side switches were connected to high voltage due to the auxiliary collector layout of the substrate, which leads to another possible degradation path. An optical inspection after each test cycle (fig. 4 & 5) was done to control the corrosion state of the device. In tab.1, different corrosion states were separated with respect to the corresponding structure (fig. 1). In parallel, tests at 85 °C, 85 % RH, 80%V_{nom} and 40 °C, 93 % RH, 80 % V_{nom} were executed to have a reference under moisture stress only.

The preconditioned samples were tested in a static and a dynamic testbench to compare the electrical properties before and after the test. In the dynamic testbench, a turn-off event at $2 \cdot I_{CES,\ nom}$ is measured with an expected voltage overshoot reaching the total voltage of 1200 V. This procedure is a pass-/fail-test and will just verify the a fully operational condition after accelerated aging testing.

PRECONDITIONING RESULTS

Corrosion monitoring with Cu-stripes

Fig. 4 shows the result of the corrosion monitoring with Cu-stripes for all test cycles with the corresponding weight gain and loss. The calibration run was fully sensor monitored (fig. 3) and the test cycles up to 1000 h were observed with an RHT-sensor (the sensor failed in the last test cycle). Overall, the percentage weight loss per day is much higher than the measured weight gain. This can be explained by the brittle surface of the Cu-stripes and the resulting mass loss inside the chamber. After each test cycle, Cu_2S-flakes were found all around the chamber and in the condensed water at the tester output. Furthermore, the gain and loss rate are nearly constant for test durations > 250 h. On the contrary, the calibration run at 50 h and the first test cycle at 150 h show a significant difference in the mass loss per day. The corrosion rate of Cu in H_2S containing moist air is highly non-linear due to the passivation effect of Cu_2O and Cu_2S. With increasing layer thickness, the supply of Cu is retarded and therefore, the growth rate is decreasing. In [7], the growth rate is divided into a linear part and a parabolic part with respect to the metal surface over the test time. The same effect can be assumed for the results in fig. 4, with a highly decreasing rate from 50-250 h of test cycle time. Especially the first hours of testing have a high influence on the layer thickness [15] and the resulting corrosion products in the weight gain and loss measurement.

These measurements can now be used to generate an impression of the acceleration factor in relationship to the application relevant climatic conditions. Due to the lack of reliable field data with focus on H_2S-pollution, the corrosion categories defined in EN ISO 9223:2012 are used. The values from fig. 4 are used for a calculation of the corrosion velocity according to EN ISO 9226:2012:

$$r_{corr} = \frac{\Delta m}{A \cdot t} \qquad (6)$$

As a result of the significant difference in the mass loss for shorter test cycles, Δm is averaged from the last four test cycles (similar loss rate) resulting in:

$$r_{corr} = \frac{\Delta m}{A \cdot t} \approx 3000\ \frac{g}{m^2 \cdot a} \qquad (7)$$

Tab. 2 shows the corresponding acceleration factors for Cu-corrosion based on the calculation (eq. 7) for each corrosion category according to EN ISO 9223:2012.

The acceleration factors in tab. 2 are of course just an estimate for the correlation between the testing and the application. But, with these categories, a corrosion state in the test can be extrapolated to the field, if the category is know. E.g. 1000 h in the test at the climatic conditions from fig. 3 & 4 would lead to a corrosion state similar to 14 – 30 years in category C4 (based on corrosion products with just one contaminant and constant conditions).

IGBT-module preconditioning

The test matrix in tab. 1 is based on the optical corrosion monitoring after each test cycle. At 400 h of accumulated

Category	$r_{corr,Cu}\ [\frac{g}{m^2 \cdot a}]$	Acceleration Factor
C1	≤ 0.9	≥ 3333
C2	0.9 – 5	3333 – 600
C3	5 – 12	600 – 250
C4	12 – 25	250 – 120
C5	25 – 50	120 – 60
CX	50 – 90	60 – 33

Table 2. Corrosion categories according to ISO9223 with the corresponding acceleration factors for the chamber climate

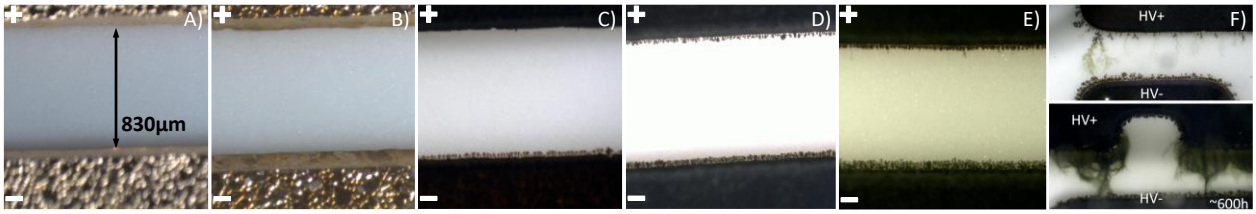

Figure 5: Preconditioned samples with different corrosion states in comparison to a reference state F) at the same climate [5]: A) Initial status, B) 2000 h HV-H³TRB at 85 °C / 85 % RH / 80 % V_{nom}, C) 400 h at 40 °C / 93 % RH / 50 ppm H_2S / 80 % V_{nom}, D) 1000 h at 40 °C / 93 % RH / 50 ppm H_2S / 80 % V_{nom}, E) 1500 h at 40 °C / 93 % RH / 50 ppm H_2S / 80 % V_{nom}

testing time, each sample showed the cathodic dendritic structures, described in fig. 1. Two samples with this specific corrosion state, showed in fig. 6 C), were removed from the test. In fig. 5 D), the final state after 1000 h of testing time is shown, with a clear evidence of beginning anodic growth as the main degradation mechanism. Due to the small amount of very short dendrites, the testing time for the remaining samples was extended up to 1500 h (fig. 5 E)). Overall, the growth rate is significantly lower compared to the result in [5] (fig.5 F)). In both test campaigns, comparable packages, the same test equipment (but different calibration) and the same climatic conditions were used. The only difference is the voltage class of the modules and the resulting lower test voltage. In [16], the electrical field is characterised as a predominant acceleration factor for ECM, with a defined threshold for every migration mechanism. A smaller electrical field can lead to highly delayed growth and might also change the composition of the resulting structures. In this case, the average insulation distance at the substrate is around 830 µm, which would lead to the following electrical field:

$$E = \frac{V}{d} = \frac{960V}{0.83mm} \approx 1150\frac{V}{mm} \qquad (8)$$

In the previous publication [5] on similar modules, the insulation distance was smaller and the bias voltage higher and therefore, the electrical field was 27 % higher. Furthermore, the surface of the substrate in fig. 5 is much cleaner (from the optical view) compared to the previous publication [5]. These factors led to the rather small dendrites and the overall high remaining insulation distances at the substrates even after 1500 h of exposure. The two humidity only splits showed no degradation after the preconditioning and the substrates just indicate a higher Cu_2O-surface thickness compared to the initial state (fig. 5).

POST TEST CHARACTERISATION

Static results

The samples of the corrosive gas testing as well as the humidity references at 40 °C and 93% RH were characterised before and after the treatment. Each sample was measured in a post-production test cycle and a

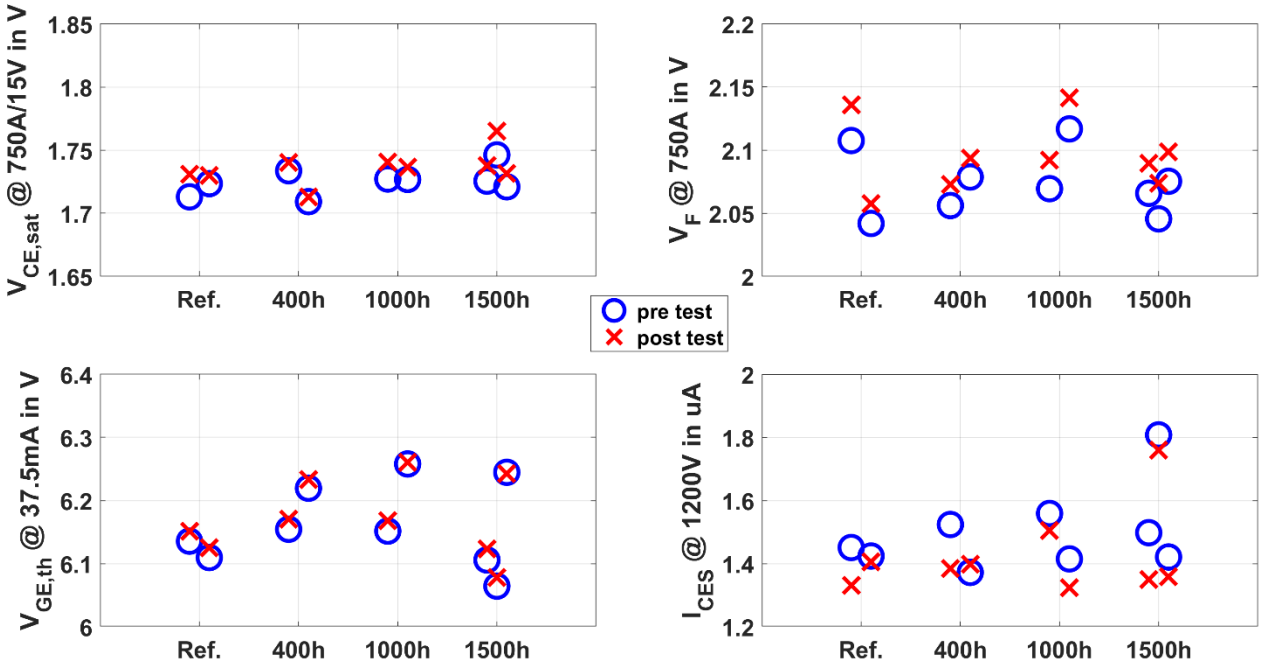

Figure 6: Static characterisation before/after the corrosive gas testing with H_2S (400 h, 1000 h, 1500 h) and the exposure to the same climatic conditions without gas supply (Ref.)

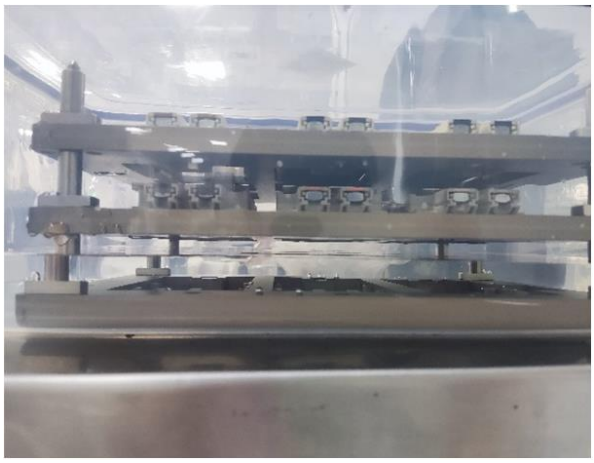

Figure 7: Setup for the soaking experiment with tested and new modules. An air sealed box is filled with water and stored in a climate chamber at 50 °C for 48 h.

selection of these values, taken at 25°C, are presented in fig. 6. The measurement values for the conduction losses of the IGBT as well as the diode are shifted to higher voltages across all samples. This is still within the normal scattering of these modules and with respect to the different corrosion states, a measurement artefact is most likely the reason for the deviation. No significant degradation was expected for these values as well as for the threshold voltage ($V_{GE,\,th}$). From testing under high humidity, the reduction of blocking capability is well known and reported [3, 6], therefore, an increase of I_{CES} at 1200 V could be a sign of decreasing insulation capability or corrosion at the chip interface. But, none of these can be stated at dry conditions by the data in fig. 6. The scattering in this measurement is attributed to the usage of a different measurement systems for the pre- and post-characterisation. Primarily, the semiconductors in this package are robust enough to survive 2000 h at HV-H³TRB conditions and therefore, no chip degradation was expected at 40 °C / 93 %. Referring to [5], even excessive dendritic growth in a much more pronounced appearance is not significantly influencing the blocking capability. The corrosion states in fig. 5 show a low number of dendrites too small to successfully short an insulation trench.

The material composition (especially the metal concentration) of the dendritic structures have a significant influence on the conductivity and the chance of a breakdown event is higher in the presence of humidity [8]. This leads to another approach in measuring the blocking voltage, again after a soaking experiment under high relative humidity.

The setup is shown in fig. 7, where the contaminated modules are stored in an air tide, water filled box. At 50 °C, the air gets saturated with water over time and the modules can be soaked in humidity for a time period of 48 h. For the next characterisation loop, just the module with the longest and most dendrites were used and compared to a new module to distinguish between temperature-/moisture and corrosion driven effects. In fig. 8, modules without corrosion (one new module and one part of split: "Humidity Ref.") are shown together with two modules from split: "H_2S-1500 h" and a HV-H³TRB sample. The significant difference in the moist and dry blocking curves is not just related to the higher temperature of 50 °C. Therefore, a temperature compensation [17] was used to shift the initial dry curve to 50° C:

$$C = 2^{\left(\frac{T_{init}-T}{11K}\right)} \tag{9}$$

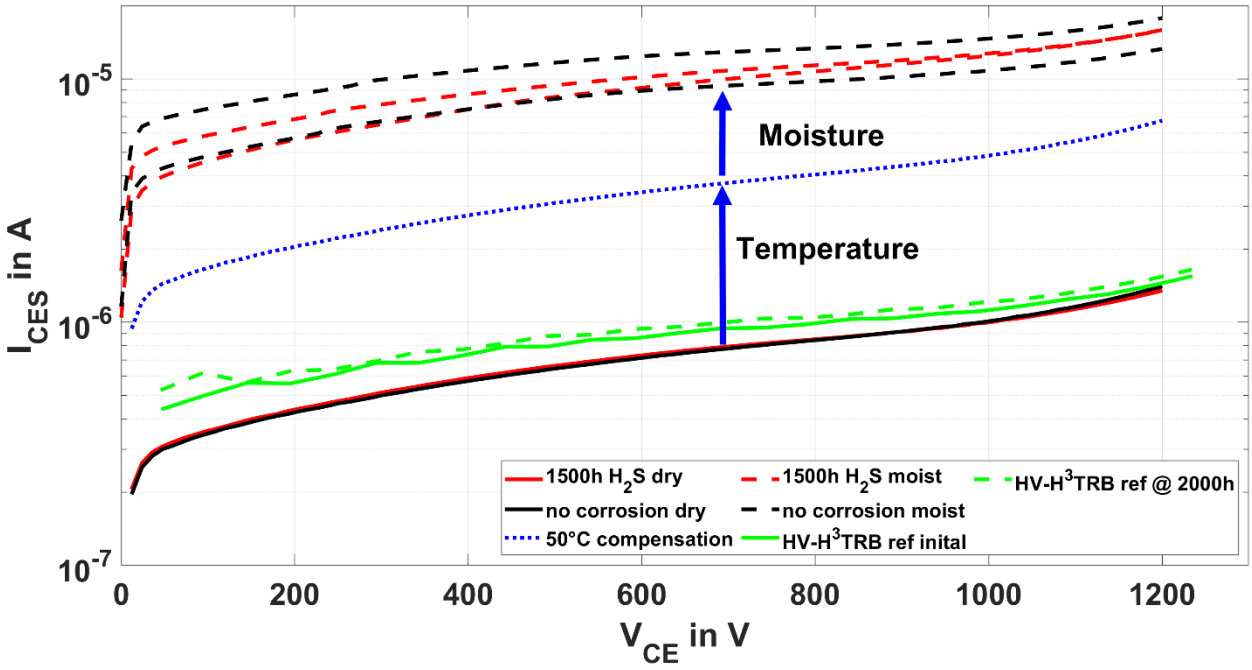

Figure 8: Blocking curves with dry and moist modules as well as HV-H³TRB reference. The measurement of the HV-H³TRB sample was performed in a different measurement range due to the expected degradation, which causes the off-set in the plot. The blue curve is the calculated 50 °C (eq. (9)) curve of a dry, new module.

Split	Quantity	Dry Test at 800V/1500A/125°C	Moist Test at 800V/1150A/50°C	Degradation
HV-H³TRB	8	8/8 passed	-	Not measurable
H_2S-400h	2	2/2 passed	-	Cathodic dendrites
H_2S-1000h	2	2/2 passed	1/1 passed	Anodic & cathodic dendrites
H_2S-1500h	3	3/3 passed	2/2 passed	Anodic & cathodic dendrites
Humidity Ref.	2	2/2 passed	1/1 passed	Not measurable

Table 3: Results of the switching test with high currents. The test is passed if the module is not destroyed in after the test procedure and the parameters were adjusted for the moist test to keep the voltage overshoot close to the nominal voltage.

The factor C is used as a multiplier for the leakage current and this can be utilised to shift the curve to higher temperatures. In fig. 8 this calculation separates the two different effects into a temperature and a moisture driven off-set. Nevertheless, all four measurements at a soaked state show a comparable behaviour and no clear tendency regarding the corrosion in the insulation trenches can be isolated. The only difference in the behaviour can be seen around 700 V for one of the corroded devices, were the curve shifts to a different slope.
In conclusion, the minor dendritic growth is not leading to any changes in the static behaviour. Even after the modules are stored under high humidity, no reduction in blocking capability can be attested.

Dynamic characterisation

To characterise the dynamic behaviour, a pass-/fail-test fulfilling a certain specification of the device is used. In this case, the device needs to be able to turn-off twice the nominal current at any time. As with the static characterisation, the measurement is split in a dry and a moist measurement. The results of these switching tests are shown in tab. 3 and all splits passed the procedure successfully.
The dry testing was executed at 125 °C (voltage overshoot limited to 1200 V) and an exemplary waveform of a humidity ref (40 °C/93 % RH/80 % V_{nom}) and a H_2S-preconditioned device is shown in fig. 9 (A). Both devices show the same waveform with comparable dv/dt and overshoot. No signs of degradation can be seen from these curves and the modules were fully functional afterwards. Even modules with an HV-H³TRB preconditioning of 2000 h passed this test, which attests a very robust module design. Furthermore, the test under moist conditions, led to the waveforms in fig. 9 (B.)) with significantly increased oscillation at V_{CE}. The current was adjusted to ~1.5 $I_{CES,nom}$ to control the voltage overshoot.
These oscillations are a result, caused by the lower temperature of 50 °C and changed switching behaviour of the bipolar semiconductor chips. Nevertheless, an influence of corrosion or the exposure to high concentrations of H_2S is not confirmed due to the fact, that unused modules show a comparable switching waveform under moist conditions.

Discussion

The preconditioned modules showed just optical signs of non-critical (few, short dendritic structures) corrosion (H_2S-exposure) and this finding was confirmed by the static measurement. There is no permanent degradation at the metals measurable and even the insulation materials like the housing-plastic and the Si-gel are still able to perform under critical electrical load. The overall excellent operation under static conditions correlates with the dynamic behaviour at high current switching. In conclusion, a degradation effect, which is not measurable

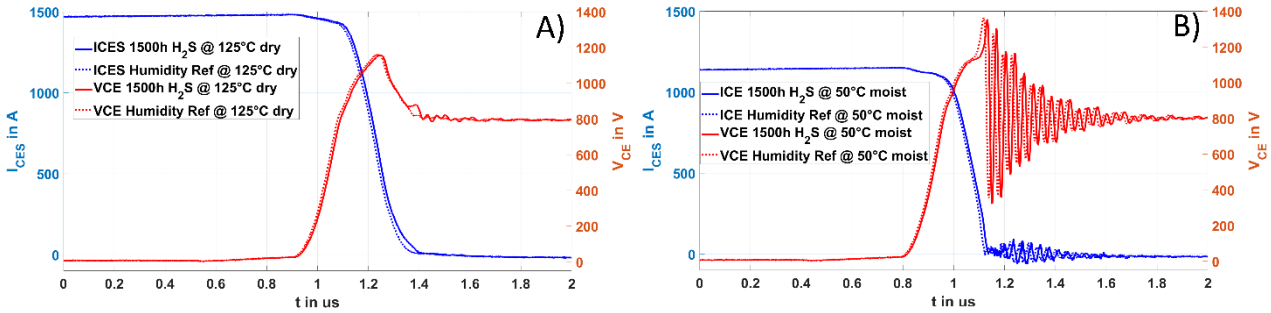

Figure 9: Switching curves of humidity and H_2S-preconditioned modules at 800 V:
A) dry conditionis at 125°C and 2 · $I_{CES,nom}$ (1500 A),
B) moist conditions at 50°C and ~1.5 · $I_{CES,nom}$ (1150 A), the switching current was reduced to limit the voltage overshoot

under static conditions has also a neglectable impact on the dynamic behaviour.
But, a change in the static behaviour can be achieved by a humidification preconditioning. If the IGBT-modules are moist, their blocking curves are shifted to higher leakage currents. The shift in the blocking curve is supposed to be not critical, since the nominal blocking voltage is still reached without any premature avalanche.

CONCLUSION AND OUTLOOK

In this study, standard IGBT-modules were preconditioned in harsh climate to evaluate the influence of corrosion products on the static and dynamic behaviour. The overall robust design of the modules prevented critical degradation after 2000 h of HV-H³TRB testing and the wide insulation distances on the substrates slowed the dendritic growth due to the H_2S exposure. Therefore, it was impossible to inflict enough degradation (in an acceptable time frame) to the devices to show a significant influence of the corrosion on the electrical performance. The tested module type performs excellent in these climatic tests and some of the design decisions can be regarded as improvements to inhibit certain corrosion effects. Especially the H_2S-induced dendritic growth at the substrates was prevented by the substrate design, which lowered the electrical field and decelerated the process. Summarised, the corrosion products were uncritical in the optical inspection and the same result was obtained from the electrical characterisation afterwards. Even modules with long testing times could withstand a high current turn-off event without failing and a significant influence of a high moisture content in the Si-gel could not be proven.
This experiment could be executed for any Si-gel potted device type and if the corrosion products or the climate related degradation is measurable, the turn-off event might cause a different result. For applications in corrosive environments, the insulation distances inside the module should be considered if ionic contamination is expected in the surrounding air.

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Surge current test of SiC MOSFET with planar Assembling and Joining Technology

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Abstract

This paper introduces a novel packaging with planar Assembling and Joining Technology (AJT). The 1200V SiC MOSFET body diode with the new AJT has been investigated under surge current conditions. The test result of the planar AJT is compared with a standard TO-247-4 discrete component. Additionally, thermal impedance of both packages is measured and compared.

Keywords: surge current test, novel packaging, SiC MOSFET.

Motivation

An active front end rectifier replaces diodes with IGBTs (or SiC MOSFETs) to convert the incoming AC grid voltage into controlled DC voltage. It has low current harmonics, enables power factor correction and bidirectional power flow.

In an industrial active front end application, inrush current may lead to a high surge current through the freewheeling diodes (or body diodes) that is far beyond the nominal rated current. The resulting peak junction temperature can exceed the maximum specified temperature by far, which causes a certain degradation of the diode at each surge event.

SiC MOSFET body diodes suffer from the surge current event much more than the Si diodes. Because the body diode has a higher forward voltage drop and a smaller chip area, which results in a higher power density. The comparison between a SiC body diode and a Si diode can be found in [1].

The surge current capability of the body diode should be specified according to application and improved.

This paper investigates the surge current capability of a novel packaging with planar Assembling and Joining Technology (AJT). The test results are compared with the standard discrete package TO-247-4.

Approach

The investigated 1200V SiC MOSFET has a chip area of 0.25cm^2, and a specific R_{DSon} of 4.25 mΩcm^2 at 25°C. The same chip type is assembled into three different packages for comparison. The I-V characteristic is measured at different V_{GS}, shown in Fig. *1*.

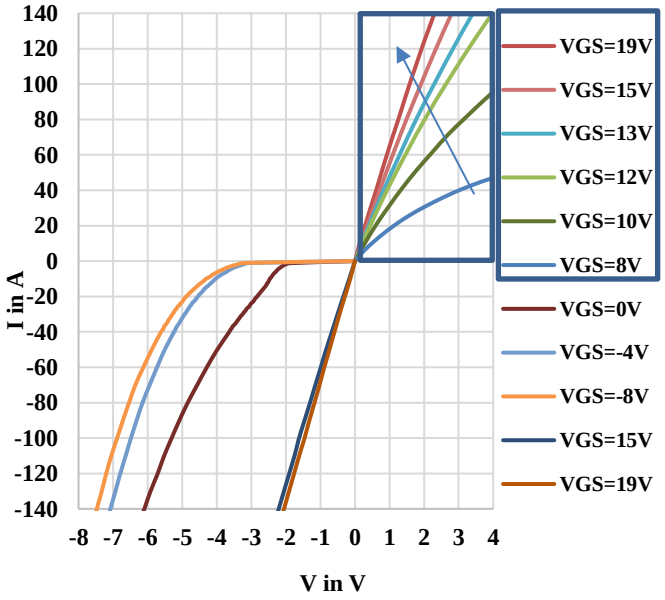

Fig. 1: I-V characteristic of 1.2kV SiC MOSFET at T_a=30°C.

The cross-section view of the three SiC MOSFET packaging types are shown in Fig. 2.

- Type 1 planar AJT with DBC:
  The SiC MOSFET is sintered on direct bonded copper (DBC), and the full source and gate area are soldered to a redistribution layer. The isolation material has a low thermal conductivity, less than 0.5W/(m·K).

- Type 2 planar AJT with Cu:
  Four chips are sintered on a thick Cu lead frame (2mm), and the full source and gate area are soldered to a redistribution layer.

- Type 3: TO247-4: (reference sample)
  One chip is soldered on 2 mm Cu lead frame, and bond wires connects the chip top side.

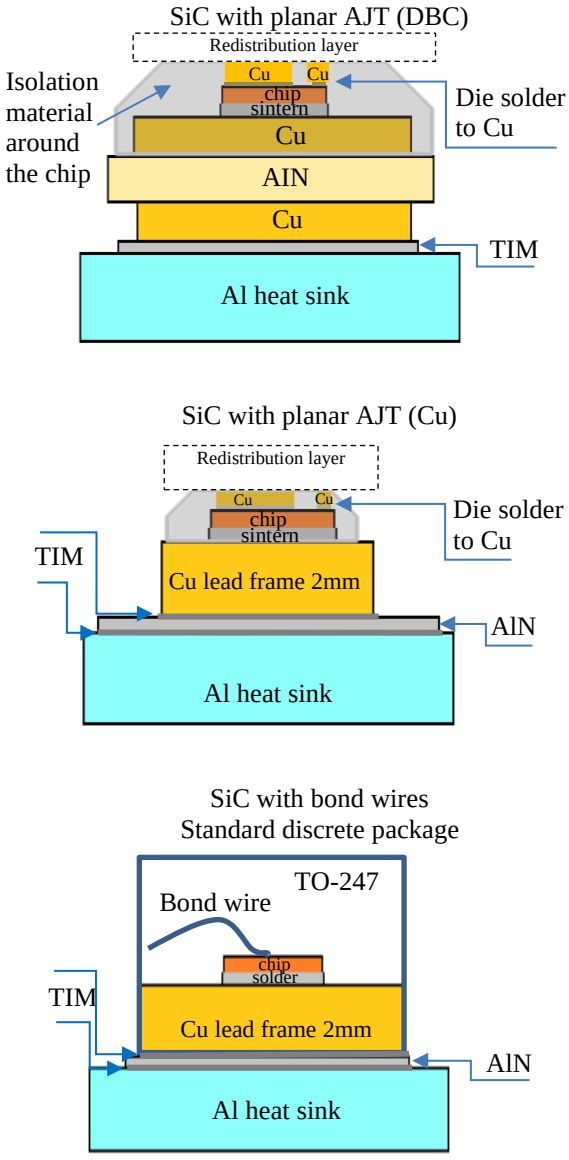

Fig. 2: Three types of SiC MOSFET packaging: planar AJT and standard discrete package TO-247.

There are 2 up to 4 samples of each package type in the surge current test. The half-sine waves load on the body diodes is applied for 10ms at room temperature, which is corresponding to 50Hz grid frequency. The surge current capability of SiC MOSFET at different load time can be found in [2].

The current stress pulse is repeated 20 times at the same current level, with 30 s cooling down time in between. Each sample is screwed on a heat sink with thin thermal interface material (thermal grease) in between to ensure better cooling under surge current conditions.

Three types of packages are compared with shortened gate and source during the surge current event. The standard package TO-247 is also tested with a negative gate-source voltage (V_{GS}=-8V), which is compared to the result under a V_{GS}=0V condition.

$$\int_0^{tp} I^2(t) \cdot dt = \frac{1}{2} \times IFSM^2 \cdot tp \qquad \text{Eq. 1}$$

The current waveform is like a half-sine pulse, the current integral I^2t is calculated with the current amplitude I_{FSM} in Eq. 1, which is a measure for the thermal load.

Each series of surge current test pulses starts from rated current with 20A increase per step. Three failure criteria parameters are monitored after each surge current event:

- the leakage current (I_{DSS}) of the SiC MOSFET at 1200V blocking voltage.
- the gate leakage current (I_{GSS}) at V_{GS}=15V.
- the forward voltage-drop (V_F) during the load of surge current.

The maximum current before chip degradation (last pass) is the surge peak forward current (I_{FSM}).

Surge Current Test Results

Two pairs of measured waveforms from planar AJT (DBC) are shown in Fig. 3 as an example. The peak current of the half sine current wave is increasing, and the corresponding voltage also increases in a similar wave form.

The planar AJT with DBC packaging (single chip) lost the blocking capability at around 400 A, which is about three times the rated current. The rated current is given in data sheet at 25°C.

Neither distortion is observed in the forward voltage wave form, nor is there an increase of gate leakage current.

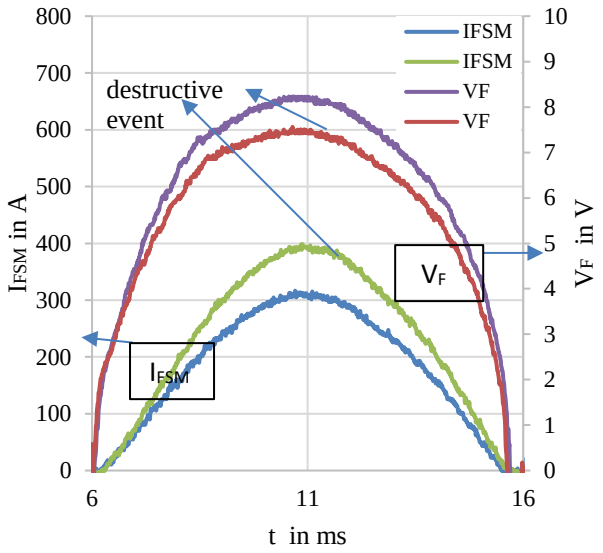

Fig. 3 Measured half sine wave form at room temperature at sample one with planar AJT (DBC).

The last I_{FSM} value before the first signs of the degradation of the packaging under test is shown in **Error! Not a valid bookmark self-reference.**. The lowest I_{FSM} value of each group is used for comparison and further I^2t calculation.

Table 1: I_{FSM} measurement results at T_a=25°C, V_{GS}=0V.

Packaging type	Chips per package	I_{FSM} before defect in A	I^2t in kA^2s (From lowest I_{FSM})
Planar AJT (DBC)	one chip	400 372 410 380	0.69
	four chips	1733 1534 1704 1532	11.74
Planar AJT (Cu)	four chips	1945 1730	14.96
TO-247-4	one chip	340 340 340 340	0.58

All planar AJT samples show the same failure mode: increase of leakage current I_{DSS} at 1200V blocking voltage, which increases from a nA range to a mA range. No distortion on forward voltage or I_{GSS} increase is observed after surge current events.

The I_{FSM} value of the planar AJT (DBC) packaging with four parallel chips (1532A) is around four times the I_{FSM} value of a single chip (372A). A symmetric layout design leads to a symmetric current distribution among parallel chips.

The I_{FSM} of the planar AJT with Cu (1730A) is approx. 13% higher than the planar AJT with DBC (1532A), because the heat distributes/spreads better in the thick Cu lead frame than through the thin Cu layer of the DBC. The integral I^2t of planar AJT with Cu is 28% higher than the planar AJT with DBC.

The I_{FSM} value of planar AJT (Cu) is divided by four (1730A/4 ~430A), since four parallel chips are in test. It is approx. 25% higher than the I_{FSM} value of the TO-247-4 (340A), which proves the advantage of a planar AJT– especially for SiC, which heats up strongly in the first some microns of the chip. The integral I^2t of the planar AJT with Cu is almost 60% higher than the integral I^2t of a TO-247-4.

The chip temperature increases dramatically in the surge current event, which causes melting or modification of the chip metallization layer at the destruction limit. The conductive layer in a planar AJT directly attaches the full source and gate area, which enables a homogeneous current distribution among the chip and prevents a high current density, e. g. under the bond feet like in a standard AJT, see Fig. 4.

Fig. 4 Top view of decapsulated DUTs after surge current tests [3].

The heat dissipation of a planar AJT is improved because a part of the heat is transferred from the chip front side into the redistribution layer.

Measurement of thermal impedance

The thermal impedance of both packaging technologies i. e. TO-247 and the planar AJT (Cu) is measured and compared. The package was heated up at 50% nominal current for 1s and cooled down for 1s. The chart of the first 10ms is shown in Fig. 5.

The planar AJT with Cu has a lower thermal impedance than the TO-247. The drift starts immediately at around 0.1 ms and further enlarges through the time. At 10 ms, the Z_{th} value difference is around 40%.

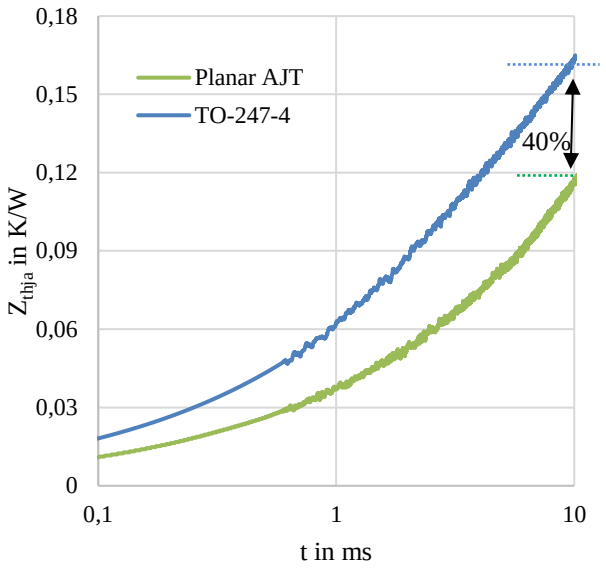

Fig. 5 Thermal impedance measurement result.

The two main reasons for the difference are:

- the heat in TO-247-4 transfers from chip to heatsink, but in the planar AJT the Cu layer on the redistribution layer attached to the chip dissipates also heat.

- The chip in the TO-247-4 is soldered on Cu lead frame, while the planar AJT has a sintered chip connection.

Further simulation will reveal the influence of each factor, which will be investigated soon.

The Z_{th} value at 10ms has 40% difference between the two packages, which is lower than the difference in surge current capability (60%).

Whereas the maximum chip temperature is the determining factor in the surge current test, the thermal impedance measurement uses the average junction temperature, which is more than 100K lower than the maximum chip temperature in a surge current event, see [4].

Influence of different VGSoff

The voltage drop of the body diode is measured until the nominal current under different V_{GS}, which is already demonstrated in Fig. 1 (third quadrant of the I-V characteristic). The voltage-drop of the body diode at V_{GS}=0V is much smaller than V_f at V_{GS}=-4V. The main reason is that at V_{GS}=0V, the gate channel still contributes to the source current and only some part of the current flows through the body diode. Up to the rated current range, the current flow differs at different negative gate-source voltage (V_{GSoff}). Depending on the input current range, the V_f difference varies from 25% to 80%.

But if the current flow reaches a higher range, e. g. up to three or four times of the rated current, the curves converged.

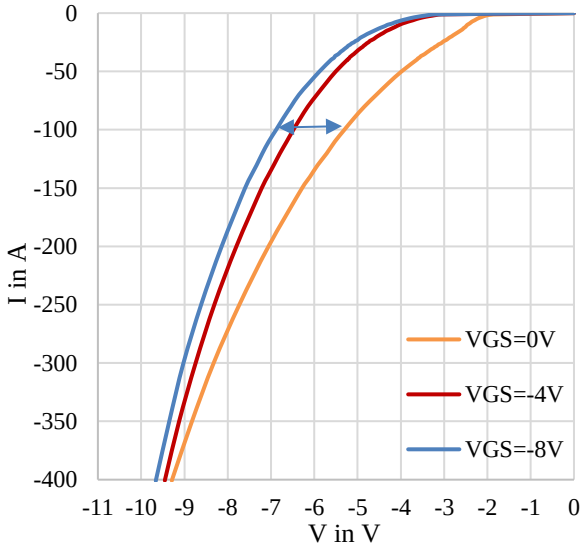

Fig. 6 I-V characteristic in third quadrant, measured up to 4 times of rated current at 30°C.

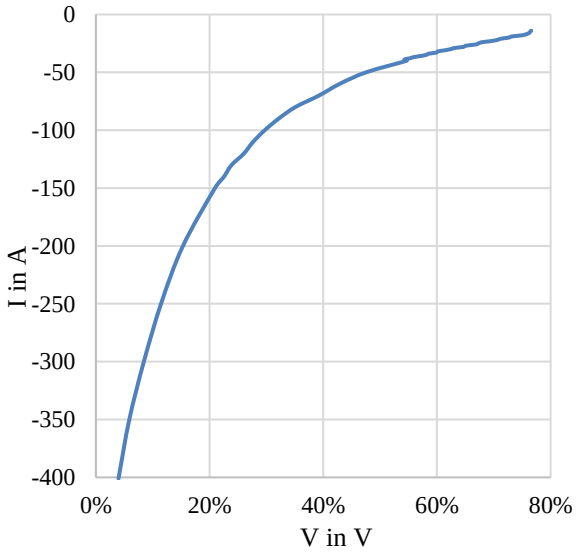

Fig. 7 the difference in voltage-drop V_{SD} in between V_{GS}=0V and V_{GS}=-8V. $\Delta V_{SD} = (V_{@Vgs=-8V} - V_{@Vgs=0V}) / V_{@Vgs=0V}$

As shown in Fig. 6, the I-V curve at different V_{GSoff} is measured up to four times of the rated current and the influence of different V_{GSoff} is getting smaller together with the increase of current. At almost four times the rating current, the difference in the voltage drop is only 5%, see Fig. 7. Most of the current flows through the body diode under a surge current condition, so the surge current capability is similar at a different gate turn-off voltage, as it was shown in [5].

Table 2 I_{FSM} measurement results at different V_{GS}, T_a=25°C.

Packaging type	V_{GS} in V	I_{FSM} before defect in A	Lowest I_{FSM} in A
TO-247-4	0V	340 340 340 340 380	340
TO-247-4	-4V	340 340 360 340 340	340

The surge current capability of the TO-247-4 package is tested with a negative gate-source voltage of V_{GS}=-4V for comparison. 5 samples were tested with the same set-up and test condition. The I_{FSM} before a destructive event is 340A, which is the same as the measurement result of TO-247 performed with V_{GS}=0V, see Table 2.

Summary

The surge current capability of a planar AJT is compared to the standard discrete packaging of a TO-247-4. The integral I^2t of this planar AJT with Cu is 60% higher than that of a standard TO247-4 discrete package. The difference in the thermal impedance explains the remarkable improvement with a planar AJT. Especially for SiC – which has a 10-times thinner drift zone. A lot of losses are generated in the first some microns of the chip. Therefore, a good front-side cooling/thermal capacitance is helpful for short-time events like surge currents.

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Channel Potential Modification induced Displacement Current during the Trench-Gate IGBT Switching

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Abstract

During the switching process of the IGBT, the Miller plateau can be observed on the gate voltage waveform. The present understanding of the Miller plateau is the Miller capacitor induced displacement current at the collector-emitter voltage transient, which is compensated by the gate current from the driver unit. Hence, the gate voltage remains constant.
*In this paper, a novel finding of the **C**hannel **P**otential Modification **i**nduced Displacement **C**urrent (CPiC) is proposed. It has been found that during the Miller plateau, the displacement current is not only provided by the Miller capacitor, but also by inner parts of the gate-emitter capacitor due to the channel potential modification. This novel finding extends the existing descriptions for the IGBT switching behavior and provides a more comprehensive understanding of the Miller plateau.*

Keywords: IGBT, Hard Switching, Miller Effect

Introduction

During the hard switching process of IGBTs, the chip internal parasitic capacitances must be charged and discharged, determining the maximum switching speed of the device. During the collector-emitter voltage transient, the voltage across the Miller capacitor C_{GC} also varies, generating the displacement current. The gate current from the gate drive unit will compensate for this displacement current. Hence, the charging of the gate-emitter capacitor C_{GE} is delayed, and the gate voltage V_{GE} remains at a constant value during this interval, which is known as the Miller plateau [1][2].
Figure 1 (a) shows the turn-on process of a 1.2 kV, 40 A discrete IGBT (IKY40N120CH3) as an instance. A slow switching speed was used to measure the gate current and calculate the gate charge accurately. As shown in the figure, the Miller plateau on the gate voltage waveform can be divided into two parts: a fast negative dV_{CE}/dt part (green shaded area) and the low V_{CE} regime with a much slower dV_{CE}/dt (blue shaded area). The gate current during the plateau is also constant and given by the on-state gate voltage $V_{GE,on}$ of the driver and the gate turn-on loop resistor $R_{G,on}$:

$$I_{G,miller} = \frac{V_{GE,on} - V_{GE,Miller}}{R_{G,on}} \qquad (1)$$

During the fast dV_{CE}/dt from $V_{CE} \approx 575$ V to about 20 V, the gate charge Q_G calculated by the gate current (35.6 nC) should be equal to the Miller capacitor charge Q_{GC} (33 nC). It basically matches the corresponding integration of the static C_{GC} - V_{CE} measurement in Figure 1 (b).

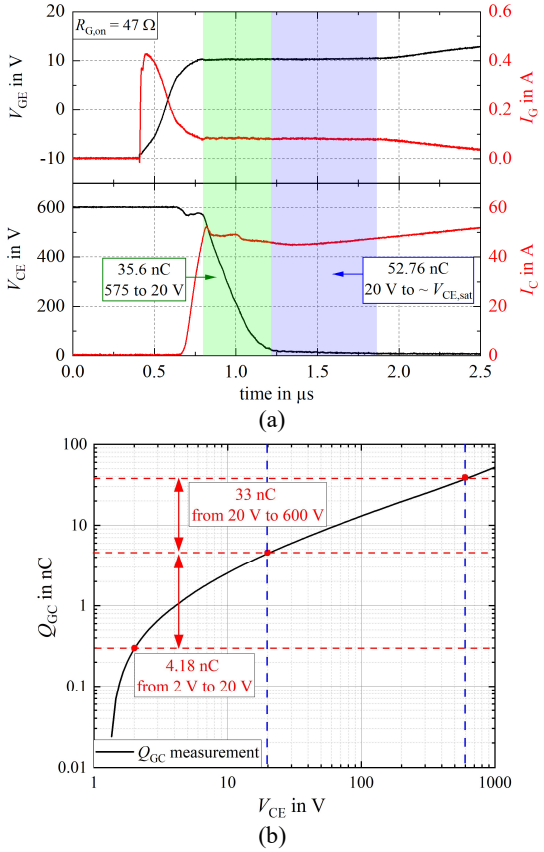


Figure 1: (a) turn-on behavior of IKY40N120CH3, the Miller plateau is divided into two parts; V_{CE} = 600 V, $R_{G,on}$ = 47 Ω, I_C = 40 A. (b) Integration of the static C_{GC} - V_{CE} measurement

However, in the slow dV_{CE}/dt phase, the calculated charge from the dynamic measurement is much higher than the value in the static test. V_{CE} drops slowly from about 20 V to near the saturation voltage $V_{CE,sat}$. The calculated charge value in this interval is 52.76 nC, and much higher than the 4.18 nC of the static C_{GC} - V_{CE} test. There may be an inevitable measurement error due to the gate current measurement, the integration interval selection, and the delay between the measurement probes. However, the overall trend is clear. A similar phenomenon can also be found in the small dV_{CE}/dt phase for the turn-off behavior. Therefore, the focus of this paper is to explain the origin of excess charge in the Miller plateau phase, especially in the low V_{CE} regime.

Dynamic Miller Effect at Low Collector-Emitter Voltage Regime

The composition of the Miller capacitor C_{GC} (orange colour) and the gate emitter capacitor C_{GE} (blue colour) without applied voltage for a trench-gate IGBT is shown in Figure 2 (a). The larger part of the Miller capacitor is the oxide capacitor of the trench side walls and the trench bottom. The field oxide is much thicker compared to the gate oxide layer; therefore, the contribution to the total C_{GC} is smaller. During the Miller plateau of the IGBT turn-on, the gate voltage is almost constant and determined by the threshold voltage $V_{G,th}$, load current I_C and the transconductance g_{fs} of the device:

$$V_{GE,Miller} = V_{G,th} + \frac{I_C}{g_{fs}} \tag{2}$$

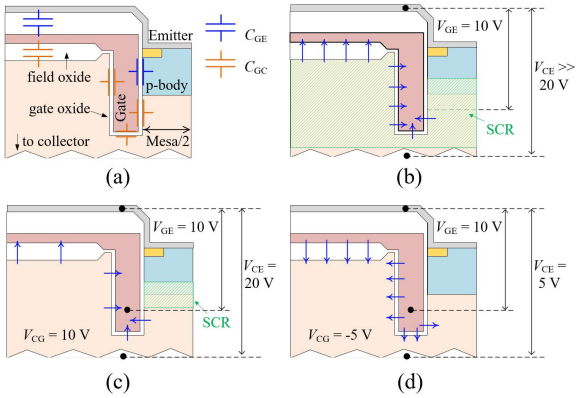


Figure 2: Simplified dynamic estimation of the Miller capacitance at different V_{CE}; (a) composition of C_{GC} and C_{GE} for a trench gate IGBT without voltage; (b) beginning of the Miller plateau $V_{CE} \approx V_{DC}$; (c) at low V_{CE} regime, $V_{CE} > V_{GE} = 20$ V; (d) $V_{CE} < V_{GE} = 5$ V

Assuming that the amplitude of the Miller plateau is 10 V, at the beginning of the plateau, the V_{CE} is still high and close to the DC-link voltage V_{DC}. At high V_{CE}, the collector potential is much higher than the gate. Inside the oxide layer, the electric field points from the collector to the gate, as indicated by the blue arrows in Figure 2 (b). The space charge region (SCR) inside the low-doped drift layer (w_{SCR}) is at this time point fully established and takes over the voltage. Therefore, the junction capacitor C_J is in series with the oxide capacitor C_{Ox} and results in a smaller Miller capacitor:

$$C_{GC} = \frac{C_{Ox} \cdot C_J}{C_{Ox} + C_J} = \frac{C_{Ox} \cdot \frac{\varepsilon \cdot A}{w_{SCR}}}{C_{Ox} + \frac{\varepsilon \cdot A}{w_{SCR}}} \tag{3}$$

After V_{CE} decreases to a lower value, e.g., 20 V, the junction capacitor becomes much higher and increases C_{GC} according to Equation (3). Hence, the dV_{CE}/dt is limited. An electric field is still inside the oxide layer, but the strength is much weaker, see Figure 2 (c). With further decreased V_{CE}, e.g., $V_{CE} = V_{GE}$, the space charge region vanishes, and the Miller capacitor becomes the pure oxide capacitor and reaches the maximum value. In the final stage of the Miller plateau, when $V_{CE} < V_{GE}$ (Figure 2 (d)), any small reduction in V_{CE} must discharge the whole oxide layer of the Miller capacitor. Therefore, a large displacement current is still required, even if the changing rate of V_{CE} is much less.

Therefore, when V_{CE} is low, e.g. close to the saturation voltage, the result obtained through the static C_{GC} - V_{CE} test cannot accurately estimate the required gate charge during the dynamic processes. Because for static C_{GC} - V_{CE} measurement, the gate and the emitter of the tested device are shorted, and $V_{CE} = V_{CG}$. As V_{CE} rises, the SCR is established instantly at the emitter pn-junction. Therefore, the value of the Miller capacitance will start to decrease. However, when the IGBT operates in the switching mode, the voltage difference between the gate and the collector has to be considered.

According to the definition, the change of electric field strength in the capacitive medium can be used to describe the displacement current:

$$I_{dis} = \varepsilon_0 \cdot \frac{dE_{Ox}}{dt} + \frac{dP_{Ox}}{dt} \approx \varepsilon_0 \cdot \frac{dE_{Ox}}{dt}. \tag{4}$$

Where P is the polarization in the medium (SiO_2), and remains constant. Therefore, to more intuitively describe the Miller effect generated displacement current at the low V_{CE} regime, a two-dimensional half-cell trench-gate IGBT model was developed in Synposis TCAD and calibrated according to the measured device. The front side design is shown in Figure 3, the thickness of the gate oxide layer is 100 nm.

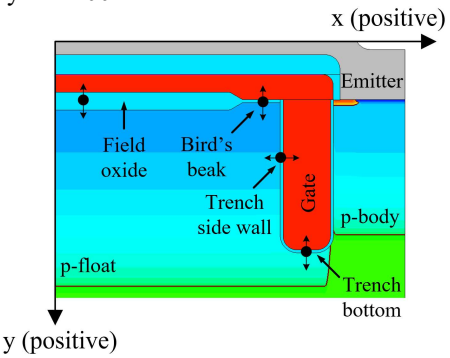


Figure 3: Front side design of the IGBT model and the extraction points for the electric field strength in the oxide layer of C_{GC}; the positive direction for x- and y-direction is given

After that, TCAD simulations were carried out to extract the internal electric field of the oxide layer with up-swept V_{CE} from 0 to 1000 V. Because the junction capacitance is in series with the oxide capacitance, the displacement current (from ΔE_{Ox}) in the oxide can be used to represent the current flow through the Miller capacitance. The V_{CE} is swept upwards with 1 V/s, which is similar to the static test. The perpendicular electric field strength of the oxide layer was extracted. The selection of extraction points is shown in Figure 3. The gate voltage was set to 0 V or positive 10 V. When V_{GE} = 0 V, it simulates the static small signal C_{GC} - V_{CE} test situation. V_{GE} = 10 V is analogous to the IGBT turn-on, where the gate voltage is in the Miller plateau level and holds in a steady state.

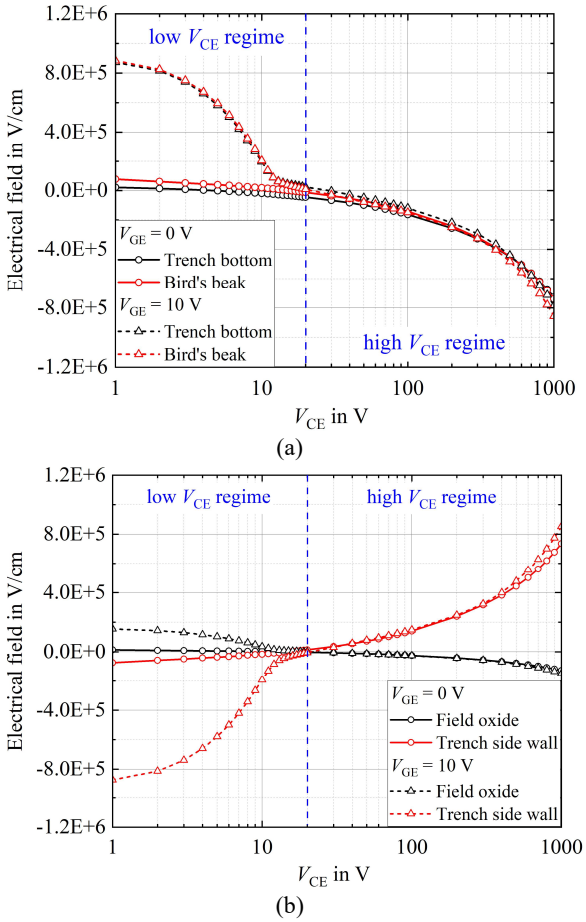


Figure 4: Electric field at the different oxide layer parts for Miller capacitor with different V_{GE} and V_{CE}

Figure 4 (a) shows the electric field at the trench bottom and the bird's beak in the y-direction with respect to V_{CE}. It can be seen that when V_{GE} is 10 V and V_{CE} is small, there is a large potential difference between the gate and the collector. Therefore, the electric field strength in the oxide layer is high. When V_{CE} = 1 V, the electric field strength in the oxide layer is about $8.8 \cdot 10^5$ V/cm in both the trench bottom and the bird's beak area. Here a positive electric field in the y-direction represents that potential of the gate is higher than the collector.

When the gate voltage is 0, the electric field strength is close to 0. It is not exact zero due to the difference in surface potential between the highly doped poly-gate and the p-float region [2][3].

In the low voltage region (V_{CE} up to 20 V), the electric field modification (ΔE_{Ox}) due to the potential difference between the gate and the collector is much higher than at V_{GE} = 0 V. If the absolute value of ΔE_{Ox} is considered, from 1 to 20 V it is almost the same change in V_{CE} as from 20 to 1000 V (high V_{CE} regime). Hence, the charge generated from the displacement current is also close, see Equation (4). Therefore, the dynamic Miller effect at low voltage is much stronger than estimated by the static small signal C_{GC} - V_{CE} test.

When V_{CE} is higher than about 20 V, the collector voltage will dominate the electric field strength of the oxide layer. Therefore, the gate voltage has almost no influence anymore. In Figure 4 (b), the situation on the trench side wall is similar. For the field oxide layer, due to the higher thickness, the electric field strength is lower than that of the gate oxide layer. However, the influence of this part should not be neglected because of the large area.

The depletion region formation/expansion process inside the device at different gate voltages is shown in Figure 5. If the gate and the emitter are shorted (V_{GE} = 0 V), there is no influence/impact from the gate voltage, the space charge region between the p-float and the drift region has already been created at V_{CE} = 2 V. Consequently, the junction capacitance is formed and in series with the oxide capacitance, reducing the Miller capacitance. When V_{CE} reaches 20 V, the depletion region reaches about 20 µm in the drift region.

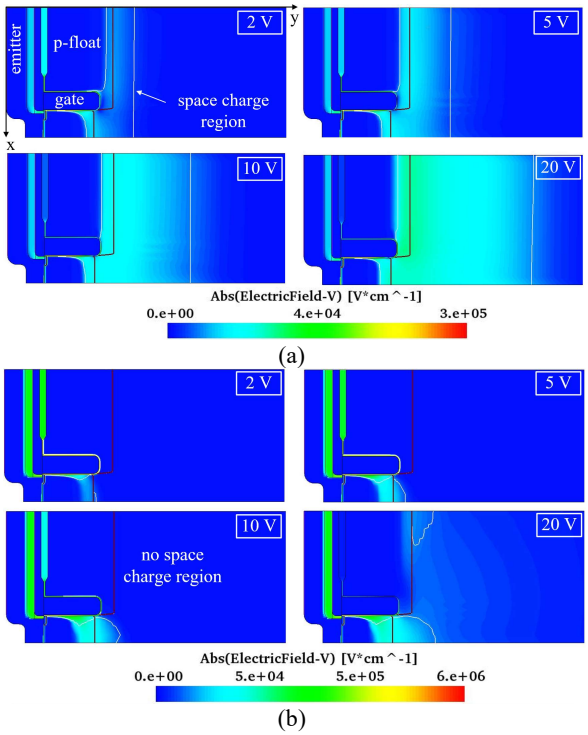


Figure 5: The formation and expansion of depletion region inside the device at different gate voltages, V_{CE} from 2 V to 20 V. (a) V_{GE} = 0 V, (b) V_{GE} = 10 V

When V_{GE} = 10 V, due to the potential difference between the gate and collector and the load current, the space charge region cannot be established at the pn-junction

immediately. The electric field strength inside the oxide layer is higher compared with V_{GE} = 0 V. With increased V_{CE}, the collector potential is opposite to the gate, thus reducing the electric field strength in the oxide layer. No space charge region can be formed since the gate potential is still higher. Until V_{CE} reaches 20 V, the formation of a space charge region can be observed at the pn-junction. Before that, the Miller capacitor is mainly the oxide layer capacitor.

Channel Potential Modification induced Displacement Current (CPiC) in the Gate-Emitter Capacitor

In addition to the displacement current generated by the Miller capacitance, during the low V_{CE} regime, the drop of V_{CE} will cause a voltage change close to the channel region. The on-state voltage of the IGBT can be expressed by:

$$V_{CE,on} = V_{pn} + V_{drift} + V_{mesa} + V_{CH} \qquad (5)$$

Where V_{pn} is the built-in voltage of the pn-junction at the collector side, V_{drift} the voltage drop in the drift region, V_{mesa} the voltage drop in the mesa region in between the trenches (where no channel is present) and the channel voltage drop V_{CH}, see Figure 6. For the turn-on process, the voltage in each part decreases and vice versa for the turn-off. At this time, since V_{GE} is stabilized at the Miller plateau level, it can be seen from Equation (4) that when the channel potential V_{CH} changes, displacement current will be generated in the gate-emitter capacitor. When the V_{GE} is greater than the threshold voltage $V_{G,th}$ and the inversion channel has been formed, C_{GE} is mainly the oxide layer capacitance due to the existence of the high conductive inversion layer, and it is large. Therefore, the displacement current generated by C_{GE} is high, too [3].

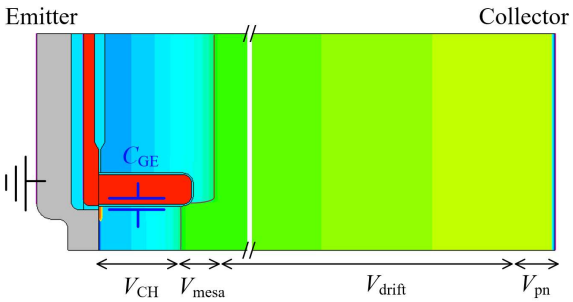


Figure 6: On-state voltage distribution of the trench-gate IGBT

Figure 7 shows the simulated switching process and the variation of the channel potential V_{CH}. The simulated results match well with the measurements, and two stages of dV_{CE}/dt during the Miller plateau can be clearly seen. The channel potential is extracted from the emitter metallization to the end of the channel, as shown in Figure 6. It changes significantly in the low V_{CE} regime, where dV_{CE}/dt is also small. For the turn-on process, the Miller plateau voltage stabilizes at approximately 10 V.

In the low dV_{CE}/dt region (blue shaded area) the channel potential drops from 8.85 V to 2.65 V. If we wait for V_{GE} to reach the 15 V, V_{CH} is much smaller with 1.08 V. For the turn-off process, this voltage rises from 1.705 V to 8.87 V.

Four time points from t_1 to t_4 at the low V_{CE} regime are selected in Figure 7 to observe the displacement current inside the device. The primary focus is on the current in the gate-emitter capacitor due to the V_{CH} modification. Hence, only the displacement current density perpendicular to the oxide layer of C_{GE} (in the x-direction) is illustrated in Figure 8. At the bottom of the trench, the displacement current is mainly in the y-direction, hence, almost zero in the x-direction.

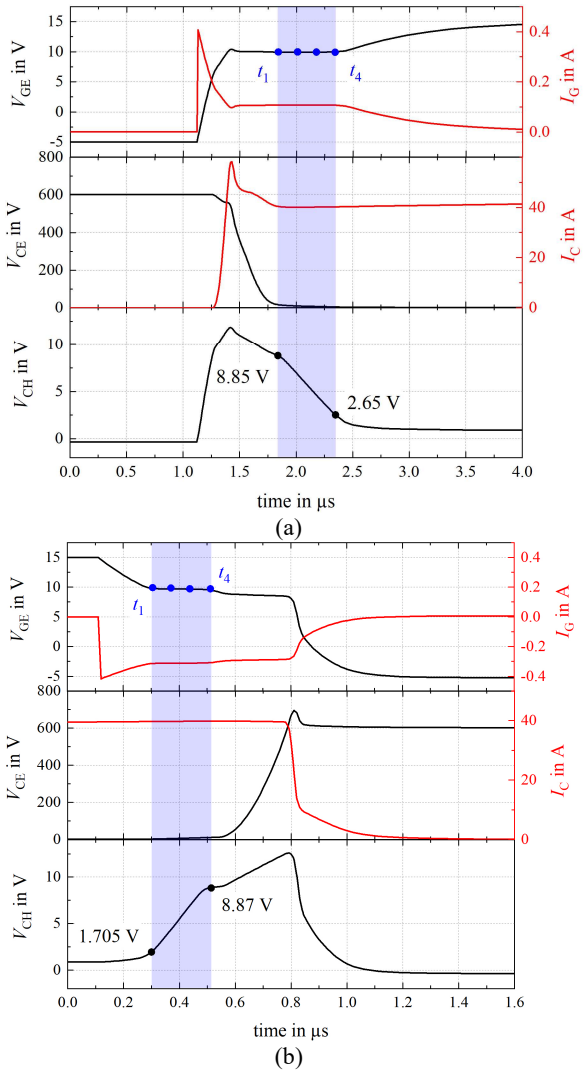


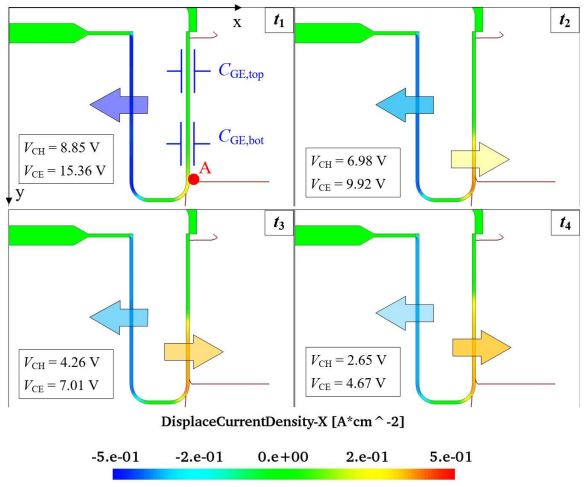
Figure 7: Simulated switching behavior with extracted V_{CH}; V_{DC} = 600 V, $R_{G,on}$ = $R_{G,off}$ = 47 Ω, I_C = 40 A, T = 300 K. (a) turn-on, (b) turn-off

The oxide layer´s displacement current density for turn-on and turn-off in the x-direction for each time point is shown in Figure 8. The corresponding channel voltage and V_{CE} are given. The direction of the arrows indicates the direction of the displacement current flowing through the oxide layer. The intensity of the colour represents the magnitude of the current density. Point A is noted as the

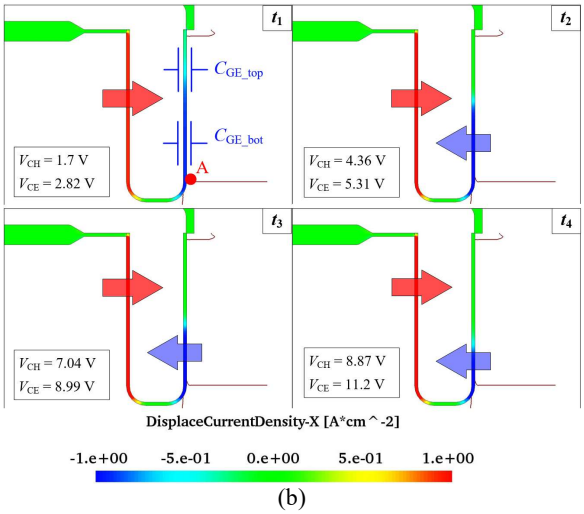
end of the channel. C_{GE} is divided into top and bottom parts for convenience of description.

At the beginning of the turn-on process t_1, a small positive displacement current is generated in the mesa region and is close to the end of the channel due to the slightly decreased V_{mesa} and V_{CH}. The direction is from the gate to the channel (emitter). Afterwards from t_2 to t_4, V_{CH} keeps decreasing, and the CPiC generated near to $C_{GE,bot}$ becomes more significant. Since the current direction is out of the gate, it is compensated by the charging gate current from the gate driver.

In addition, a negative displacement current can be seen for the left trench side wall, which is from the gate to the collector. This current belongs to the displacement current generated by the Miller capacitor causing the Miller plateau from the conventional understanding. In the upper part of the gate capacitor, CPiC is not apparent since the V_{CH} change is small in the upper part of C_{GE}.



(a)



(b)

Figure 8: Displacement current density j_{Dis} in x-direction in the oxide at different time points in Figure 7 during the switching; (a) turn-on, (b) turn-off

For the turn-off process, V_{CH} increases during the low V_{CE} regime. Therefore, the direction of CPiC generated in the gate capacitance is opposite and flows into the gate from the channel. Similarly, this current, along with the current generated by the Miller capacitance, is compensated by the discharge current from the gate driver.

The above analysis shows that the Miller plateau is not only a consequence of the Miller capacitor. The gate capacitor will also affect this process and should therefore also affect the device's switching speed. During the Miller plateau phase, the gate current can be considered as the displacement current from the whole oxide layers of C_{GC} and C_{GE}.

$$I_{G,Miller} \approx I_{Ox} = I_{GC,total} + I_{GE,total} \tag{6}$$

Therefore, by extracting the current of the entire oxide layer, the ratio between CPiC and the displacement current from the Miller capacitor can be quantitatively analysed.

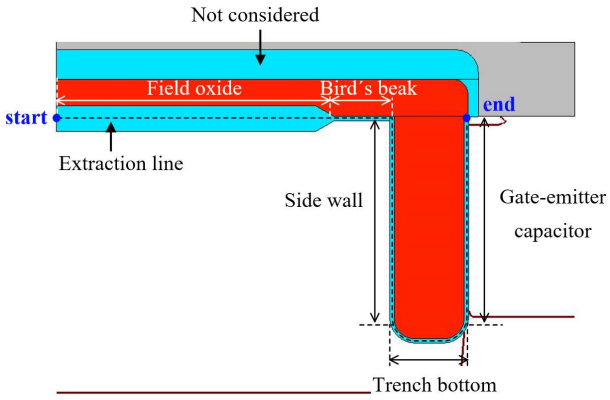


Figure 9: The extraction line (black dashed) of the displacement current through the oxide layer of C_{GC} and C_{GE}

The extraction line is shown in Figure 9. The starting point is the left edge of the field oxide layer, and then along the field oxide layer to the right, through the bird's beak area, the left trench side wall, the bottom of the trench, and finally reaches the emitter n^+-region through the right trench side wall. The part from the trench bottom to the n^+-region can be approximately considered as the C_{GE} region, generating CPiC:

$$I_{GE,total} = I_{CPiC} = I_{GE,bot} + I_{GE,top}. \tag{7}$$

The sum of the displacement currents in the oxide layer in other regions is the displacement current generated by the Miller capacitance:

$$I_{GC,total} = I_{GC,field\_Ox} + I_{GC,birdsbeak} + I_{GC,side\_wall} + I_{GC,trench\_bot}. \tag{8}$$

The displacement current in the top part gate oxide layer is not considered because the potential modification in the gate is negligible during the Miller plateau.

The IGBT model in TCAD is a two-dimensional model, but the default depth in the z-direction is 1 µm. Therefore, the length of the extraction line in Figure 9 corresponds to the area of the oxide layer A_{Ox} in µm^2. Thus, the displacement current in the oxide layer can be

obtained by integrating the displacement current density from the "start" point to the "end" point:

$$I_{G,Miller} \approx I_{Ox} = \int_{start}^{end} j_{Dis,Ox} \cdot dA_{Ox} \,. \qquad (9)$$

Figure 10 shows the distribution of the displacement current in the oxide layer at the turn-off time t_1 and the turn-on time t_4. The orange parts represent the Miller capacitance and the generated displacement current. The blue colour parts represent gate-emitter capacitance and CPiC effect. It can be seen that at t_1 for turn-off, CPiC accounts for about 25.5% of the total gate current. And it is about 19.4% at t_4 for turn-on.

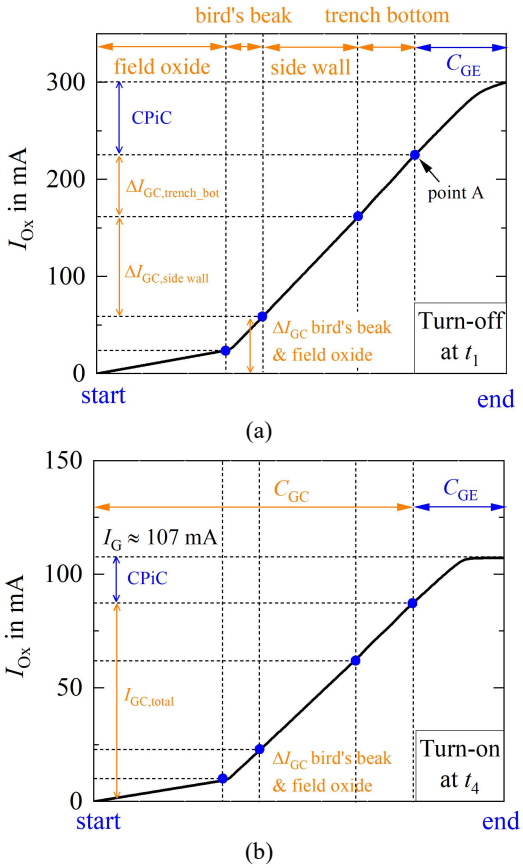


Figure 10: The displacement current through the corresponding part of the oxide layer I_{Ox}, (a) at turn-off t_1, (b) at turn-on t_4

		$I_{G,Miller} \approx I_{Ox}$	$I_{GC,total}$	CPiC	% of CPiC to I_{OX}
turn-off	t_1	300.4	223.6	76.8	**25.5**
	t_2	311.8	254.1	57.7	**18.5**
	t_3	311.8	267.7	44.1	**14.1**
	t_4	310.7	281.3	29.4	**9.5**
turn-oon	t_1	107.8	105.3	2.5	**2.3**
	t_2	107.7	97.02	10.7	**9.9**
	t_3	107.6	91.7	15.9	**14.8**
	t_4	107.2	86.4	20.8	**19.4**

Table 1: Displacement current generated by C_{GE} and C_{GC} at different time points and proportions to the total oxide current I_{Ox} during the Miller plateau with slow dV_{CE}/dt, current in mA

Table 1 summarizes the CPiC fraction from t_1 to t_4 during turn-on and turn-off. The main reason for the additional charge at the end of the Miller plateau is still the charging and discharging of the Miller capacitor. However, the CPiC generated in C_{GE} plays an essential role in the Miller plateau, too. This knowledge could be taken into account in the device design for further optimization of the switching (esp. dv/dt phase).

Conclusion

In this paper, the Channel Potential Modification induced Displacement Current during the Miller plateau of the trench-gate IGBT was introduced and verified by the TCAD simulation. Due to the channel voltage variation, the gate capacitance also generates a displacement current in the Miller plateau which is (eventually) compensated by the gate current. Therefore, the Miller plateau is also affected by the gate-emitter capacitance. The cell-design of the IGBT, especially the length of the channel, will have a significant impact on the CPiC.
In some scenarios, such as low-inductive short circuit type II, where the electron current in the channel changes sharply, the channel potential will also be affected by CPiC, and leads to an increased gate voltage overshoot [4].

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Compact GaN-based Bidirectional Polarization Super Junction HFETs with Schottky Gate on Sapphire

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Abstract

Performance evaluation of compact GaN-Based Bidirectional Polarization Super-Junction Heterojunction Field Effect Transistors with Schottky Gate (Bi PSJ SG HFET) fabricated on the sapphire substrate is presented in this paper. The on-state performance under various bias conditions is simulated and measured, and the operating mechanisms are analysed. Measured electric characteristics of fabricated Bi PSJ SG HFETs show symmetrical characteristics in the first and third quadrants, successfully realizing the bidirectionality. The logic function of the on-state performance of Bi PSJ HFETs is summarized. Numerical simulations show that a device can withstand high blocking voltages with a "box" like electric field in the common drift region. The measured average area-specific on-state resistance Ron. A of a Bi PSJ SG HFET is 64 mΩ.cm2 in both directions at room temperature for a device with a 40μm length of PSJ. In addition, temperature dependence on the area-specific on-state resistance of Bi PSJ SG HFETs with 40μm is also measured. Using analytical models of on-state resistance, the Ron. A is calculated and fit well with measured results with different PSJ length.

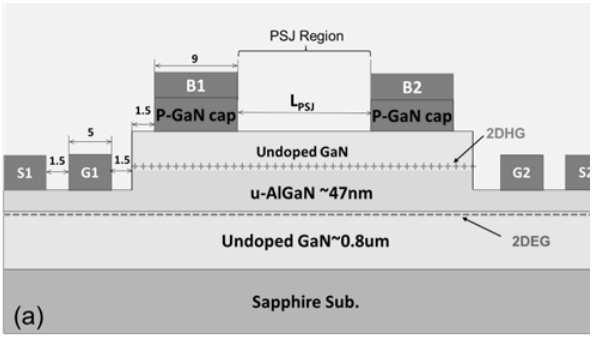
Keywords: GaN; Polarization Super Junction; bidirectional switch

INTRODUCTION

GaN-based power converters are attracting much attention and have become excellent candidates for power electronic applications because of their superior material properties. GaN devices with lateral structures utilizing high-mobility Two-Dimension Electron Gas (2DEG) have been extensively researched, and they dominate the GaN semiconductor market because of their low on-state resistances [1]. In 2006, the concept of Polarization Super Junction (PSJ) was proposed to enhance the breakdown voltage of GaN lateral devices and suppress current collapse ([2], [3]). PSJ technology is based on undoped GaN/AlGaN/GaN double heterostructures. It utilizes the charge compensation effect through high-density positive and negative polarization charges formed at each of the hetero-interfaces to enable a flat electric field distribution in the blocking condition [4]. GaN-based bidirectional Super Heterojunction Field Effect Transistors (BiSHFETs) with metal-semiconductor and PN junction gate structures using the PSJ concept was first demonstrated in 2012[5]. This paper proposes more compact Bidirectional PSJ HFETs with Schottky Gate (Bi PSJ SG HFETs) on sapphire substrate. Such monolithic bidirectional devices fabricated on insulator substrates are seen as essential elements for the next generation of ultra-compact and efficient power electronics systems [6]. There are previous reports on simulation and experimental demonstration of monolithic bidirectional switches reported in Silicon ([7], [8]), SiC ([9], [10]) and conventional GaN[11].

DEVICE STRUCTURE

Fig.1(a) shows a simplified cross-section of a bidirectional PSJ HFET with Schottky Gate (Bi PSJ SG HFETs) with geometric parameters. As shown in Fig.1(a), the basic structure of the Bi PSJ HFET arises from GaN/AlGaN/GaN double heterostructures which employs an inherent charge balance in the common PSJ drift region. The Bi PSJ HFET with Schottky Gate is a symmetrical device with six electrodes. There are two source electrodes (S1 and S2), two base electrodes (B1 and B2), and two gate electrodes (G1 and G2). S1 and S2 form ohmic contacts to 2DEG, while G1 and G2 form Schottky contacts. Two base electrodes (B1 and B2) are ohmic to 2DHG and can be connected to the sources (S1 and S2) or the gates (G1 and G2) to form four-terminal devices. When bases are connected with adjacent sources, the device can provide an inherent body diode in either direction [12]. The distance between two base electrodes is defined as the length of the PSJ region (L_{PSJ}). The schematic equivalent circuit



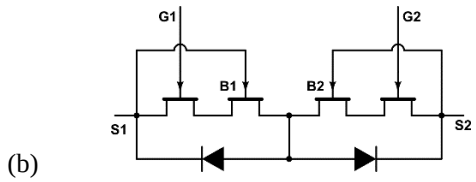


Figure 1: (a) A simplified cross-section of Bidirectional PSJ HFETs with Schottky Gate. Dimensions are in µm. (b) The schematic equivalent circuit of Bi PSJ SG HFETs.

in Fig.1(b) stands for Bi PSJ SG HFETs considered in this study.

Like unidirectional PSJ HFETs, the L_{PSJ} is used to support the forward blocking voltage and can be scaled up directly as a function of its length ([2], [13]). As reported in [4], a unidirectional PSJ HFET with L_{PSJ} of 40µm can withstand blocking voltages above 3 kV.

DEVICE SIMULATION

The device behaviour of Bi PSJ SG HFETs with 40µm-L_{PSJ} has been analyzed under various bias conditions by TCAD simulation and validated with experiments [7]. The simulated device structure is shown in Fig.1(a), which corresponds to fabricated devices with parameters as described later. In this study, Base (B1 and B2) electrodes are connected to the adjacent sources acting as a four-terminal device.

On-state Characteristic

Fig. 2 and Fig.3 shows simulated I_{s2}-V_{s2s1} characteristics of Bi PSJ SG HFETs with 40µm-L_{PSJ} working under two different bias conditions. Inset figures in Fig.2 and Fig.3 are simplified testing circuits.

Fig.2 shows simulated symmetrical I_{s2}-V_{s2s1} characteristics of Bi PSJ SG HFETs with 40µm- L_{PSJ} in both directions. According to a condition of Source 2 voltage with respect to Source1 voltage, the I_{s2}-V_{s2s1} characteristics can be divided into two regions, which are defined as 'Forward Region' and 'Reverse Region'. Here, the 'forward' refers to the S2 voltage being positive with respect to S1 (V_{s2s1}>0), and the 'reverse' refers to V_{s2s1} as negative (V_{s2s1}<0). In the forward region, Gate2 is referenced with respect to adjacent S2 (V_{g2s2}=0V) while the voltage of Gate1 changes from -6V to 0V with a 1V step, as shown in the inset circuit in Fig.2. Here, the device works as a three-terminal GaN device. In a manner like a conventional HFET, the forward current Is2 flows from S2 to S1 through the 2DEG and is controlled by Gate1 voltage (V_{g1s1}). As V_{g1s1} reduces to less than -6 V, the device enters off-state. The simulated forward on-state resistance (Ron) for L_{PSJ}=40µm is 33 Ω.mm at V_{s2s1}=1V, V_{g1s1}=0V. In the reverse region, Gate1 is connected with Source1. Simulated reverse characteristics of I_{s2}-V_{s2s1} are identical to that of forward because Bi PSJ SG HFETs have a symmetrical structure.

In Fig.3 the simulated I_{s2}-V_{s2s1} characteristics are obtained when keeping a negative Gate2 voltage with

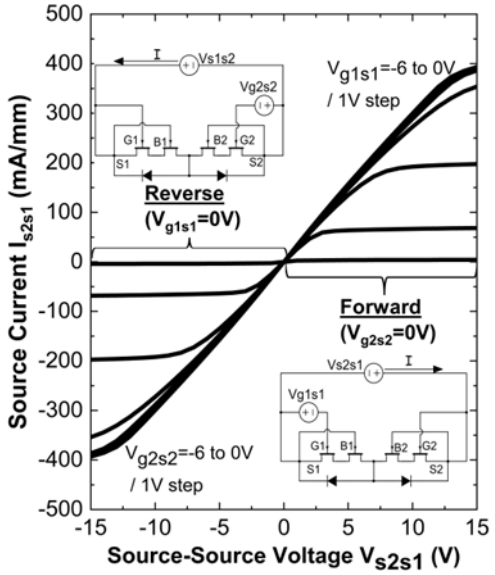


Figure 2: Simulated forward Is-Vs2s1 characteristic of Bi PSJ SG HFETs in both directions.

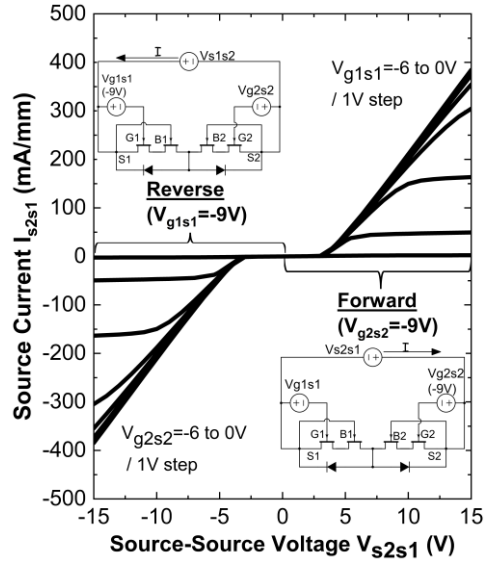


Figure 3: The simulated Is2-Vs2s1 characteristic with a negative gate2 voltage Vg2s2 of -9V (Vg2s2=-9V) in the forward region while -9V Vg1s1 in the reverse region.

respect to Source2 at -9V in the forward region while keeping V_{g1s1}=-9V in the reverse region. Source current I_{s2s1} in the forward and reverse bias condition is successfully controlled by Gate1 voltage (V_{g1s1}) and Gate2 voltage (V_{g2s2}) respectively, although the on-state voltage increases. The main reason for the increased 'forward' on-state voltage is that the 2DEG under Gate2 is fully depleted when the applied Gate2 voltage is negative, which is smaller than the threshold voltage. Therefore, the region under Gate2 performs as a diode depletion region. The calculated 'forward' on-state voltages at I_{s2} = 10mA/mm is 0.4 V (V_{g2s2} = 0 V) and 3.1 V (V_{g2s2} = -9 V) respectively. In the reverse region, the region under Gate1 is depleted.

Bias conditions			Device State
V_{s2s1}	V_{g1s1}	V_{g2s2}	
V_{s2s1}>0	On	On	On
	On	Off	V_{on} increase
	Off	On	Off
	Off	Off	Off
V_{s2s1}<0	On	On	On
	On	Off	Off
	Off	On	V_{on} increase
	Off	Off	Off

Table 1: Summarised device behaviour

According to the simulated results, the logic behaviour of bidirectional PSJ Schottky Gate HFETs in various bias conditions can be summarized in Table 1, which is in agreement with the simulation results reported in [5]. When V_{s2s1} is positive, Bi PSJ SG HFETs are controlled by Gate 1, while Bi PSJ HFETs are controlled by Gate 2 in a reverse bias condition.

Off-state Characteristic

Fig.4(a) shows the simulated off-state 2-D electrical potential distribution at a forward bias of V_{s2s1}=*8200V*, V_{g1s1}=*-15V and* V_{g2s2}=*0V* in an ideal case. The equipotential lines are distributed almost uniformly along the PSJ region. Under a forward bias of V_{s2s1}, G2 and S2 are connected as 'Drain' of three-terminal devices, and G1 is applied with -15V to turn off the device. The 2DHG and 2DEG of Bi PSJ SG HFETs are discharged through Base and 'Drain', respectively. Once the drift region between two bases of the Bi PSJ SG HFET is depleted, and flat electrical field distribution can be obtained over this region dur to charge balance between 2DHG and 2DEG. Fig.4(b) and Fig.4(c) are the 1-D potential distribution and the 1-D electric field along the x-coordinate at a position identified by the black dotted line (A-A') of Fig.4(a), respectively. As shown in Fig.4(c), the electric field is over the PSJ region, and the breakdown occurs at the edge of the Base. Under ideal forward blocking conditions, the simulated breakdown Voltage (BV) of Bi PSJ SG HFETs with 40µm-L_{PSJ} is 8260V at V_{g2s2}=0V, well above 3.3kV.

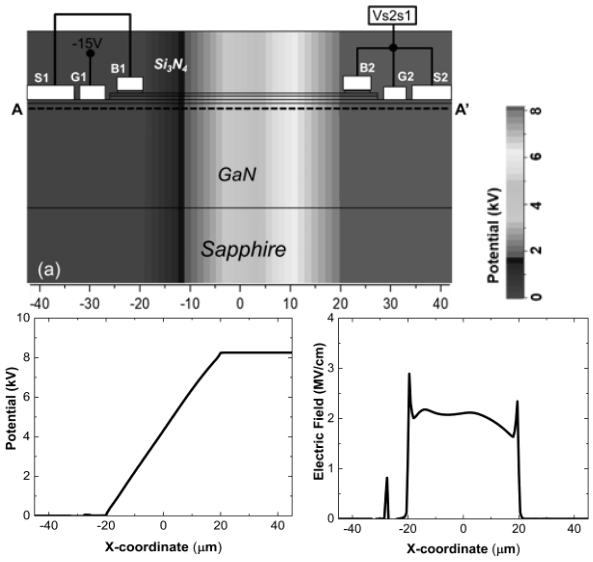


Figure 3: (a) The off-state 2-D electrostatic potential distribution at a forward bias of Vs2s1=8200V, Vg1s1=-15V and Vg2s2=0V. (b)The 1-D potential distribution and (c)The 1-D electric field intensity along the x-coordinate along the black dotted line (A-A') in Fig.4(a).

Previous results on unidirectional PSJ HFETs show a linear relationship between breakdown voltage and PSJ length ([4], [7]). Based on this, conservatively, it can be estimated that BV increases by 500 V for every 5µm increase in L_{PSJ}. Considering that the measured BV is around 2.5kV for a unidirectional PSJ HFET with 20µm-L_{PSJ} [13] on Sapphire, a bidirectional device with a 40µm-L_{PSJ} can be reasonably expected to withstand the voltage well above 3.5 kV.

EXPERIMENTAL RESULTS

Fig.5 shows the simplified cross-section of fabricated Bi PSJ SG HFETs with 40µm-$L_{PSJ.}$ Generally, the GaN buffer layer of GaN HEMTs is doped by acceptors like Carbon (C), which can help prevent leakage through the buffer region by lifting the GaN conduction band upwards by better confining the 2DEG channel and preventing the 2DEG spillover effect in the buffer. In this study, in order to only observe the polarization superfunction related effects on 2DEG/2DHG charge control conventional background, Carbon acceptor

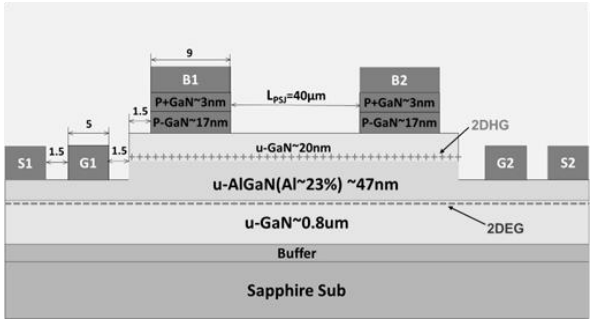


Figure 4: A simplified cross-section of fabricated Bi PSJ SG HFETS with 40µm-L_{PSJ}.

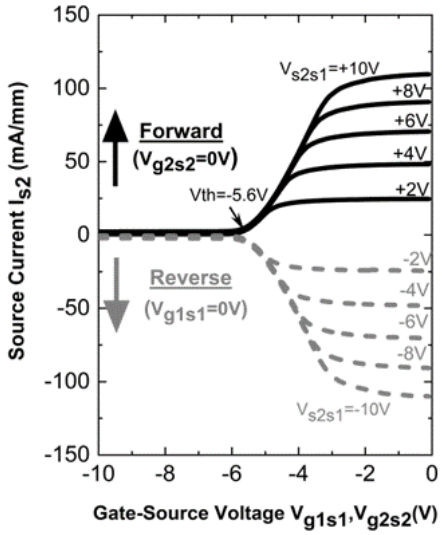


Figure 5: Measured transfer characteristics of fabricated Bi PSJ SG HFETs in both directions.

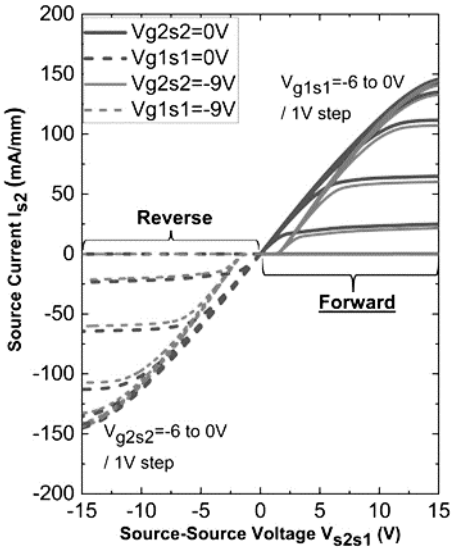


Figure 7: Measured Is2-Vs1s2 characteristics of fabricated Bi PSJ SG HFETs in both directions with various bias conditions.

doping is not used in the GaN buffer region. These Bi PSJ SG HFETs are built on undoped GaN/AlGaN/GaN double heterostructures grown on a sapphire substrate. It consists of an 0.8µm-thick undoped GaN buffer layer (u-GaN), a 47nm-thick un-doped AlGaN layer with an Al composition of 23%, and a 20nm-thick un-doped GaN layer. A 17nm-thick p-type doped GaN cap (P-GaN) layer with $5 \times 10^{19} cm^{-3}$ and a 3nm-thick P-GaN layer with $2 \times 10^{20} cm^{-3}$ have been grown on u-GaN, which enable an ohmic contact to 2DHG. Fabricated Bi PSJ SG HFETs on Sapphire substrate have four pads of Gate1, Gate2, Source1 and Source2. Two bases are connected to the adjacent source electrode, respectively.

Measurement of Fabricated Bi PSJ SG HFETs

Fig. 6 shows transfer characteristics of fabricated Bi PSJ SG HFETs with 40µm-L_{PSJ}. The Source current I_{s2} in the forward and reverse bias conditions are successfully controlled by Gate1 voltage (V_{g1s1}) and Gate2 voltage (V_{g2s2}), respectively. The threshold voltage V_{th} of Bi PSJ SG HFETs is 5.6V in both directions. Fig.7 shows I_{s2}-V_{s2s1} characteristics of the fabricated Bi PSJ SG HFET with 40µm-L_{PSJ}. Bias voltage settings are consistent with that in the simulation described earlier. As shown in the figure, the measured I_{s2}-V_{s2s1} characteristics are symmetrical in both directions and realize the logic functions of bidirectional switching shown in Table1. Calculated on-state voltages at I_{s2}=10mA/mm are 0.8 V (V_{g2s2} = 0 V) and 2.2 V (V_{g2s2} = -9 V) in the 'forward Region' at room temperature. Under different bias conditions, fabricated Bi PSJ SG HFETs can be operated as bidirectional switches, unidirectional HFETs with Drain Injection Transistor (DIT) mode and diodes in both directions.

Fig.8 shows the buffer leakage and the surface leakage of the inset structure in Fig.8. Without C-doping in GaN buffer layer, the unintentionally doped buffer layer ends up slightly n-type and causes buffer leakage issues. This buffer leakage is the dominant factor in the leakage current in the off state for Bi PSJ SG HFETs. The surface leakage, associated with poor passivation, surface states and sidewall damage, is reasonably low which suggests good process control. Due to the high buffer leakage, a slightly high leakage current of around 6mA/mm at 200V under forward blocking conditions was measured. Equipment compliance limits further forward blocking voltage measurement. Fig.9 shows the measured leakage currents between two bases of the device with 40µm-$L_{PSJ,}$ with a measured value of about 19nA/mm at V_{B2B1}=100V.

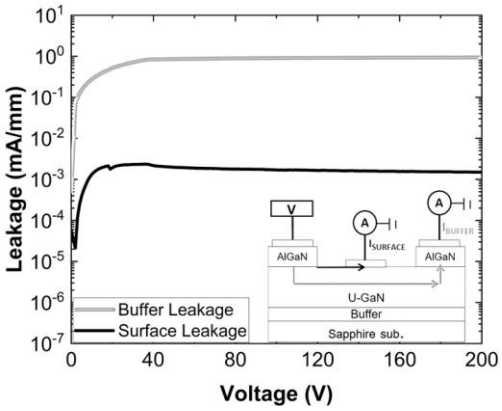


Figure 6: Measured buffer leakage and surface leakage.

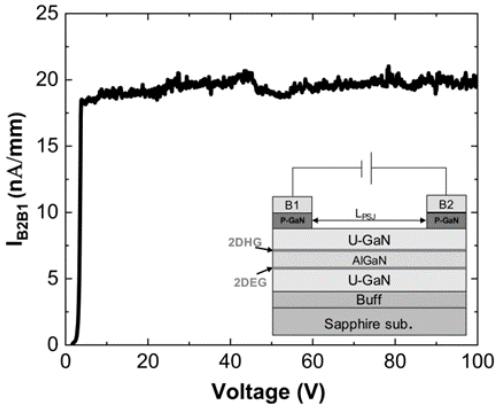


Figure 9: Measured leakage between B1 and B2.

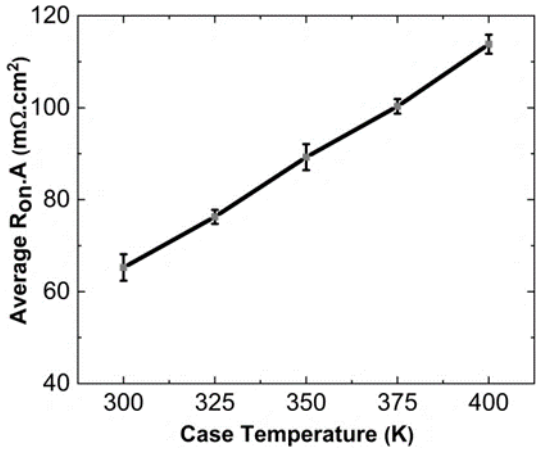


Figure 10: The average Ron. A of fabricated Bi PSJ SG HFETs with 40μm- L_{PSJ} at a temperature from 300K to 400 K.

This base leakage is obtained when keeping 2 gates floating and V_{s2s1} at 0V. The purpose of this study is to validate the device concept and functionality with different gate polarity control. Future work is needed with optimum epitaxial structure for demonstrating high voltage breakdown devices.

The average variation in Ron.A of 8 samples of Bi PSJ SG HFETs with 40μm-L_{PSJ} as a function of case temperatures are presented in Fig.10. When the temperature increases from 300K to 400K, Ron.A of Bi PSJ SG HFETs is found to increase from 65.24mΩ.cm2 to 113.82mΩ.cm2 in a linear fashion. The maximum discrepancy is within 5.31% of its mean value at 350K.

Calculation and Analysis on Ron.A

Under on-state conditions, the source current is flowing through the 2DEG and is controlled by Gate1 in the forward region and Gate2 in the reverse region. According to differences in the sheet carrier density and the mobility of 2DEG and 2DHG, Bi PSJ SG HFETs can be divided into different areas. As shown in Fig.11, along the dashed line which the current flow direction, the device can be divided into seven regions, namely the PSJ region, channel regions, gap regions, and contact regions. Gap regions consist of 2 areas between the source and the adjacent gate. Regions under 2 bases are defined as

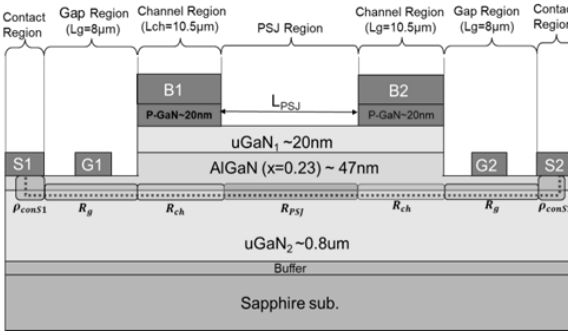


Figure 7: The calculated and measured Ron.A of Bi PSJ SG HFETs and PSJ OG HFETs with L_{PSJ} from 5μm to 40μm at room temperature.

channel regions, and contact regions are under source electrodes. Therefore, the total specific ON-state resistance (Ron.A) can be considered as the sum of the PSJ region resistance (R_{PSJ}), two channel region resistance (R_{ch}), and two gap regions resistance (R_g) multiplies the device area (A) and then plus the contact resistivity (ρ_{conS1} and ρ_{conS2}), as shown in Equation (1).

$$R_{on}A = (R_{PSJ} + 2R_{ch} + 2R_g) \times A + \rho_{conS1} + \rho_{conS2} \quad (1)$$

The contact resistivity of the Source1 and the Source2 electrode ($\boldsymbol{\rho_{conS1}}$ and $\boldsymbol{\rho_{conS2}}$) can be measured and calculated by the transmission line method (TLM), as shown in

$$\rho_{conS1} = \rho_{conS2} = R_c \times L_T \times W = 0.26\, m\Omega \cdot cm2 \quad (2)$$

The resistance of other regions can be expressed as

$$R = \frac{L}{\boldsymbol{q\mu\sigma W}} \quad (3)$$

Where q is the electron charge, W stands for the device width. μ stands for the mobility of 2DEG and σ is the 2DEG sheet density. L is the length of the region, which is shown in Fig.11.

In the calculation, the 2DEG mobility (μ) is set around 700cm^2/Vs same as the measured value, and the device width is assumed constant. The resistance of the PSJ region, gap regions and channel regions are determined by the length (L) and the sheet density (σ) of each region. The sheet density (σ) can be calculated by using analytical models of sheet carrier densities in PSJ HFETs[13], which is influenced by the thickness of PSJ layers and Al mole fraction. Considering that partial carriers are captured by traps which have gained high kinetic energy after being accelerated by the electric field, the sheet density of 2DEG is adjusted with experimental results.

Fig.12 presents the calculated and measured Ron.A of Bi PSJ SG HFETs with L_{PSJ} from 5μm to 40μm at room temperature. The identical Vg (Vg1) = 0V is applied to the calculation and measurement. As presented in Fig.12, calculated Ron.A of Bi PSJ SG HFETs fits well with the experimental results when altering PSJ length from 5 to 40μm. Factors like the fabrication misalignment between processes and random measurement errors attribute to differences in Fig.12. In addition, it should be noted that the 2DEG mobility for each region is assumed as constant in calculations, unlike actual devices, which can be affected by some factors, such as charge concentration and electrical field. The resistance of 2 gap regions (R_g) and 2 channel regions (R_{ch}) contribute to additional resistance for Bi PSJ SG HFETs, because of the thin AlGaN layer, the low Al mole function and the long region length. Table 2 shows the calculated resistance component ratio to the total Ron.A of Bi PSJ SG HFETs with L_{PSJ} from 5μm to 40μm. With the decrease in L_{PSJ}, the percentage of R_{ch} and R_g to the total Ron.A becomes large.

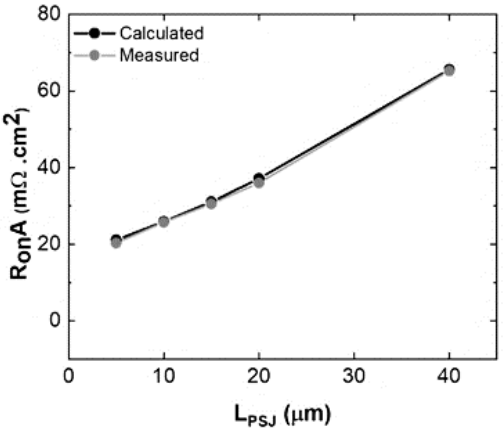


Figure 8: The calculated and measured Ron.A of Bi PSJ SG HFETs with L_{PSJ} from 5μm to 40μm at room temperature.

L_{PSJ} (μm)	Component Ratio (%)			ρ_{consS} (mΩ.cm^2)	Ron.A (mΩ.cm^2)
	R_{PSJ}	R_g	R_{ch}		
5	10	46	44	0.26	21.07
10	19	42	40		25.91
15	26	38	36		31.26
20	32	35	33		37.12
40	48	27	25		65.64

Table 2: Each component ratio to the total Ron in the Analytical model.

CONCLUSIONS

In this paper, the performances of compact bidirectional HFETs with Schottky Gate using the PSJ concept are presented. These devices share the same drift region in operation in the first and third quadrants and therefore can be one of the most compact bidirectional switches reported to date. The simulated and measured electrical characteristics display logic functions of bidirectional switching in various bias conditions. The simulated off-state I_{s2}-V_{s2s1} shows Bi PSJ SG HFET with a 40μm length can withstand the voltage well above 8 kV in an ideal condition. In any case, based on measured data of unidirectional PSJ HFETs fabricated on Sapphire using similar material configurations, off-state performances in excess of 3.3 kV are reasonable. The average measured area-specific on-state resistance Ron.A of Bi PSJ SG HFET with L_{PSJ}=40μm is 65.24 mΩ.cm2. The linear increase in the Ron.A as a function of temperature of Bi PSJ HFETs as well as the on-state resistance versus L_{PSJ} show that the device can be scaled easily scaled in both voltage and currents. We also built the analytical model of on-state resistance of Bi PSJ SG HFETs to calculate and analyze its components.

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High power thyristor with enhanced case non-rupture current capability

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Abstract

A new packaging technology for a phase-control thyristor providing enhanced case non-rupture current capability is presented. The new housing with 100 mm pole piece diameter is developed for thyristors and rectifier diodes rated at 6.5 kV to withstand currents applied in reverse direction up to 95 kA.

Keywords: phase-control thyristor, press-pack housing, hockey-puck housing, enhanced case non-rupture current capability.

INTRODUCTION

Press-Pack (Fig. 1) phase-control thyristors (PCT) are favored solution for high power applications such as high-power rectifiers, motor drives, HVDC and more [1]. The PCT is still the number one choice for such applications due to its unique trade-off between low conduction losses, reliability, and high blocking capability [2]. In the applications mentioned above, fault situations may occur which can cause the power semiconductor device to lose its blocking capability and eventually expose it to excessive fault currents in reverse direction. The excessive currents will then cause arcing inside the press-pack. As a result of the extreme heat (approx. 20'000 °C), the internal atmospheric pressure increases massively, and the hermetic sealing of the press-pack housing is at risk. The magnitude of the reverse current limit without damaging the housing is defined as the case non-rupture current I_{RSMC} [3].

Fig. 1: Press-Pack or Hockey-Puck type of housing.

EXPERIMENTAL

The new package for the PCT is equipped with additional protection elements to strengthen its resistance against electric arcs. Fig. 2 shows a cross section of the enhanced packaging design with the three key elements: the additional flange or protection disc (yellow), the polymer-based protection-ring (blue) and the oval shaped O-ring (dark grey) clamped in-between. The differences become especially apparent when comparing to a standard version as shown in Fig. 3.

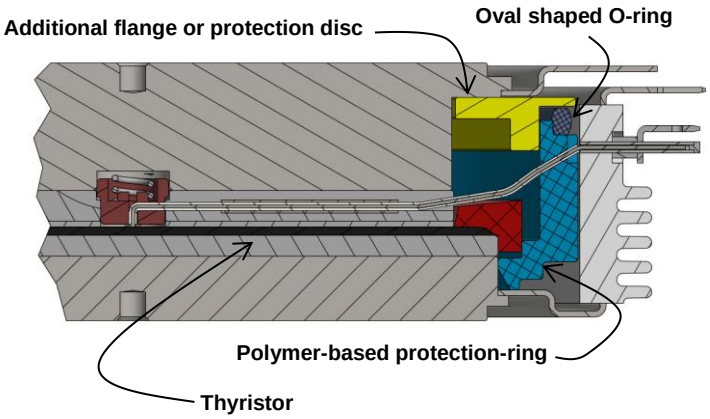

Fig. 2: Cross-section of the new packaging for phase control thyristors providing enhanced case-non rupture current capability.

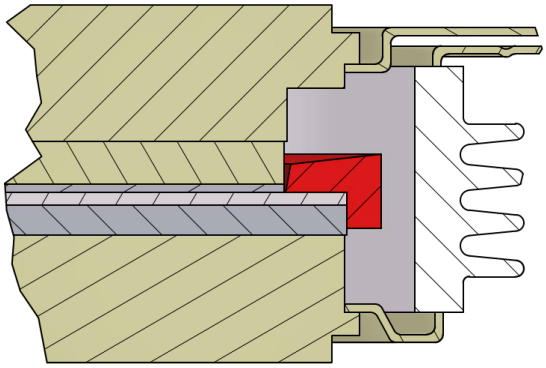

Fig. 3: Cross-section a standard packaging for phase-control thyristors.

The I_{RSMC} capability was assessed in accordance with the international standard IEC 60747-6:2016. Prior to the experimental testing, the devices were damaged mechanically on the junction termination to ensure the failure location occurs at the edge of the silicon wafer. This is needed to ensure the testing is conducted under extreme conditions where the packaging sealing is directly exposed to the electric arc. The case-non rupture current testing was then conducted in the KEMA Labs in Prague by applying 10 ms sinusoidal current pulses in reverse direction (Fig. 4). The device was in-situ video-recorded using a high-speed IR-camera to observe if and how the plasma is escaping. Based on this, an optimized design was developed.

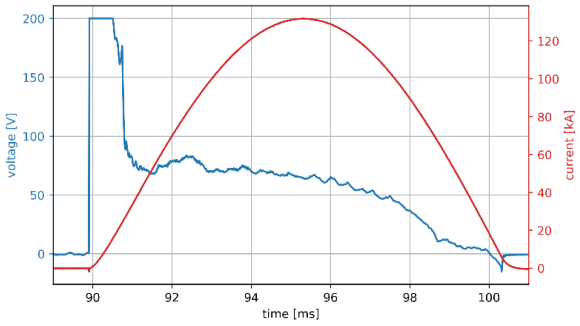

Fig. 4: Measured current and voltage waveform of the I_{RSMC} testing.

The predetermined breaking point was designed at the top flanges to avoid the ceramic housing to break which could cause further damages to the converter installation. This was confirmed by experimental testing. The experimental investigations led to the conclusion that reverse 10 ms sinusoidal current pulses up to 95 kA can be withstood without impairing the hermetic sealing.

Pre-damaged PCT wafers

All devices (PCT wafers 6.5 kV) were pre-damaged in the bevel area by a laser (Fig. 5) and later electrically (capacitor discharge) to ensure low remaining blocking voltage (< 1 kV). This procedure is required to control to location where the arc is generate and gives the needed freedom to external facility to set the current value in the desired range. A high remaining voltage may negatively influence the accuracy of set current. The wafer pre-damage is out of the contact area and thus represents the worst case scenario for case non rupture current test, which is a device failure at bevel area.

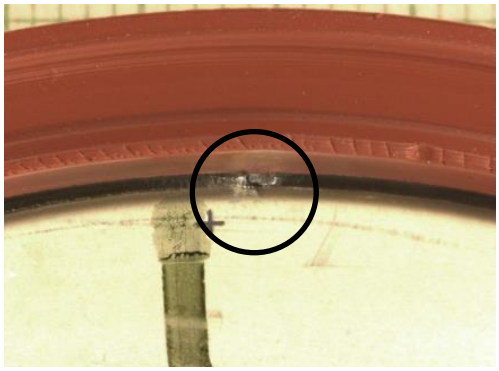

Fig. 5: Pre-damaged area (circled) on bevel situated under red rubber.

ENHANCED CASE NON-RUPTURE CAPABILITY

As has been already shown in Fig. 2, the enhanced case non-rupture capability is ensured by three key elements:

Oval shaped O-ring

One of the important parts is the silicone rubber O-ring with an elliptic or oval shaped cross-section. This special type of ring enables to use one design of housing assembly for different Si-wafer thicknesses and to deal with manufacturing tolerances (Fig. 6).

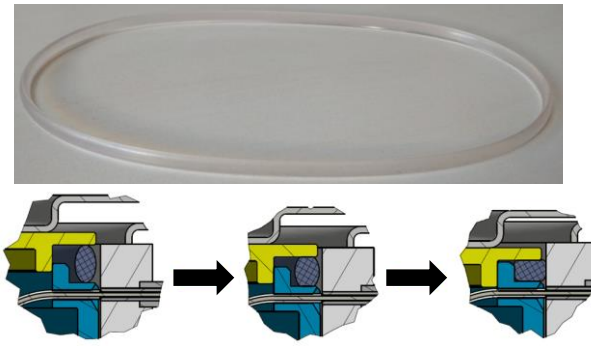

Fig. 6: The silicon O-ring (top) and a deforming mechanism of the O-ring if a thinner wafer is present (bottom).

Polymer-based protection ring

It is obvious that polymer-based protection ring acts like a protection against rupture of the ceramic insulator and also against an exposure of hot plasma which will arise as a consequence of reverse short-circuit failure. The key parameters for the polymer selection were the permanent operating temperature, pressure development, CTI index, water absorption, tensile strength, low flammability, price and manufacturability which led to three polymer families: PTFE, PPA and PPS.

Price, manufacturability, permanent operating temperature. PTFE can't be manufactured by injection molding which is known to be cheaper in the long term than machining from semi-finished product. PPA & PPS have also good price/power ratio in regards to the permanent operating temperature. PEEK and other high-tech polymer families with higher permanent operating temperature weren't considered because they are just too expensive and challenging for the manufacturing.

It is not all only about type of main polymer family. At first, we thought that PTFE can very well withstand the hard conditions because of its well-known ability to resist a high heat. However, in agreement with polymer experts that the main feature helping to withstand high heat is the level of filling and not only the type of polymer family. Due to reinforcements from mineral fills or glass fibers, polymer can survive (Fig. 7). This allows to use PPA & PPS polymer family for the protection ring. Higher CTI points to the PPA family instead of PPS which is obvious.

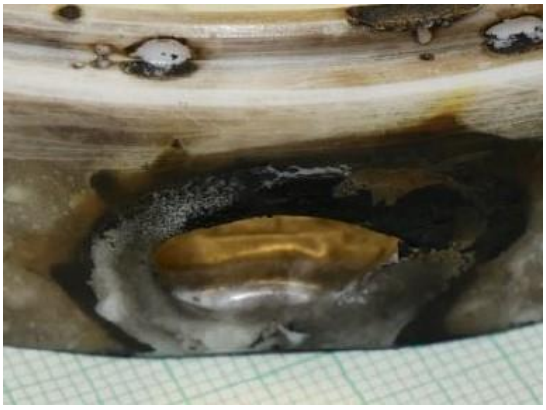

Fig. 7: Burned hole in PTFE protection ring with no mineral or glass fiber filling.

Flammability and flame retardants. Flame retardants were not observed to improve the protection properties of the protection ring. In fact, on the contrary, these retardants could negatively influence a resilience of the ring and the injection molding is more challenging.

The more filling, the more fragility. Lack of mineral filling or glass fiber-reinforcement leads to a burn-through failure of the protection ring. Too high level of filling can lead to cracks of the ring which causes a break on ceramic insulator and escape of hot gases. Therefore, the impact strength [kJ/m2] is very important factor and needs to be chosen wisely (Fig. 8).

Fig. 8: Brittle fracture on polymer protection ring with too high reinforcement filling caused by massive pressure increase in the housing during reverse short-circuit failure.

Additional flange or protection disc

The last key protection element is protection disc which mainly protects the thin cathode top flange area. The disc is tightly centered by the protection ring and remains on the oval shaped silicon O-ring which also presses the protection disc tightly onto the thin cathode top flange area. The behavior of the protection disc made from polymer and steel was investigated.

Polymer protection disc. It might seem that the polymer protection disc would totally protect the thin top flange against a burn-through failure. However, an annealing from both polymer parts together with massive pressure development from a hot in-housing atmosphere caused a total destruction of the housing (Fig. 9 & Fig. 10).

Fig. 9: Destroyed housing where both key features were made from polymer (current magnitude approx. 85 kA).

Fig. 10: Test setup in KEMA Labs in Prague (top), destroyed clamped housing where both key features were made from polymer (current approx. 85 kA) (middle), massive plasma escape captured on high-speed camera (bottom).

Steel protection disc. The steel protection disc is an ideal configuration which, according to the experiments, can withstand a maximal reverse 10 ms sinusoidal current pulses $I_{RSMC\text{-}MAX}$ of approx. 115 kA without compromising the housing hermeticity (Fig. 11).

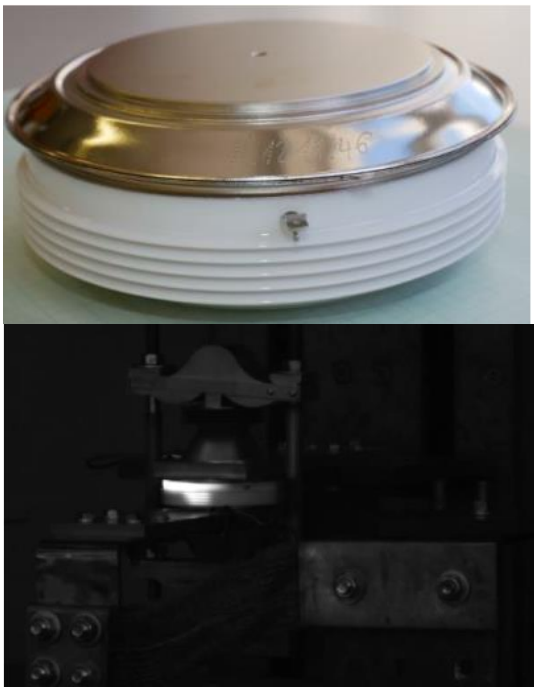

Fig. 11: Housing without hermeticity failure after 10 ms sinusoidal current pulse below or near $I_{RSMC\text{-}MAX}$ (top), photo from high-speed camera during pulse below or near $I_{RSMC\text{-}MAX}$ (bottom).

However, in order to provide a sufficient safety margin the magnitude of I_{RSMC} was set to 95 kA. In case that the $I_{RSMC\text{-}MAX}$ is exceeded, the plasma from the reverse short-circuit failure escapes from the housing in a controlled or predetermined way according to Fig. 12.

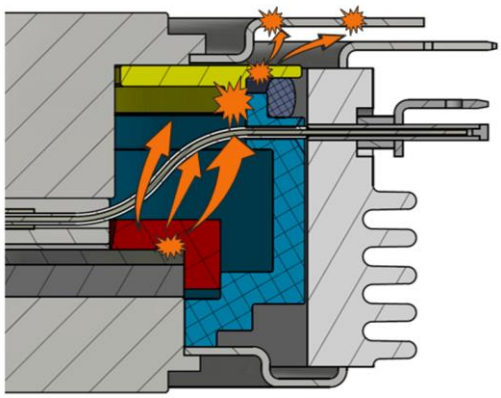

Fig. 12: Controlled or predetermined mechanism of plasma escaping.

This is usually causing only one or several small holes like on Fig. 13, which is less dangerous than shattered flying ceramic parts which can cause injury to people or destroy equipment or installations (Fig. 10).

Fig. 13: Melted spot (circled) on top flange where the plasma escaped (top), photo from high-speed camera when $I_{RSMC\text{-}MAX}$ is exceeded (bottom).

Ceramic foam ring

One of the tested designs contains an additional ceramic foam ring (Fig. 14). This feature improves the case non-rupture performance of the press-pack housing by an absorption of mechanical and thermal energy from the arc. However, this solution is not possible to use in industrial standard applications due to its high fragility which can caused unforeseen circumstances in the housing during transportation or thermal cycling. Nonetheless, this configuration enabled an $I_{RSMC\text{-}MAX\_CERAMIC}$ of approx. 135 kA.

Fig. 14: Assembly with an additional ceramic foam ring (top) and the whole assembly with mounted protection disc but without a housing lid or cathode pole-piece (bottom).

CONCLUSION

A new packaging approach for press-pack phase-control thyristors was presented. The enhanced case-non rupture current capability offers improved safety and reliability in case of fault events for high-power rectifier converters. This was achieved by implementing the three key protection features (polymer protection ring, steel protection disc and silicon oval O-ring) which provide the case non-rupture current I_{RSMC} = 95 kA with a sufficient safety margin.

Abbreviations

Comparative tracking index (CTI)

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Novel Constant Surface Concentration Depletion Mechanism and Its Experiments in Homogenization Field LDMOS

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Abstract

A novel constant surface concentration depletion (CSD) mechanism for the homogenization field (HOF) LDMOS is proposed and experimentally demonstrated in this paper. Because the depletion of the HOF LDMOS is independent on the P-substrate, the surface doping concentration of the HOF LDMOS can keep constant and thus the total doping dose of the N-drift region can increase with the junction and trench depths. Based on the CSD mechanism, a CSD HOF LDMOS with 15 μm trench depth was designed and experimentally fabricated. The doping dose of the N-drift region is increased up to 8 × 10^{12} cm^{-2}. As a results, a measured low specific on-resistance $R_{on,sp}$ of 15.6 mΩ·cm^2 was observed under a breakdown voltage V_B of 420 V, realizing a high figure of merit FOM = V_B^2 / $R_{on,sp}$ of 11.3 MW/cm^2 and a reduction of 53.3% compared with the theoretical limit of the triple RESURF technology under the same V_B. $R_{on,sp}$ of the CSD HOF LDMOS also realizes a reduction of 20.8% when compared with that of the best-in-class HOF LDMOS.

Keywords: Homogenization field, LDMOS, Breakdown voltage, Specific on-resistance, Constant surface concentration depletion

I. INTRODUCTION

To achieve higher breakdown voltage V_B and lower specific on-resistance $R_{on,sp}$, integrated power devices have been developed from the single reduced surface field (RESURF) to double and triple RESURF technologies [1]-[3]. Furthermore, the superjunction concept was introduced into the integrated devices to further enhance the doping concentration in the drift region and reduce $R_{on,sp}$ [4]-[9]. Drift regions of these devices are mainly depleted by PN junctions with charge balance between immobile positive and negative ionized charges. As a result, there exists a theoretically fixed optimized doping dose D_N for a given region, such as the well-known RESURF dose:

$$D_N = 1\times10^{12} \quad \mathrm{cm}^{-2} \tag{1}$$

For the device formed through implantation annealing processes, the drift region exhibits a Gaussian distribution. It is revealed from (1) that D_N of the RESURF device is independent on the junction depth. Then, the surface doping concentration N_s of the device decreases with an increase in the depth of the doping junction. The different constant doping doses has also been discussed by both analytical models and experiments [8]-[11]. This phenomenon is referred to as constant dose depletion in this paper.

Recently, a new type of homogenization field (HOF) devices have been reported [12]-[14]. The HOF devices feature periodic MIS structures in the drift region to fully deplete the highly doped N-type region. Consequently, the depletion in the HOF device is relatively independent of the PN depletion, showing a self-charge balance by the discrete MIS arrays. However, the depletion mechanism of the HOF device has not been deeply researched, yet.

In this paper, a novel constant surface concentration depletion (CSD) mechanism for the HOF laterally diffused metal oxide semiconductor (LDMOS) is proposed and experimentally demonstrated. Section II gives the HOF structure and CSD mechanism. Section III presents experiments and discussions.

II. STRUCTURE AND MECHANISM

2.1 HOF Structure

The structure of the HOF LDMOS is shown in Fig. 1, which is characterized by the deep insertion of periodically discrete MIS trenches into the drift region. MIS trenches, located at an equal distance from the source end, are connected through surface metal

interconnects, forming a MIS depletion array that effectively depletes the entire drift region. The depletion region of the HOF structure is determined by the depth of the MIS trenches. As a result, the depletion mechanism of the HOF device is different from that of the conventional (Con) LDMOS.

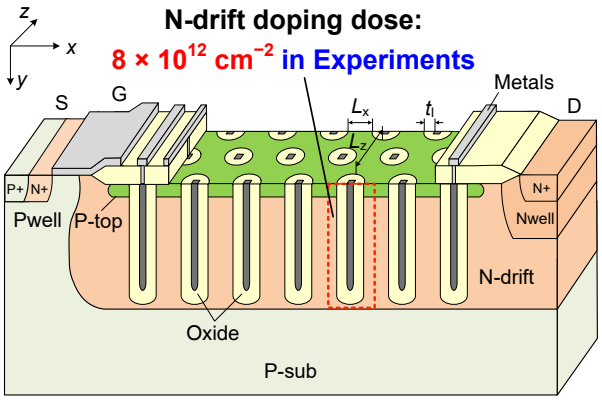


Fig. 1 Structure of CSD HOF LDMOS. The periodic discrete MIS trenches are introduced deep into the drift region to form the constant surface concentration depletion. A high D_N up to 8×10^{12} cm^{-2} was demonstrated in experiments.

2.2 CSD Mechanism

Since the depletion of the drift region in HOF devices is independent of the P-substrate and primarily depends on the trench depth, a deeper trench enables the depletion in deeper region into the device. Under a Gaussian distribution, a constant surface doping concentration N_s can be maintained while increasing the depth of the junction in the drift region, i.e., increasing the standard deviation σ, thus achieving a continuously increased D_N. The CSD mechanism is shown in Fig. 2.

Fig. 2(a) presents the schematic diagram of the CSD mechanism based on 3-D MIS assisted depletion. The constant N_s in the HOF LDMOS is maintained, while the D_N is increased as the junction depth of the N-drift and trench depth increase. The analytical model for the HOF device has been reported in [12]. The design formula for N_s is as follows:

$$\frac{\varepsilon_s E_c}{qT}\tanh\left(\frac{L_x}{2T}\right) \le N_s \le \frac{\varepsilon_s E_c}{qT} \tag{2}$$

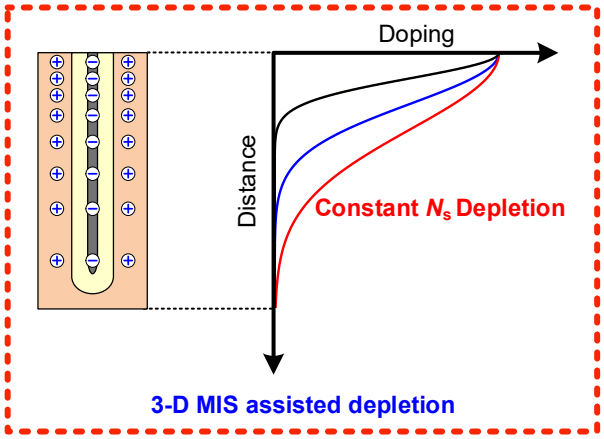
where ε_s is the dielectric constant of the silicon and q is the electron charge. L_x is the distance between trenches in the x-direction. E_c and T are the critical electric field and characteristic thickness that can be calculated by:

$$\begin{cases} T = \sqrt{\dfrac{L_z^2}{8} + \dfrac{\varepsilon_S}{2\varepsilon_I} t_I L_z} \\ E_c = 6.645 \exp(1.636 L_d^{-0.1269}) \end{cases}$$

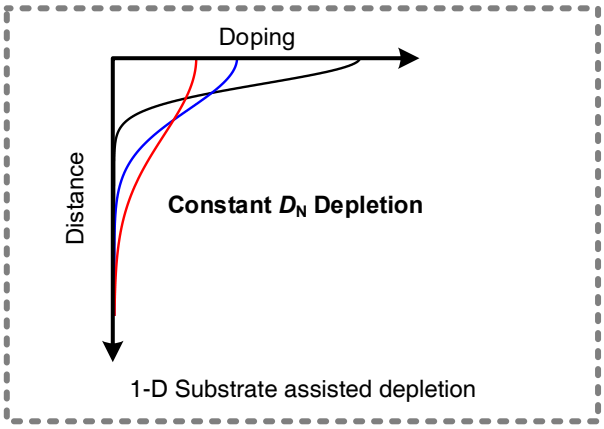
with L_z, L_d, t_I and ε_I being the distance between trenches in the z-direction, the drift region length, the thickness and dielectric constant of the oxide. Under the Gaussian doping distribution, D_N can be obtained by integrating the doping concentration in the y-direction of the drift region as follows:

$$D_N = \int_0^\infty N_s \exp\left(-\frac{y^2}{2\sigma^2}\right) dy = \sqrt{\frac{\pi}{2}} N_s \sigma \tag{3}$$

D_N of the HOF device increases monotonically with the junction depth or σ, with $D_N \propto \sigma$. Then, D_N of the HOF device can be significantly increased to reduce $R_{on,sp}$. In contrast to this, the Con device based on 1-D substrate assisted depletion, with $D_N \approx$ constant, cannot introduce more conduction carriers by increasing the junction depth alone, as shown in Fig. 2(b).



(a)



(b)

Fig. 2(a) CSD mechanism of the constant N_s depletion. N_s of the HOF LDMOS can keep a constant and the D_N is increased with the increases of the junction depth of the N-drift and trench depth; (b) The constant D_N depletion in the Con RESURF LDMOS with increase junction depth and reduced N_s.

III. DESIGN AND EXPERIMENTS

3.1 Design of CSD HOF LDMOS

Design formula (3) provides a very simple guideline for the HOF devices, where improving device characteristics can be achieved by simply increasing the junction and trench depths in the drift region. Compared with our previous work [14], the trench depth is increased from 12 μm to 15 μm and the corresponding D_N is increased from 6.8×10^{12} cm^{-2} to 8×10^{12} cm^{-2}. Based on the CSD mechanism, it is possible to achieve a predictable decrease in $R_{on,sp}$ while maintaining a constant V_B.

Fig. 3 compares the equipotential line distributions of CSD HOF LDMOS and Con LDMOS at breakdown. In the CSD HOF LDMOS device, the drift region is fully depleted by the MIS deep trench, resulting in a uniform distribution of the equipotential lines throughout the device. In contrast, the Con LDMOS exhibits an obvious neutral region, which leads to premature breakdown at the source end of the device.

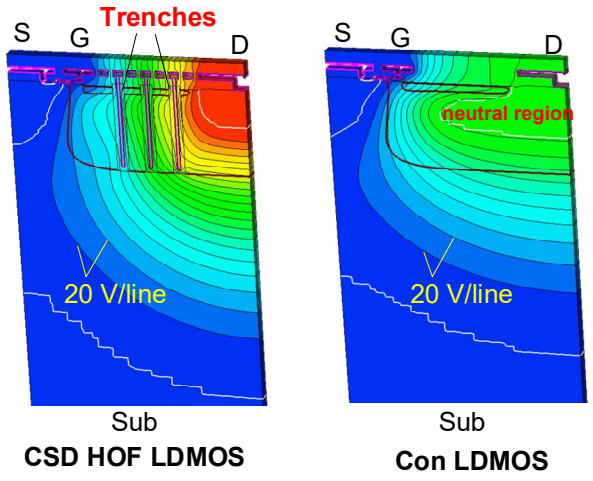


Fig. 3 Equal-potential lines of CSD HOF LDMOS and Con LDMOS. The drift region of the HOF LDMOS is fully depleted because of the CSD mechanism and an obvious neutral region is observed in the Con LDMOS.

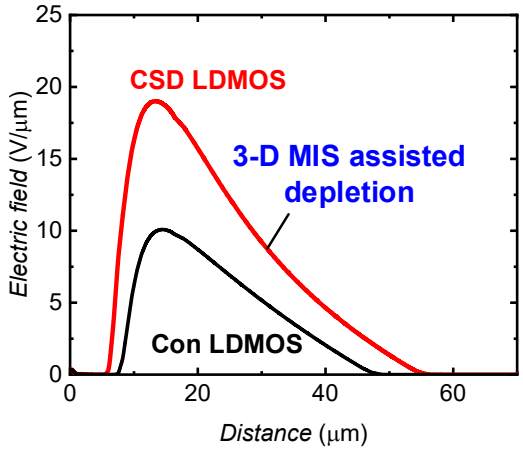


Fig. 4 Vertical electric field distributions of CSD HOF LDMOS and Con LDMOS. The peak field of the CSD HOF LDMOS is increased from 10 V/μm of the Con LDMOS to 20 V/μm by the 3-D MIS assisted depletion.

Fig. 4 compares the electric field distributions under the drain of CSD HOF LDMOS and Con LDMOS. The CSD HOF LDMOS demonstrates a peak electric field of 20 V/μm because of the 3-D MIS assisted depletion. In contrast, the vertical electric field of the Con LDMOS is limited to 10 V/μm due to the premature breakdown at the surface. Compared with the Con LDMOS, the simulated V_B of CSD HOF LDMOS is increased from 212 V to 439 V, showing a significant 107% improvement, as illustrated in Fig. 5.

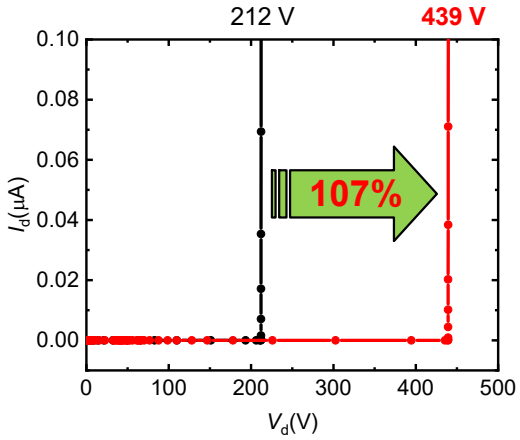


Fig. 5 Simulated V_B of CSD HOF LDMOS and Con LDMOS. V_B of the CSD HOF LDMOS is increased by 107% when compared with that of the Con LDMOS.

3.2 Experiments of CSD HOF LDMOS

Based on the 0.5 μm Central Semiconductor Manufacturing Corporation (CSMC) process platform, a CSD HOF LDMOS was fabricated. Fig. 6 presents the micro photo and layout of the drift region for the CSD HOF LDMOS, featuring the introduction of 7 trench arrays in the drift region. In comparison to the device in [14], the HOF device designed using the CSD mechanism incorporates 15 μm deeper trenches to deplete a higher D_N of 8×10^{12} cm^{-2}.

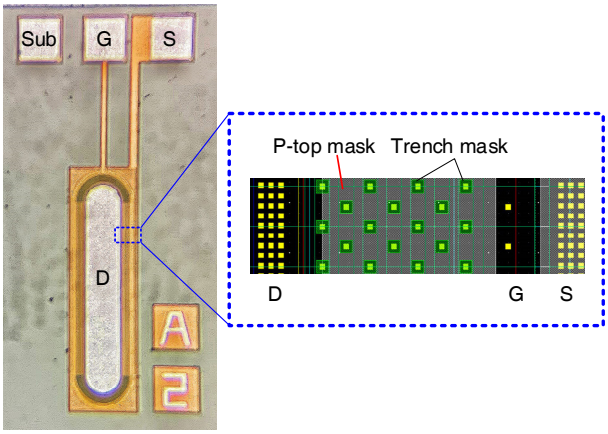


Fig. 6 Micro photo and layout of CSD HOF LDMOS. Deep trenchs of 15 μm were formed in the drift reigon with 7 trench arrays.

Fig. 7 illustrates the measured I_d - V_d curves of the CSD HOF LDMOS device in the off-state and on-state. The testing results reveal a V_B of 420 V and an $R_{on,sp}$ of 15.6 mΩ·cm^2. This achievement corresponds to a high figure of merit *FOM* of 11.3 MW/cm^2, calculated using the formula $FOM = V_B^2 / R_{on,sp}$.

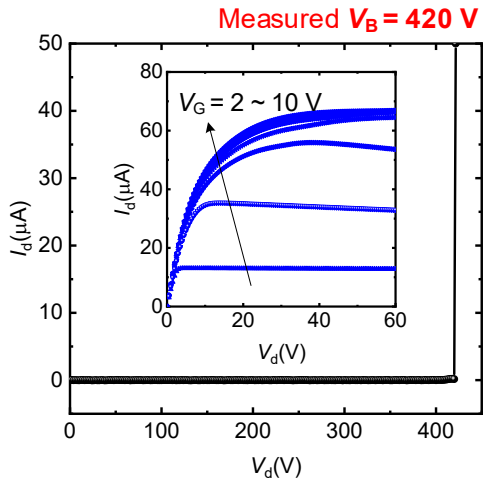


Fig. 7 Measured off-state and on-state I_d – V_d lines. The measured low $R_{on,sp}$ of 15.6 mΩ·cm^2 was observed under a V_B of 420 V, realizing a high $FOM = V_B^2 / R_{on,sp}$ of 11.3 MW/cm^2.

Fig. 8 compares the measured $R_{on,sp}$ - V_B characteristics of the CSD HOF LDMOS and other reported devices [3]-[8], [14]-[15] in a logarithmic scale. The $R_{on,sp}$ characteristic of the CSD HOF LDMOS is better than those of the recently reported devices, exhibiting a 20.8% improvement over the best-in-class $R_{on,sp}$ of the previously reported HOF device [14] while maintaining the same V_B. Furthermore, this achievement signifies a remarkable reduction of 53.3% compared with the theoretical limit achievable with the triple RESURF technology [3] at the same V_B.

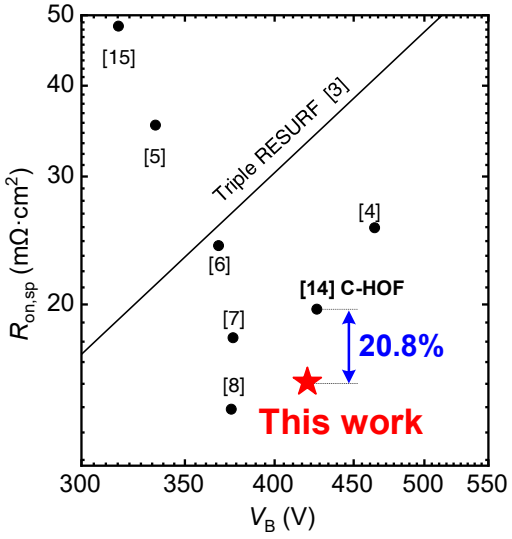


Fig. 8 $R_{on,sp}$-V_B characteristics of the CSD HOF LDMOS and reported experiments [3]-[8], [14]-[15]. The CSD HOF LDMOS realizes a $R_{on,sp}$ reduced by 20.8% when compared with the HOF LDMOS we reported in [14].

IV. CONCLUSION

This paper proposed and experimentally demonstrated the new CSD mechanism for HOF devices. Compared with the conventional constant D_N depletion mechanism in PN junction depleted devices, the HOF device achieved complete MIS-assisted depletion in the drift region, allowing for a constant surface concentration depletion. By increasing the junction and trench depths, the doping dose of the N-drift region was increased up to 8×10^{12} cm^{-2}. This resulted in a $R_{on,sp}$ of 15.6 mΩ·cm^2, measured at a V_B of 420 V. Consequently, the CSD HOF device achieved a high *FOM* of 11.3 MW/cm^2 and a remarkable 53.3% reduction compared with the theoretical limit of triple RESURF technology at the same V_B. Additionally, the CSD HOF LDMOS demonstrated a 20.8% reduction in $R_{on,sp}$ compared with the best-in-class HOF LDMOS. The CSD mechanism presented a simple and feasible approach for improving the characteristics of HOF devices.

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