SiC Power Device Processing with special regard to Ion Implantation

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Abstract

For power device fabrication distinct challenges have to be addressed. In many fields they are identical to the needs in the CMOS world. However, some features of power device technologies require customized processes. Power devices in general are facing the main demand to lower dissipation losses caused by increasing current densities at decreasing structure sizes and optimized performance of device switching behavior at the same time. Hence, advanced manufacturing processes of wafer frontside and backside as well as for engineering of bulk properties are necessary.

Whereas MOSFETs used in CMOS IC switches typically operate at a parameter range of some µA at voltages of <5V, power devices utilize up to kA currents at voltages of up to kV range. Therefore chip areas are much larger to cope with these requirements. Also, 3D device structuring is required in order to enable current flow from the chip frontside to the backside.

In general technology requirements in combination with given raw material properties drive manufacturing challenges. That in turn puts pressure on advancing both single unit process steps as well as novel integration concepts, also incorporating feed forward run to run systems and new computational capabilities towards AI. The overall equipment effectiveness in terms of availability, performance and quality is key for an economic production environment. Machine learning based concepts are developed both for the prediction of individual equipment behavior as well as to manage complexity in the overall manufacturing process line. Furthermore ML-assisted root cause analysis is developed to identify important "hidden" parameters in production equipment as well as to help revealing and understanding complex correlations.

Keywords: SiC, Ion Implantation

As of today, Silicon is still the dominant mainstream material system with IGBTs and various kinds of Power MOSFETs still being optimized for upcoming applications. Due to their decade-long history and the maturity of the involved manufacturing processes it becomes increasingly difficult to find ways to enhance their efficiency at reasonable costs. Prominent examples are the increasingly stringent requirements towards total thickness variation of low voltage power MOSFETs as well as balancing the active dopant concentration on sub-percentage level for advanced super junction concepts.

In recent years Wide Band Gap materials like SiC and GaN gained momentum and market share. Their application range partially reaches into the one of the Silicon technology portfolio. Products based on WBG technologies are currently more expensive compared to their Silicon equivalents, yet with decreasing complexity and cost of the overall system solution for the customer they achieve the break-even point for an increasing number of applications. However, advanced processes especially in terms of efficient and high-quality epitaxial layer growth, advanced doping processes by ion implantation and subsequent annealing as well as challenges in wafer thinning bare a significant amount of innovation that to a large part still has to be exploited.

Epitaxial layer growth of high quality 4H-SiC is not only an art by itself, the productivity of currently available equipment also bottlenecks fast fab extensions in the field of SiC device processing. Significant equipment competition and process innovation is driven in that field.

Thinning of SiC wafers from their original 350µm thickness to the final device target (typically around 100µm for 1200V devices) is difficult and costly. SiC belongs to the hardest material systems and can only by grinded by diamond – the economic pain is obvious.

Besides epitaxy and wafer thinning ion implantation certainly plays a key role in SiC device processing. Due the negligible amount of diffusion in SiC all dopant profiles have to be placed exactly and in its final form via implantation processes. Whereas the principal design of ion implanter equipment still stays the same as for

silicon, distinct adaptions have to be made in terms of ion source technology and end station design.

Dedicated ion sources are required to create efficient amounts of Al ion beams. Currently competition between vaporizer and sputter source designs can be observed – both with their advantages and disadvantages. Vaporizer sources are a known technology since decades for usage of Sb implantations in silicon-based technologies, however, transition times from Al operation to other implantation species like N or P are significant and therefore reducing production efficiency. Sputter sources are a relatively new technology in volume production, therefore still an active field of research in order to maximize ion source lifetimes as well as operational efficiency.

In terms of end station adaptions especially the capability of processing hot implants is desperately needed especially for high dose contact applications. In-situ annealing of crystal damage prevents 4H-SiC from being transformed into other polymorph types of SiC and therefore harming device operation. 500°C are established as industry standard for hot implantation, however, research suggests that even more elevated temperatures might further benefit specific applications.
Since SiC is a quite dense material (3,21g/cm^{-3}) with hardly any diffusion of doping elements at practicable temperatures, dopant profiles have to be placed exactly to its final position by ion implantation. This implies that implantation energies are quite high for deep layers. One possible way of overcoming this obstacle is the usage of channeling implantation for the creation of deep extended dopant profiles. Due to the low probability of large energy transfer collisions ion stopping is dominated by the electronic drag, allowing for an extended tail of the implantation profile. That can result in plateau-like profiles instead of gaussian peaks and results in less surface near damage creation. Depending on the combination of crystal channel used as well as implantation parameters like element, implant energy and dose along with substrate temperature critical angles will differ significantly. Independently of the exact value, enhanced effort for tool and wafer material control will be required.

Overall, basic implantation knowledge for SiC application exists, however, there is significant room for further innovation as well as process optimization in the years to come.

As known from the silicon world also implantation in SiC have to be followed by thermal anneals in order to remove implantation damage and to activate dopants. In 4H-SiC temperatures in the range of 1600 – 1900°C are required, giving raise to the development of dedicated furnace systems. From a process point of view the usage of graphitic carbon capping layers is advised to stabilize the wafer surface and to avoid step-bunching.
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