Understanding Power Semiconductor Technology Platforms for Building a Viable and Sustainable Product Roadmap

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Abstract

In this paper, key technical pillars for a power device technology and product development roadmap are discussed. First, the main performance requirements of power semiconductors are outlined to establish modern development trends that can lead to a viable power device development roadmap. The basic principles of power semiconductor "Technology Platforms" will be presented in relation to well- defined "Device Sections". In addition, device classification and technology complexity aspects will be reviewed as important technical pillars in the roadmap building process. Understanding the above can help map out future development tasks targeting next generation products with improved performance over cost ratios.

Keywords: Power Electronics, Power Semiconductors, Technology Platforms.

INTRODUCTION

Power electronics applications are the foundation for driving the electrification mega-trend by providing efficient, sustainable, and reliable energy for the urban, industrial and transportation sectors. At the heart of this trend lies the power semiconductor device [1] which is responsible for modulating and controlling the electrical energy flow between the energy source and the application load. Therefore, power semiconductors are today present in all parts of the electrical energy chain, starting with low power applications such as computers and mobile phone chargers up to very high-power applications such as for grid systems (see Figure 1).

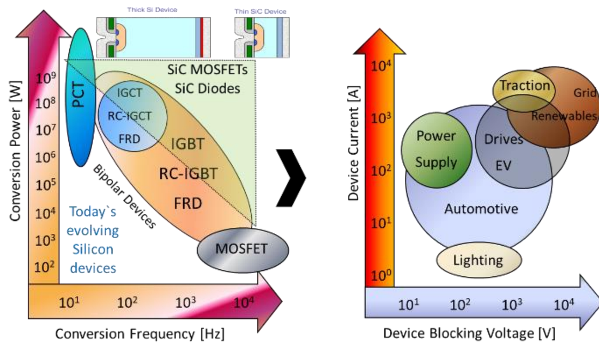

Fig. 1. Power semiconductors and applications.

For decades, Silicon based power semiconductors have dominated the power electronics market. They have maintained pole position through tremendous advancements in materials, process fabrication and the design and architecture of different device concepts. The prominent market position of Silicon power devices will be maintained due to the mature technologies and the continuous advancements in electrical characteristics, ratings, and reliability [2]. However, power devices based on wide bandgap materials such as Silicon Carbide (SiC) and Gallium Nitride (GaN) are currently employed in many applications due to their superior properties and potentially near ideal electrical performance. Such attributes are welcomed today by system designers as they enable higher power densities with increased operating efficiencies. For example, recent design and process breakthroughs resulted in a wide range of SiC MOSFET product platforms. This led to substantial growth in market adoption for key applications such as in automotive drivetrains.

The continuous drive for improved performance for both Silicon and SiC based power devices will be based on developing more advanced technologies. In this paper, the basic principles of power semiconductor "Technology Platforms" [3] will be presented and in relation to the main power semiconductor component sections at both chip and package levels. To build a viable and sustainable technology and product roadmap aligned with an established industrial business strategy, understanding some key roadmap technical pillars is important as shown in Figure 2 and discussed in this paper.

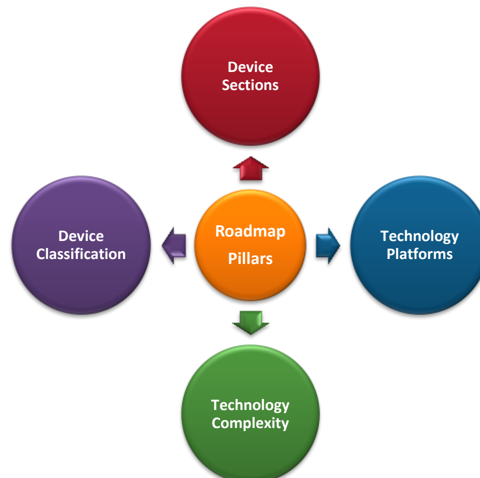

Fig. 2. Power semiconductors roadmap technical pillars.

These four technical pillars can aid research and development teams in industry and academia to devise future power device development projects targeting new technologies and products with improved overall performance over cost ratios. It can also assist with recent development trends addressing different application requirements with respect to device optimisation and customization (see Figure 3). Generally, the paper will focus on vertical devices targeting high power levels compared to lateral devices in the low power segment.

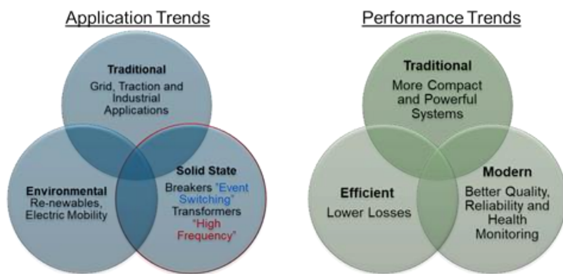

Fig. 3. Power electronics application and performance trends.

As an example, it is worth noting that more applications are emerging (e.g., renewables, EV and solid-state breakers or transformers) with different performance requirements. Advanced solid-state solutions requiring power electronics platforms, such as DC breakers, necessitate the power semiconductor to be optimized for so-called "Event Switching" operational mode as opposed to typical switching patterns in inverters. On the other end of the scale, HV devices need to be optimized for higher operating frequencies (>5kHz) required in resonance topologies employed in DC/DC conversion.

DEVICE REQUIREMENTS AND DEVELOPMENT

There exists a long list of electrical and reliability performance requirements for power semiconductor components [4]. However, the primary considerations can be divided into three categories as shown in Figure 4 and listed below:

1. **Power:** power density capability (electrical losses and thermal management)
2. **Control:** controllable switching (gate response, gate charge, turn-off softness, and EMI)
3. **Margins:** safe-operating-area, fault-handling capability, and reliability

Devices targeting high power densities aim for low conduction and switching losses, low thermal resistance, and high operating junction temperature. For the second category, there needs to be controllable turn-on, low gate charge, soft turn-off transients with low over-shoot voltages and minimal EMI levels. The last category, with regards to margins, includes a wide Safe-Operating-Area (SOA) associated with the turn-off current capability, fault-withstand capability such as short-circuit for IGBTs and MOSFETs or Surge Current for IGCTs and Diodes. In addition, the device (not the package) reliability requirements are associated with current and voltage sharing for devices arranged in parallel or series; stable conduction and stable blocking with no short to long term parameter drift or degradation and very low failure rates (FITs) due to cosmic rays.

When considering all the above issues, design engineers must also evaluate the attributes of the package. There is a continuous trend towards more compact and powerful packages, which combine a higher device packaging density with optimized chip and electrical layout designs for improved thermal properties and low parasitic elements. Improved joining technologies are crucial to achieve low thermal resistance and increased temperature and power cycling capabilities. The package role for device protection from harsh environmental conditions such as humidity is also a critical subject today.

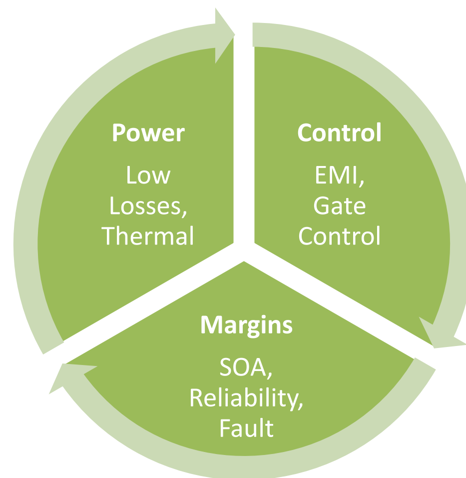

Fig. 4. Power semiconductor component requirements.

For power devices in general [5], the main technology drivers for providing higher power are always approached on two principal levels as illustrated in Figure 5 and listed below:

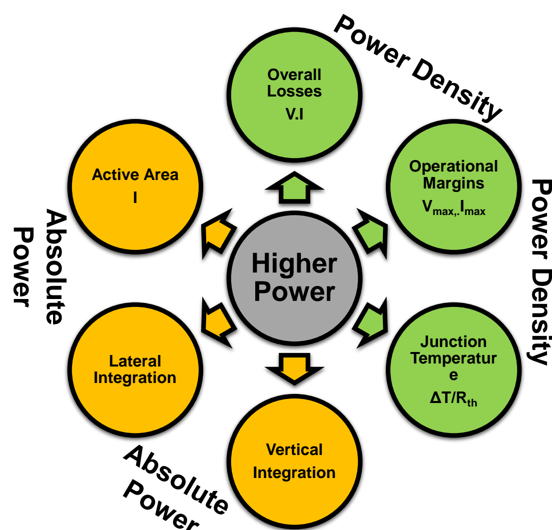

Fig. 5. Power Device technology drivers for higher power.

POWER DEVICE COMPONENT SECTIONS

To better understand the power semiconductor component, the chip and package structures can be each divided into different and distinctive sections as shown in Figure 6. These sections are defined by having clear functional targets and can be interchangeable with other different section concepts. Hence, a good understanding of each section building blocks, evolution and development trends is necessary for creating a viable power semiconductor product roadmap. In the following, we will outline the chip and package sections separately.

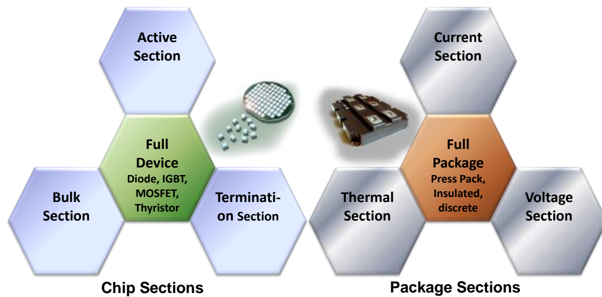

Fig. 6. Power semiconductor component sections.

Chip Sections

At chip level, the structure can be divided into three sections; namely the Bulk Section, the Termination Section, and the Active Section as shown in Figure 7 below with more detail:

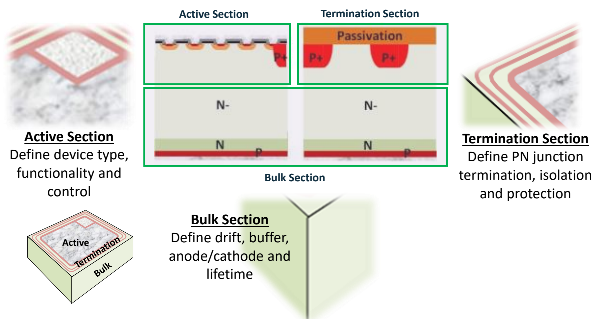

Fig. 7. Power semiconductor chip sections (e.g., IGBT).

The Bulk Section: is key for defining the device blocking capability while strongly affecting the device overall losses and operational mode (e.g., Unipolar or Bipolar). The bulk region also defines the bipolar gain levels for bipolar switching devices such as IGBTs and IGCTs which plays a critical role for the device performance under different operating conditions. The Bulk Section consists mainly of

- Lightly doped N- drift region which is the main design feature that distinguishes power devices from their low power counterparts. The N-drift region parameters (doping and thickness) mainly define the device blocking capability and voltage class. Other advanced bulk designs include lowly doped N-type and P-type pillars for providing super junction device concepts such as those in high voltage MOSFETs.
- Higher doped N-type buffer region is required for Punch-Through (PT) or Field-Stop (FS) type devices. When omitting the N-buffer region, a Non-Punch-Through (NPT) structure is obtained. Reverse blocking NPT type devices are also feasible as mentioned in the following sections.
- The bulk also incorporates higher doped P collector / anode regions (for IGBT and IGCT) or N cathode / drain regions (for Diode and MOSFET). For example, the difference between the Unipolar MOSFET and Bipolar IGBT is in principle a change from a highly doped N-type Drain to P-type Collector which enables bipolar mode behaviour of the IGBT.
- Shorted N-type regions (collector shorts) to realise a Reverse Conducting RC-IGBT or other special designs.
- Lifetime control in the bulk plays also an important role for excess carrier profiling (plasma engineering) for bipolar devices.
- Metallization layers for low ohmic contact and packaging.

The Termination Section: is positioned on the edge of the device for shaping and controlling the electric field distribution “in the semiconductor” AND “at the surface” to obtain maximum voltage withstand capability with low leakage currents and stable blocking especially at high temperatures. The Termination Section consists of

- PN Junction Termination (JT) which can be based on different design concepts. For chips/die (IGBT, MOSFET), planar designs are employed including Guard Rings (GR) with or without Field Plates or Junction Termination Extension (JTE) (e.g., Variable Lateral Doping (VLD)). For larger circular wafer devices (IGCT, Thyristor, Diode) employed in hermetic press-packs, positive or negative angle edge bevelling or mesa type designs are ideal.
- Termination Passivation which incorporates several different passivation and protection layers depending on the junction termination design requirements. In principle, there are three levels of passivation layers. The first is the layer that is in direct contact to the semiconductor materials and therefore has a strong influence on the surface charge levels and electric field distribution (can be a semi-conducting layer). The second is a thin protection layer against flashovers, mechanical damage, and humidity. The third top layer is relatively thick and consists of an organic material such as polyimide to provide further protection.
- For reverse blocking or bidirectional devices, the termination section is present on both sides of a vertical device.

The Active Section: defines the device type, functionality, and controllability. Therefore, it strongly

impacts the device over-all power ratings and performance. The Bipolar Diode, Schottky Diode, Thyristor, GTO/IGCT, Bipolar Transistor, MOSFET/IGBT are all different device concepts which are based on different active section design concepts. In general, the active section consists of

- The main active area which is responsible for the current conduction, voltage blocking and switching modes of operation. For example, the active area of MOSFETs and IGBTs consists of emitter MOS cells based on planar or trench gate structures having different layouts such as cellular or linear type designs.
- The Gate control terminal and distribution for switching devices. This design differs for gate current-controlled devices such as Thyristor or Transistors than those for voltage-controlled devices such as MOSFETs and IGBTs.
- The active to termination transition region (i.e., edge of active section). This design is key to maintain robust switching along with high voltage blocking capability especially for diode designs.
- Local lifetime control in the active section plays an important role for excess carrier profiling (plasma engineering) such as for Fast Recovery Diodes.
- Frontside metallization layers for low ohmic contact and packaging.
- For bidirectional type devices, the active section is present on both sides of a vertical device.

Package Sections

Similar section definitions can be applied to the power semiconductor package as shown in Figure 8. Without going into a detailed description, the package sections can be listed as follows:

The Thermal Section: is mainly related to the thermal path of the power semiconductor package. This includes the semiconductor chip, a substrate which can consist of an insulating layer (e.g., Direct Copper Bonding DCB substrate), a Copper heat spreading layer or base-plate if present. The joining layers of the above elements such as the soldering films are also key to the thermal characteristics of the component. Optimum layout designs and materials are required to achieve the minimum thermal resistance and thermal stability during device operation.

The Voltage Section: constitute the package encapsulation materials which is key to the module mechanical robustness and to chip protection from external harsh conditions. The filling materials can range from hermetic, Silicone Gel or Transfer molding. The latter is very common for discrete package as well as modern modules employed in automotive or consumer type applications. The package substrates, terminals, frame, and cover are also important when considering the design and related dimensions to withstand and insulate very high voltages (e.g., creepage distances).

The Current Section: relates to the main current flow in the package. For insulated type modules (i.e., chip needs to be insulated from cooling system), the current flows laterally while for press-pack modules (cooling plate is electrically active), the current flow is vertical. The current path includes the chip, wire-bonds, substrate, main terminals, and base-plate (for press-pack). The gate distribution and layout design are also part of the current section and an optimum design is required for uniform gate signal propagation and switching behaviour.

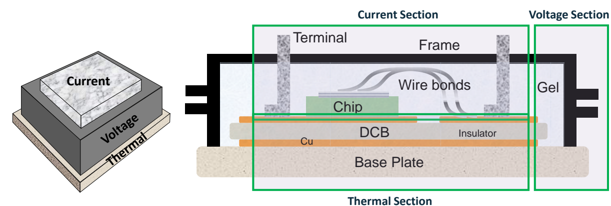

Fig. 8. Power semiconductor package sections.

The previously mentioned component (chip and package) sections can only be realised by developing the associated so-called “Technology Platforms” which will be described in the following paragraphs. It is important to outline first that the main and final target for the power semiconductor device technology development is to establish a range of product platforms or product portfolio with well-defined performance specifications and targeted applications.

POWER DEVICE TECHNOLOGY PLATFORMS

In industrial terms, “Product Platforms” are a set of products which utilizes qualified “Technology Platforms” for providing a wide range of ratings, configurations, and performance specifications. A given product platform can also constitute variants with minor modifications to achieve a range of optimised performance levels for specific applications. The “Technology Platforms” shown in Figure 9 are the main manufacturing pillars for realizing different device sections which the associated product platforms are based on. The technology platforms can be expressed as three distinctive categories or groups; namely the Process Platforms, the Design Platforms, and the Integration Platforms as follows:

- **Process Platforms:** a single or a sequence of processes with the target to realize an independent device building block and functionality for a given device section. A process platform can be as simple as depositing multilayer metals for a backside contact with no photolithography masks required, to more complex multi-mask processes to establish for example an IGBT MOS cell.

- **Design Platforms:** a single or set of design rules or guidelines for a given process platform (within the process capability) to modify or adjust a targeted performance. It also includes design layouts and starting material specification which are associated

with a given device section. Hence, adjusting mask dimensions, implant parameters, diffusion rates, layer thicknesses … etc, are all considered to be design platforms. When the design platforms are finalised, the targeted performance specification is normally reached.

- **Integration Platforms:** a set of process sequences and design features that when combined, the final device and functionalities are realised. The integration platforms can be represented as an overall process router and device structure. In addition, to develop, upgrade or deviate from an existing finalised device structure, new sets of process and design platforms need to be developed and inserted into the original process flow in the form of a single process step or set of processes (sub-router) to provide a new integration platform.

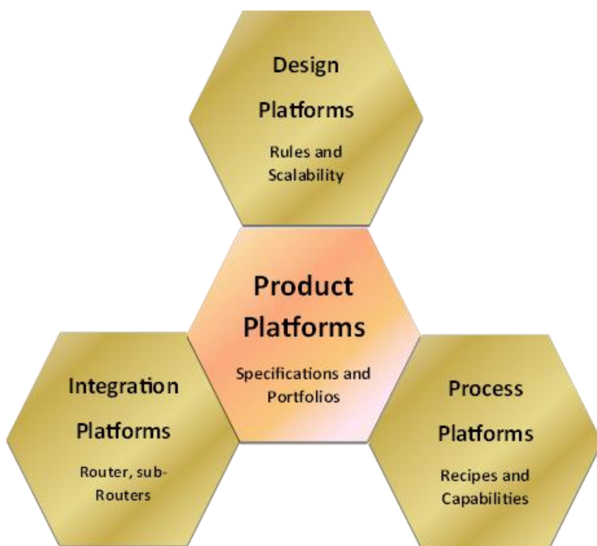

Fig. 9. Technology Platforms leading to Product Platforms.

In general terms, research and development of power devices runs through a technology development phase which requires successful technology verification followed by a product development phase which requires product qualification. Preferably, both process and integration platforms should be established and verified during technology development while some adjustments of the design platforms can still be performed during product development.

DEVICE CLASSIFICATION AND TECHNOLOGY COMPLEXITY

Device classification and customisation trends are shown in Figure 10. Many device/package footprint and performance standards have been developed to satisfy the demand of the power electronics market with respect to high level performance and multi-sourcing of components. However, customisation trends have been developed to further optimise the system performance by providing more enhanced products in terms of applicability and performance. This is justified since the power semiconductor is a key component in the power electronics system and it`s performance defines to a large degree the performance specification and competitiveness of the system. The customisation can range from simple variations to fine-tune the device losses (e.g., adjust the device technology point in terms of static versus dynamic losses), to providing alternative solutions to standard offerings (e.g., IGCT or RC-IGBT) which require more development efforts or to provide completely new and unique solutions for a specific application (e.g., press pack IGBT modules for HVDC). Some of the customised solutions can become popular due to their high-performance levels and could eventually establish themselves as a standard when adopted by different manufacturers while considering that no Intellectual Property issues are present. As mentioned previously, the high growth and expansion of power electronics applications with high performance expectations is a strong driving factor for more customisation development trends of power semiconductors devices.

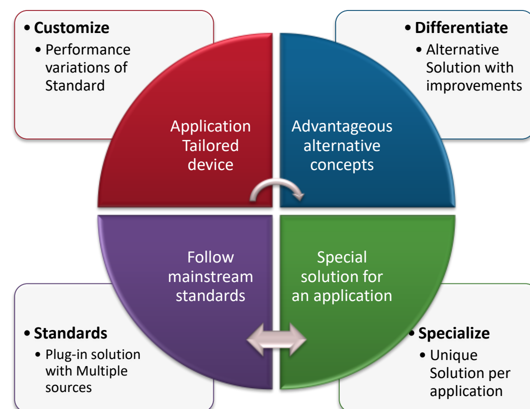

Fig. 10. Power device classification and customization trends.

Addressing technology development trends targeting higher power levels as described previously and the customisation trends listed above will require a detailed assessment of the technology complexity faced by the development teams. Figure 11 below illustrates the different complexity levels which range from developing completely new technology platforms to simple variant of existing platforms.

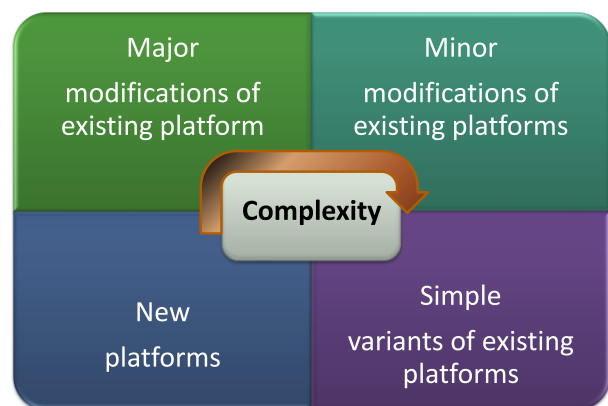

Fig. 11. Complexity levels for power device technologies.

Typically, new platforms or major modifications to existing platforms might require new process and integration platforms while minor to simple modifications can be achieved with changes to the design platforms only. In addition to the technical pillars, the other two important roadmap enablers in terms of financial and resource (skills and equipment) pillars can be planned accordingly based on the above principles.

DISCUSSION

To understand better the previous discussion, we present an example for the development of a reverse conducting RC-IGBT which combines both the switch and diode mode functionalities in a single chip as shown in Figure 12. Based on the development trends shown in Figure 5, this technology can lead to the increase of the absolute power levels by replacing the diode space with RC-IGBT chips. A reduction in the package footprint while keeping the same current rating is also possible. However, the target performance specification must ensure that other power density related factors such as losses, SOA / Reliability margins and high operating temperatures remain unaffected or preferably improved when possible. The RC-IGBT technology development is normally based on established IGBT technology platforms while carrying out the required modifications to enable reverse conducting functionality. This task becomes more challenging if the targeted RC-IGBT aims to fully replace the standard two-chip (i.e., IGBT and fast diode) component in mainstream hard switching applications. In otherwards, the RC-IGBT can be classed as a differentiating technology to mainstream IGBTs. This has been the case in recent years with RC-IGBTs employed in HVDC (e.g., the BIGT [6]) and automotive applications.

The RC-IGBT faces many development challenges to ensure that (a) no snap-back characteristics are present during on-state, (b) optimised trade-off between diode and switch mode losses, (c) good current uniformity and high SOA and (d) controlled switching behaviour.

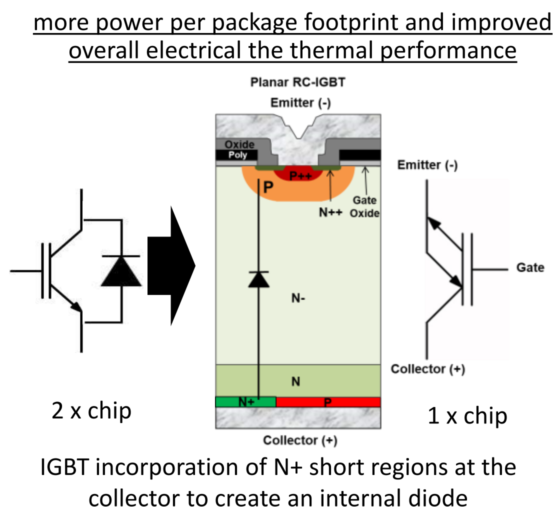

Fig. 12. From IGBT / Diode to RC-IGBT.

Overall, the RC-IGBT technology requires major modifications to an existing IGBT technology platform. The main IGBT sections where modifications are necessary are the bulk and active sections. The bulk section will require collector N+ type short regions to provide an internal diode structure while lifetime control might also be needed for plasma engineering to enable fast reverse recovery switching in diode mode operation. Hence, new process and integration platforms are developed while at the same time some of the original IGBT design platforms are adjusted to achieve the required RC-IGBT performance specification. Furthermore, the RC-IGBT could potentially require package improvements in terms of new footprint and layout designs to ensure that higher electrical and thermal performance levels are obtained due to the new integrated solution.

CONCLUSIONS

The paper introduced the growing power electronics market in relation to both modern application and performance trends. The power device requirements per application determines future development trends with focus on increased power levels, margins, and controllability. To help establish a viable technology and product roadmap, key “roadmap technical pillars” have been identified and discussed in this paper including the principles of “Technology Platforms” when related to different “Device Sections”.

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