Impact of Super Junction Concepts in Silicon and Wide Bandgap Semiconductors

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The first two-dimensional varactor, which closely resembles the modern day super junction concept, was proposed by Shirota and Kaneda in 1978, as shown in Fig 1, to enable spread of depletion regions into a multi-layer n/p layer composite structure so that the range of capacitance-voltage characteristics could be widened in comparison to conventional varactor structures [1]. The first reported charge balance structure to enhance the breakdown voltage in a lateral device is the REduced SURface Field (RESURF) concept, introduced by Apple and Vaes in 1979 [2]. This concept alone widened the scope and application of power ICs into a multi-billion market today. The first power device structure employing composite n/p layer was proposed by Coe in 1982 [3] and the first super-junction device making use of such layers in a vertical device was reported by Infineon in 1990s [4]. Ever since, the super-junction concept has revolutionised the silicon power MOSFET market up to 900 V. This is simply because, the super-junction concept enabled silicon power MOSFETs to achieve area specific on-state resistance for a given breakdown voltage beyond the 1-D material limits of Silicon. As shown in Fig 2, doing so enabled achievements of linear increase in on-state resistance with breakdown voltage, when historically, the onstate resistance (Rds(on)) relationship as a function of breakdown voltage is typically $BV^{2.5}$ in conventional MOSFETs. Not only that, but the super-junction concept also led to better area effectiveness of the devices to fit into smaller packages as well as significant reduction of switching losses. The area-specific on-state resistances of the present-day SJ- power MOSFETs are only limited by their capacitive effects.

The super-junction concept is highly suited to MOS-Bipolar devices such as the IGBT [5] and/or the Clustered IGBT [6], as shown in Fig 3 and 4. In these devices, the pillars enable (a) charge balance (b) a path for extraction of holes in the turn-off conditions and keep the drift regions as thin as possible. In an IGBT, employing a p-pillar is a complex design challenge. In the trench Clustered IGBTs, where these p-pillars are only connected to the floating p well, an effective PMOS can be formed to extract holes in a very effective way, which can lead to a very significant reduction in turn-off energy losses from 7.2 mJ to 2.5 mJ, without affecting on-state losses, as shown in Fig 5 [7]. As TCIGBTs are devoid of limitations posed by the dynamic avalanche, our studies showed that such SJ-TCIGBTs can be operated at 500 A/cm^2 with significantly low switching losses and can operate beyond the 1-D material limits of SiC at 3 kV or so, as shown in Fig 6.

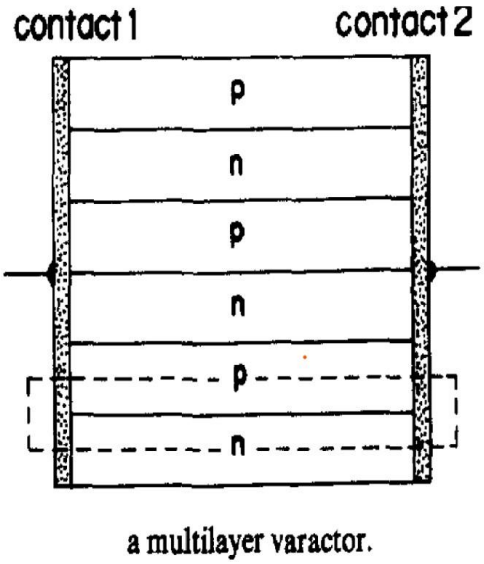

Fig 1. The simplified view of the Varactor [1].

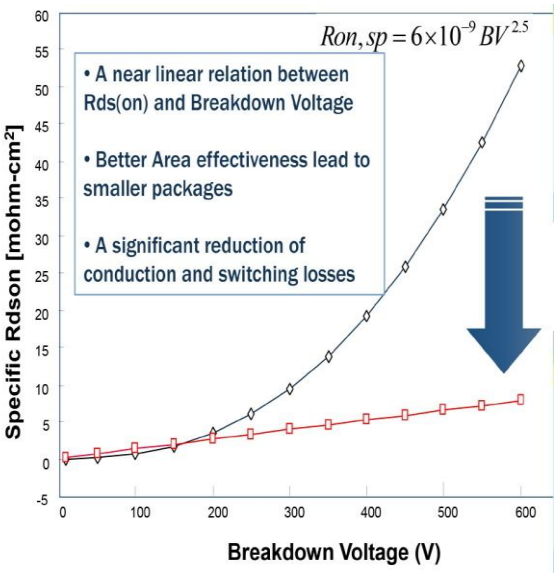

Fig 2. The influence of Super-junction on the Ron(sp) as a function of breakdown voltage.

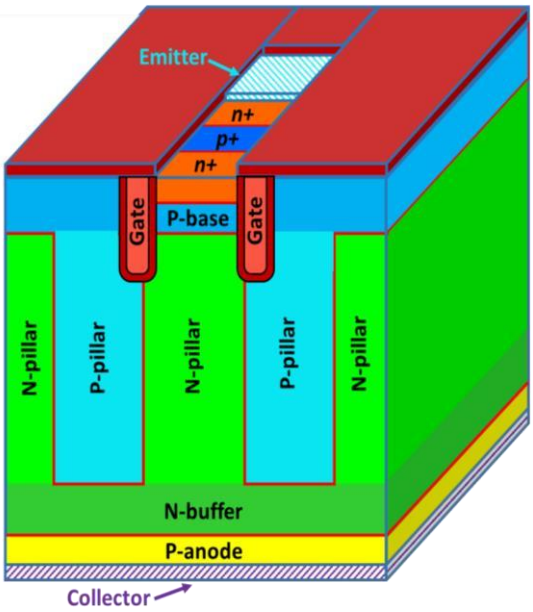

Fig 3: A Simplified 3-D cross-section of a SJ-IGBT

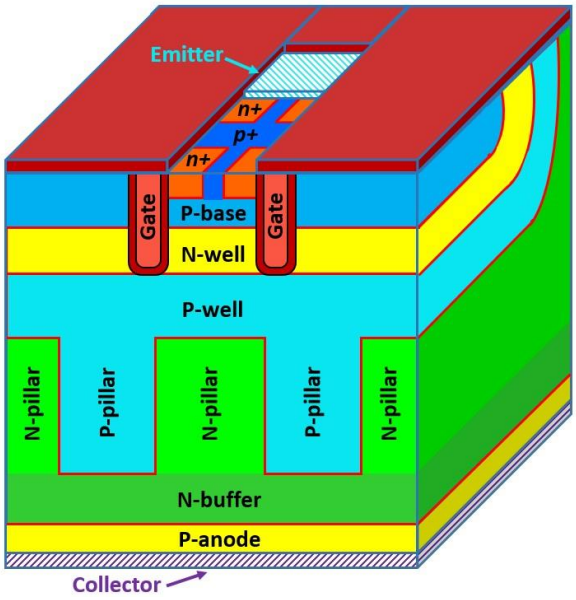

Fig 4: A Simplified 3-D cross-section of a SJ-TCIGBT

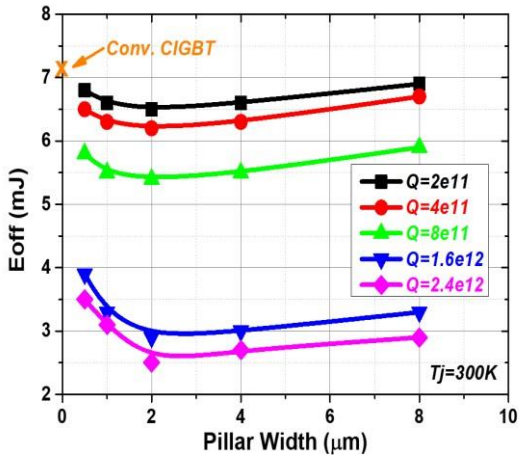

Fig 5: Predicted reduction in Eoff losses as a function of SJ charge and p pillar width in a SJ-TCIGBT [7].

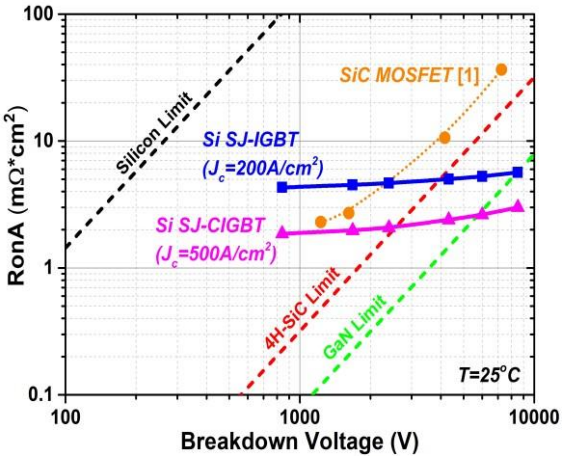

Fig 6: Predicted performance improvements of the SJTCIGBT and SJ-TIGBT [7].

The super-junction concept can be effectively used in SiC to reduce the epitaxial layer thickness as well as approach the 1-D material limits of 4H-SiC [8]. It is well known that the cost of SiC MOSFETs are considerably higher than that of Silicon counterparts. As most of the costs are in the bulk and epitaxy growth of SiC materials, it is difficult to see how these can be reduced to the levels of Silicon devices in a foreseeable future. The application of SJ concepts in SiC are like that of Silicon technology but need more advanced manufacturing facilities. Jury is out, therefore, on the performance over cost advantages of SiC SJ devices. Moreover, the increase in background doping concentrations due to the employment of SJ pillars can lead to higher switching losses in WBG technologies in SiC and conventional vertical GaN technologies. However, such is not the case with lateral devices made of Gallium Nitride, which use polarisation properties to achieve super-junction. Polarisation Junction based concepts were first hypothesised in 2006 [9] and first devices were reported in 2011 [10].

Conventional lateral GaN power devices are primarily based on positive polarisation, which results in high density 2-Dimensional Electron Gas at the AlGaN/GaN heterostructures. These devices make use of field plates to achieve high blocking voltages. As shown in Fig 7, Polarisation Super Junction based lateral GaN devices make use of double heterostructures of GaN/AlGaN/GaN structures to avail of charge balance of high density 2-Dimensional hole gas to co-exist with high density of 2-Dimensional Electron Gas and achieve charge balance. In such devices, the charges are not created by doping and are optimised by growth. Therefore, these charges are not largely dependent on temperature, which makes these GaN based Polarization Super Junction (PSJ) technologies highly suited for cryogenic operations as well as high temperature operations.

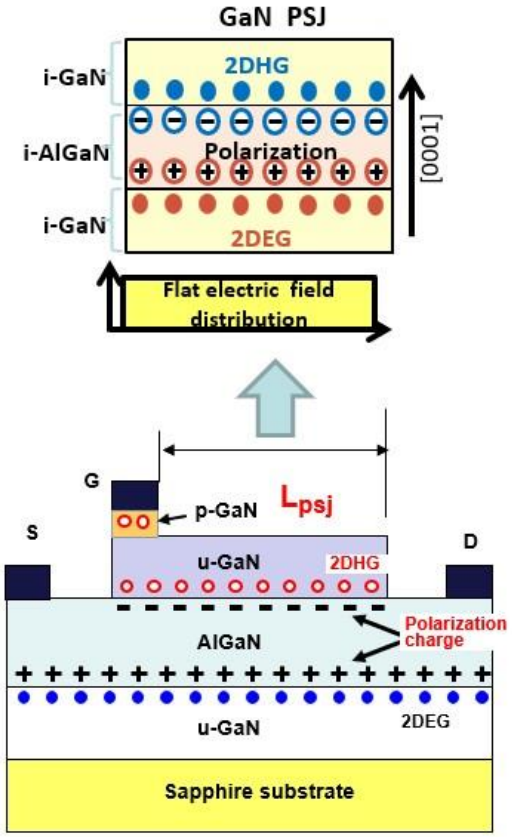

Fig 7: Details of the PSJ concept and the conceptual design of a simplified PSJ-HEMT

Material	E_{cr} (V/cm)	Q_{opt} (/cm^2)	Drift (µm) for 1.2 kV
Silicon	3e5	1e12	120
GaN	3e6	1e13	15

- Charge balance by **GROWTH**.
- Charge balance independent of temperature.

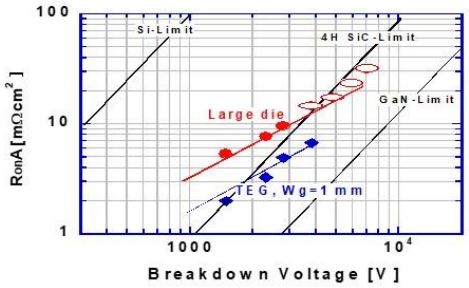

Fig 8: Key benefits of GaN technology over Silicon and the measured performance of PSJ HEMTs [13].

There are no field plates employed in the PSJ devices, which makes the processing much cheaper, and the blocking voltages can be directly scaled as a function of the charged balanced drift region (known as Lpsj) [11]. On Sapphire substrates, blocking voltages as high as 10 kV has been reported [12], while on Silicon substrates, the blocking voltage is limited by the vertical breakdown of the GaN/Silicon region. From a perspective of 1-D material limits, these devices perform close to 4H-SiC limits, as shown in Fig 8, [13] and large area devices are limited by the constraints posed by the geometrical limits posed by semiconductor processing.

Most recent results of the 1.2 kV rated large area diodes and HEMTs are highly encouraging. For example, the hybrid Schottky-Junction Diode shows excellent surge current capability [14] and no parasitic turn-on of the junction diode at least up to 6 to 8 times the rated current. 1.2 kV PSJ HEMTs show excellent static electrical characteristics as well as dV/dt capability as low as 1 kV/us, as shown in Fig 9 and with very low energy losses shown in Fig 10, which makes these devices suited for motor drive applications [15]. The bidirectional switches are in development [16] and promise to be ideal for various emerging current source inverter applications. As shown in Fig 11, PSJ technology is a platform technology on which power diodes, transistors, or bidirectional switches as well as PMOS and NMOS devices can be made simultaneously [17]. It is important to note that complementary MOS devices are possible and can be a highly suited platform for Power Management IC operating in voltages above 1.2 kV.

It is also possible to consider vertical polarization based super-junctions at nano-scale level [18]. A reduction of almost two orders of magnitude in R_{ON}.A can be achieved using VI-PSJ structures for breakdown voltage of 1kV, which could extend to three orders of magnitude improvement for 10kV devices, in comparison to conventional SiC devices, can be possible, as shown in Fig 12. Thus, the predicted performances of such devices are very attractive, but these will also require highly complex processing.

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