Surge current test of SiC MOSFET with planar Assembling and Joining Technology

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Abstract

This paper introduces a novel packaging with planar Assembling and Joining Technology (AJT). The 1200V SiC MOSFET body diode with the new AJT has been investigated under surge current conditions. The test result of the planar AJT is compared with a standard TO-247-4 discrete component. Additionally, thermal impedance of both packages is measured and compared.

Keywords: surge current test, novel packaging, SiC MOSFET.

Motivation

An active front end rectifier replaces diodes with IGBTs (or SiC MOSFETs) to convert the incoming AC grid voltage into controlled DC voltage. It has low current harmonics, enables power factor correction and bidirectional power flow.

In an industrial active front end application, inrush current may lead to a high surge current through the freewheeling diodes (or body diodes) that is far beyond the nominal rated current. The resulting peak junction temperature can exceed the maximum specified temperature by far, which causes a certain degradation of the diode at each surge event.

SiC MOSFET body diodes suffer from the surge current event much more than the Si diodes. Because the body diode has a higher forward voltage drop and a smaller chip area, which results in a higher power density. The comparison between a SiC body diode and a Si diode can be found in [1].

The surge current capability of the body diode should be specified according to application and improved.

This paper investigates the surge current capability of a novel packaging with planar Assembling and Joining Technology (AJT). The test results are compared with the standard discrete package TO-247-4.

Approach

The investigated 1200V SiC MOSFET has a chip area of $0.25cm^2$, and a specific R_{DSon} of 4.25 $m\Omega cm^2$ at 25°C. The same chip type is assembled into three different packages for comparison. The I-V characteristic is measured at different V_{GS}, shown in Fig. *1*.

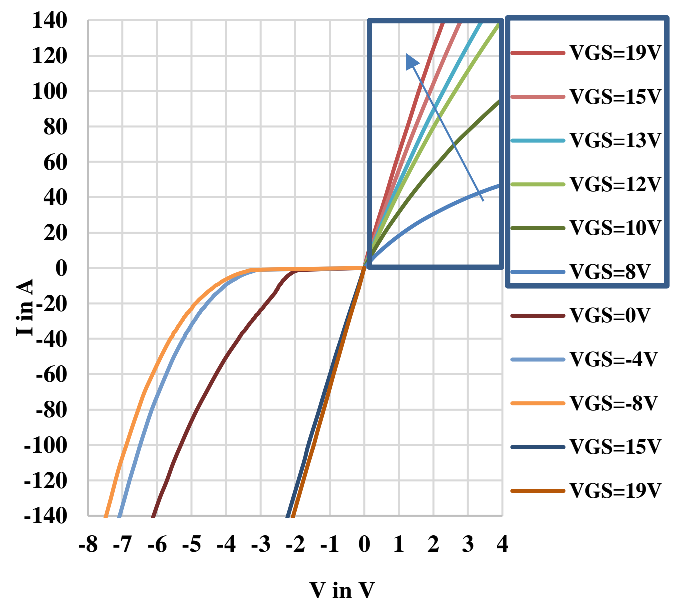

Fig. 1: I-V characteristic of 1.2kV SiC MOSFET at T_a=30°C.

The cross-section view of the three SiC MOSFET packaging types are shown in Fig. 2.

- Type 1 planar AJT with DBC:
  The SiC MOSFET is sintered on direct bonded copper (DBC), and the full source and gate area are soldered to a redistribution layer. The isolation material has a low thermal conductivity, less than 0.5W/(m·K).

- Type 2 planar AJT with Cu:
  Four chips are sintered on a thick Cu lead frame (2mm), and the full source and gate area are soldered to a redistribution layer.

- Type 3: TO247-4: (reference sample)
  One chip is soldered on 2 mm Cu lead frame, and bond wires connects the chip top side.

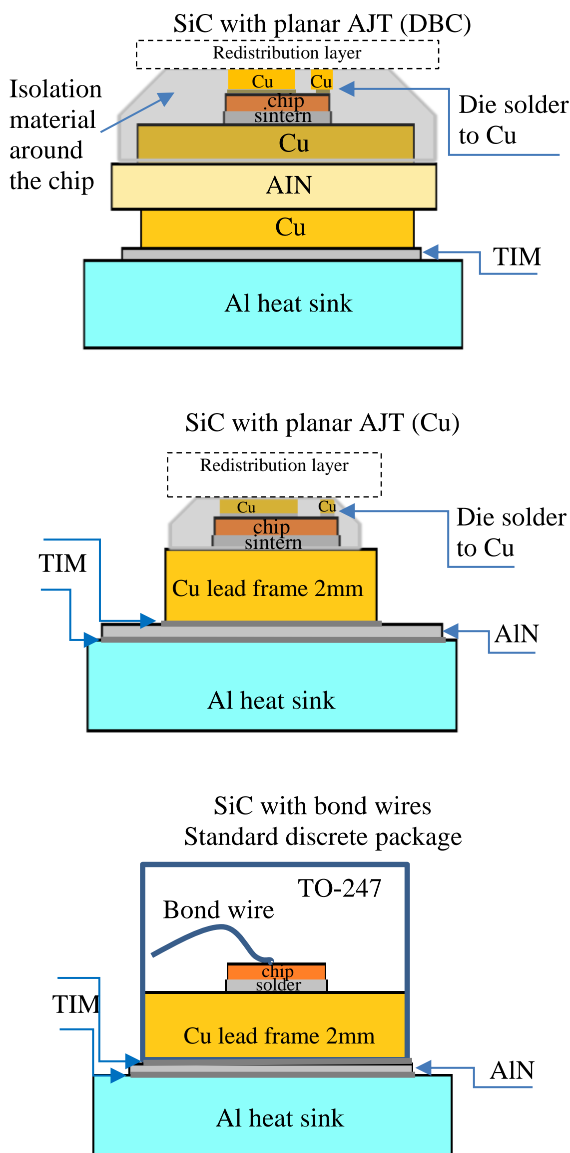

Fig. 2: Three types of SiC MOSFET packaging: planar AJT and standard discrete package TO-247.

There are 2 up to 4 samples of each package type in the surge current test. The half-sine waves load on the body diodes is applied for 10ms at room temperature, which is corresponding to 50Hz grid frequency. The surge current capability of SiC MOSFET at different load time can be found in [2].

The current stress pulse is repeated 20 times at the same current level, with 30 s cooling down time in between. Each sample is screwed on a heat sink with thin thermal interface material (thermal grease) in between to ensure better cooling under surge current conditions.

Three types of packages are compared with shortened gate and source during the surge current event. The standard package TO-247 is also tested with a negative gate-source voltage (V_{GS}=-8V), which is compared to the result under a V_{GS}=0V condition.

$$\int_0^{tp} I^2(t) \cdot dt = \frac{1}{2} \times IFSM^2 \cdot tp \qquad \text{Eq. 1}$$

The current waveform is like a half-sine pulse, the current integral I^2t is calculated with the current amplitude I_{FSM} in Eq. 1, which is a measure for the thermal load.

Each series of surge current test pulses starts from rated current with 20A increase per step. Three failure criteria parameters are monitored after each surge current event:

- the leakage current (I_{DSS}) of the SiC MOSFET at 1200V blocking voltage.
- the gate leakage current (I_{GSS}) at V_{GS}=15V.
- the forward voltage-drop (V_F) during the load of surge current.

The maximum current before chip degradation (last pass) is the surge peak forward current (I_{FSM}).

Surge Current Test Results

Two pairs of measured waveforms from planar AJT (DBC) are shown in Fig. 3 as an example. The peak current of the half sine current wave is increasing, and the corresponding voltage also increases in a similar wave form.

The planar AJT with DBC packaging (single chip) lost the blocking capability at around 400 A, which is about three times the rated current. The rated current is given in data sheet at 25°C.

Neither distortion is observed in the forward voltage wave form, nor is there an increase of gate leakage current.

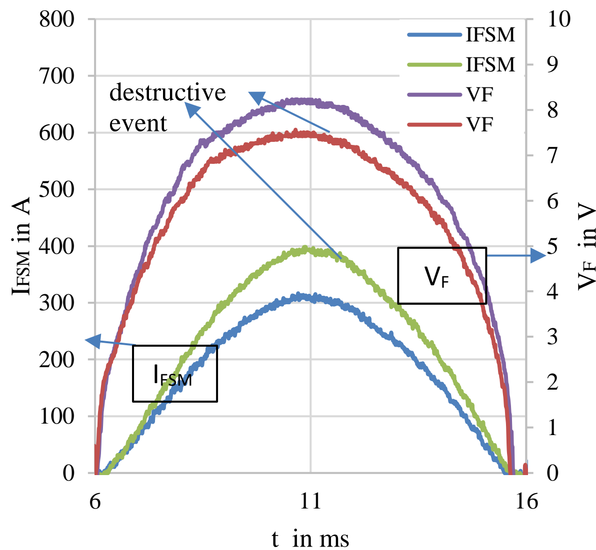

Fig. 3 Measured half sine wave form at room temperature at sample one with planar AJT (DBC).

The last I_{FSM} value before the first signs of the degradation of the packaging under test is shown in **Error! Not a valid bookmark self-reference.**. The lowest I_{FSM} value of each group is used for comparison and further I^2t calculation.

Table 1: I_{FSM} measurement results at T_a=25°C, V_{GS}=0V.

Packaging type	Chips per package	I_{FSM} before defect in A	I^2t in kA^2s (From lowest I_{FSM})
Planar AJT (DBC)	one chip	400 372 410 380	0.69
	four chips	1733 1534 1704 1532	11.74
Planar AJT (Cu)	four chips	1945 1730	14.96
TO-247-4	one chip	340 340 340 340	0.58

All planar AJT samples show the same failure mode: increase of leakage current I_{DSS} at 1200V blocking voltage, which increases from a nA range to a mA range. No distortion on forward voltage or I_{GSS} increase is observed after surge current events.

The I_{FSM} value of the planar AJT (DBC) packaging with four parallel chips (1532A) is around four times the I_{FSM} value of a single chip (372A). A symmetric layout design leads to a symmetric current distribution among parallel chips.

The I_{FSM} of the planar AJT with Cu (1730A) is approx. 13% higher than the planar AJT with DBC (1532A), because the heat distributes/spreads better in the thick Cu lead frame than through the thin Cu layer of the DBC. The integral I^2t of planar AJT with Cu is 28% higher than the planar AJT with DBC.

The I_{FSM} value of planar AJT (Cu) is divided by four (1730A/4 ~430A), since four parallel chips are in test. It is approx. 25% higher than the I_{FSM} value of the TO-247-4 (340A), which proves the advantage of a planar AJT– especially for SiC, which heats up strongly in the first some microns of the chip. The integral I^2t of the planar AJT with Cu is almost 60% higher than the integral I^2t of a TO-247-4.

The chip temperature increases dramatically in the surge current event, which causes melting or modification of the chip metallization layer at the destruction limit. The conductive layer in a planar AJT directly attaches the full source and gate area, which enables a homogeneous current distribution among the chip and prevents a high current density, e. g. under the bond feet like in a standard AJT, see Fig. 4.

Fig. 4 Top view of decapsulated DUTs after surge current tests [3].

The heat dissipation of a planar AJT is improved because a part of the heat is transferred from the chip front side into the redistribution layer.

Measurement of thermal impedance

The thermal impedance of both packaging technologies i. e. TO-247 and the planar AJT (Cu) is measured and compared. The package was heated up at 50% nominal current for 1s and cooled down for 1s. The chart of the first 10ms is shown in Fig. 5.

The planar AJT with Cu has a lower thermal impedance than the TO-247. The drift starts immediately at around 0.1 ms and further enlarges through the time. At 10 ms, the Z_{th} value difference is around 40%.

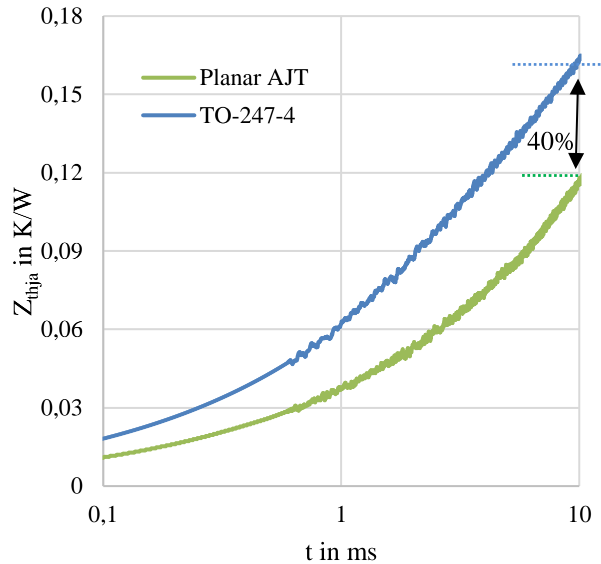

Fig. 5 Thermal impedance measurement result.

The two main reasons for the difference are:

- the heat in TO-247-4 transfers from chip to heatsink, but in the planar AJT the Cu layer on the redistribution layer attached to the chip dissipates also heat.
- The chip in the TO-247-4 is soldered on Cu lead frame, while the planar AJT has a sintered chip connection.

Further simulation will reveal the influence of each factor, which will be investigated soon.

The Z_{th} value at 10ms has 40% difference between the two packages, which is lower than the difference in surge current capability (60%).

Whereas the maximum chip temperature is the determining factor in the surge current test, the thermal impedance measurement uses the average junction temperature, which is more than 100K lower than the maximum chip temperature in a surge current event, see [4].

Influence of different VGSoff

The voltage drop of the body diode is measured until the nominal current under different V_{GS}, which is already demonstrated in Fig. 1 (third quadrant of the I-V characteristic). The voltage-drop of the body diode at V_{GS}=0V is much smaller than V_f at V_{GS}=-4V. The main reason is that at V_{GS}=0V, the gate channel still contributes to the source current and only some part of the current flows through the body diode. Up to the rated current range, the current flow differs at different negative gate-source voltage (V_{GSoff}). Depending on the input current range, the V_f difference varies from 25% to 80%.

But if the current flow reaches a higher range, e. g. up to three or four times of the rated current, the curves converged.

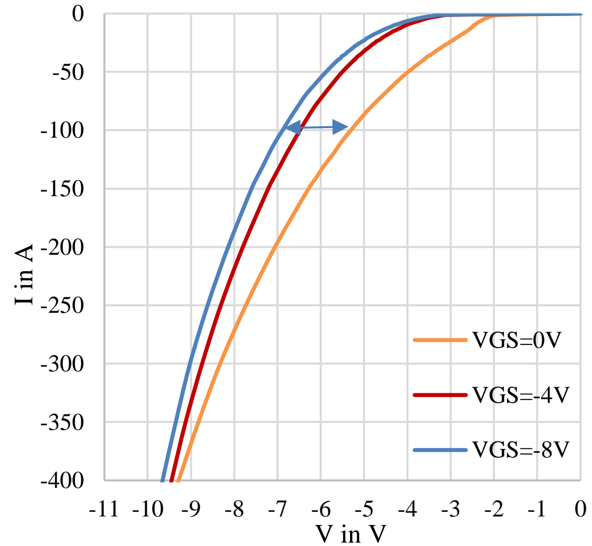

Fig. 6 I-V characteristic in third quadrant, measured up to 4 times of rated current at 30°C.

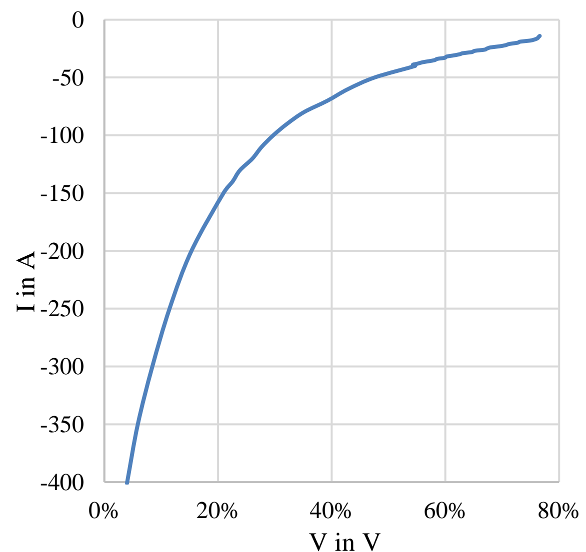

Fig. 7 the difference in voltage-drop V_{SD} in between V_{GS}=0V and V_{GS}=-8V. $\Delta V_{SD} = (V_{@Vgs=-8V} - V_{@Vgs=0V}) / V_{@Vgs=0V}$

As shown in Fig. 6, the I-V curve at different V_{GSoff} is measured up to four times of the rated current and the influence of different V_{GSoff} is getting smaller together with the increase of current. At almost four times the rating current, the difference in the voltage drop is only 5%, see Fig. 7. Most of the current flows through the body diode under a surge current condition, so the surge current capability is similar at a different gate turn-off voltage, as it was shown in [5].

Table 2 I_{FSM} measurement results at different V_{GS}, T_a=25°C.

Packaging type	V_{GS} in V	I_{FSM} before defect in A	Lowest I_{FSM} in A
TO-247-4	0V	340 340 340 340 380	340
TO-247-4	-4V	340 340 360 340 340	340

The surge current capability of the TO-247-4 package is tested with a negative gate-source voltage of V_{GS}=-4V for comparison. 5 samples were tested with the same set-up and test condition. The I_{FSM} before a destructive event is 340A, which is the same as the measurement result of TO-247 performed with V_{GS}=0V, see Table 2.

Summary

The surge current capability of a planar AJT is compared to the standard discrete packaging of a TO-247-4. The integral I^2t of this planar AJT with Cu is 60% higher than that of a standard TO247-4 discrete package. The difference in the thermal impedance explains the remarkable improvement with a planar AJT. Especially for SiC – which has a 10-times thinner drift zone. A lot of losses are generated in the first some microns of the chip. Therefore, a good front-side cooling/thermal capacitance is helpful for short-time events like surge currents.

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