Compact GaN-based Bidirectional Polarization Super Junction HFETs with Schottky Gate on Sapphire

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Abstract

Performance evaluation of compact GaN-Based Bidirectional Polarization Super-Junction Heterojunction Field Effect Transistors with Schottky Gate (Bi PSJ SG HFET) fabricated on the sapphire substrate is presented in this paper. The on-state performance under various bias conditions is simulated and measured, and the operating mechanisms are analysed. Measured electric characteristics of fabricated Bi PSJ SG HFETs show symmetrical characteristics in the first and third quadrants, successfully realizing the bidirectionality. The logic function of the on-state performance of Bi PSJ HFETs is summarized. Numerical simulations show that a device can withstand high blocking voltages with a "box" like electric field in the common drift region. The measured average area-specific on-state resistance Ron. A of a Bi PSJ SG HFET is 64 mΩ.cm2 in both directions at room temperature for a device with a 40µm length of PSJ. In addition, temperature dependence on the area-specific on-state resistance of Bi PSJ SG HFETs with 40µm is also measured. Using analytical models of on-state resistance, the Ron. A is calculated and fit well with measured results with different PSJ length.

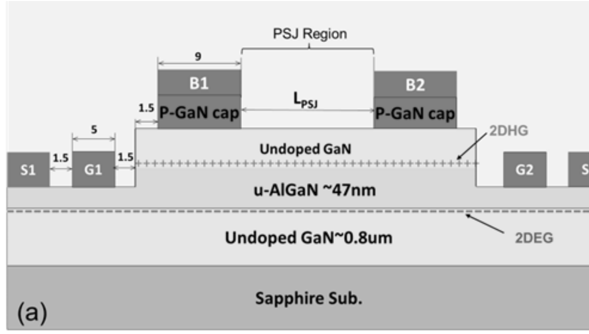
Keywords: GaN; Polarization Super Junction; bidirectional switch

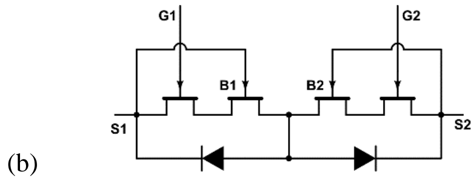
INTRODUCTION

GaN-based power converters are attracting much attention and have become excellent candidates for power electronic applications because of their superior material properties. GaN devices with lateral structures utilizing high-mobility Two-Dimension Electron Gas (2DEG) have been extensively researched, and they dominate the GaN semiconductor market because of their low on-state resistances [1]. In 2006, the concept of Polarization Super Junction (PSJ) was proposed to enhance the breakdown voltage of GaN lateral devices and suppress current collapse ([2], [3]). PSJ technology is based on undoped GaN/AlGaN/GaN double heterostructures. It utilizes the charge compensation effect through high-density positive and negative polarization charges formed at each of the hetero-interfaces to enable a flat electric field distribution in the blocking condition [4]. GaN-based bidirectional Super Heterojunction Field Effect Transistors (BiSHFETs) with metal-semiconductor and PN junction gate structures using the PSJ concept was first demonstrated in 2012[5]. This paper proposes more compact Bidirectional PSJ HFETs with Schottky Gate (Bi PSJ SG HFETs) on sapphire substrate. Such monolithic bidirectional devices fabricated on insulator substrates are seen as essential elements for the next generation of ultra-compact and efficient power electronics systems [6]. There are previous reports on simulation and experimental demonstration of monolithic bidirectional switches reported in Silicon ([7], [8]), SiC ([9], [10]) and conventional GaN[11].

DEVICE STRUCTURE

Fig.1(a) shows a simplified cross-section of a bidirectional PSJ HFET with Schottky Gate (Bi PSJ SG HFETs) with geometric parameters. As shown in Fig.1(a), the basic structure of the Bi PSJ HFET arises from GaN/AlGaN/GaN double heterostructures which employs an inherent charge balance in the common PSJ drift region. The Bi PSJ HFET with Schottky Gate is a symmetrical device with six electrodes. There are two source electrodes (S1 and S2), two base electrodes (B1 and B2), and two gate electrodes (G1 and G2). S1 and S2 form ohmic contacts to 2DEG, while G1 and G2 form Schottky contacts. Two base electrodes (B1 and B2) are ohmic to 2DHG and can be connected to the sources (S1 and S2) or the gates (G1 and G2) to form four-terminal devices. When bases are connected with adjacent sources, the device can provide an inherent body diode in either direction [12]. The distance between two base electrodes is defined as the length of the PSJ region (L_{PSJ}). The schematic equivalent circuit





(b)

Figure 1: (a) A simplified cross-section of Bidirectional PSJ HFETs with Schottky Gate. Dimensions are in µm. (b) The schematic equivalent circuit of Bi PSJ SG HFETs.

in Fig.1(b) stands for Bi PSJ SG HFETs considered in this study.

Like unidirectional PSJ HFETs, the $\boldsymbol{L_{PSJ}}$ is used to support the forward blocking voltage and can be scaled up directly as a function of its length ([2], [13]). As reported in [4], a unidirectional PSJ HFET with $\boldsymbol{L_{PSJ}}$ of 40µm can withstand blocking voltages above 3 kV.

DEVICE SIMULATION

The device behaviour of Bi PSJ SG HFETs with 40µm-L_{PSJ} has been analyzed under various bias conditions by TCAD simulation and validated with experiments [7]. The simulated device structure is shown in Fig.1(a), which corresponds to fabricated devices with parameters as described later. In this study, Base (B1 and B2) electrodes are connected to the adjacent sources acting as a four-terminal device.

On-state Characteristic

Fig. 2 and Fig.3 shows simulated I_{s2}-V_{s2s1} characteristics of Bi PSJ SG HFETs with 40µm-L_{PSJ} working under two different bias conditions. Inset figures in Fig.2 and Fig.3 are simplified testing circuits.

Fig.2 shows simulated symmetrical I_{s2}-V_{s2s1} characteristics of Bi PSJ SG HFETs with 40µm- L_{PSJ} in both directions. According to a condition of Source 2 voltage with respect to Source1 voltage, the I_{s2}-V_{s2s1} characteristics can be divided into two regions, which are defined as 'Forward Region' and 'Reverse Region'. Here, the 'forward' refers to the S2 voltage being positive with respect to S1 (V_{s2s1}>0), and the 'reverse' refers to V_{s2s1} as negative (V_{s2s1}<0). In the forward region, Gate2 is referenced with respect to adjacent S2 (V_{g2s2}=0V) while the voltage of Gate1 changes from -6V to 0V with a 1V step, as shown in the inset circuit in Fig.2. Here, the device works as a three-terminal GaN device. In a manner like a conventional HFET, the forward current Is2 flows from S2 to S1 through the 2DEG and is controlled by Gate1 voltage (V_{g1s1}). As V_{g1s1} reduces to less than -6 V, the device enters off-state. The simulated forward on-state resistance (Ron) for L_{PSJ}=40µm is 33 Ω.mm at V_{s2s1}=1V, V_{g1s1}=0V. In the reverse region, Gate1 is connected with Source1. Simulated reverse characteristics of I_{s2}-V_{s2s1} are identical to that of forward because Bi PSJ SG HFETs have a symmetrical structure.

In Fig.3 the simulated I_{s2}-V_{s2s1} characteristics are obtained when keeping a negative Gate2 voltage with

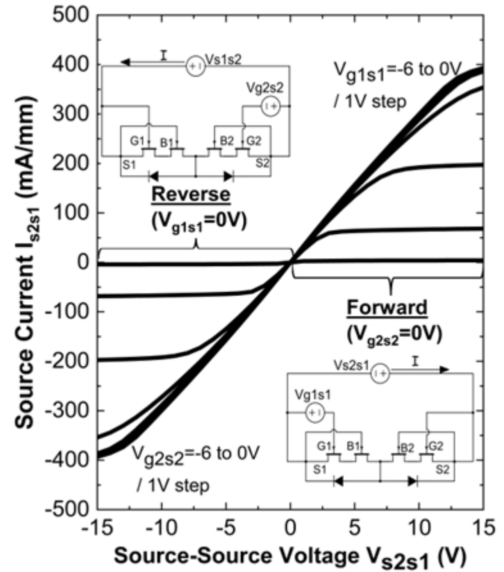


Figure 2: Simulated forward Is-Vs2s1 characteristic of Bi PSJ SG HFETs in both directions.

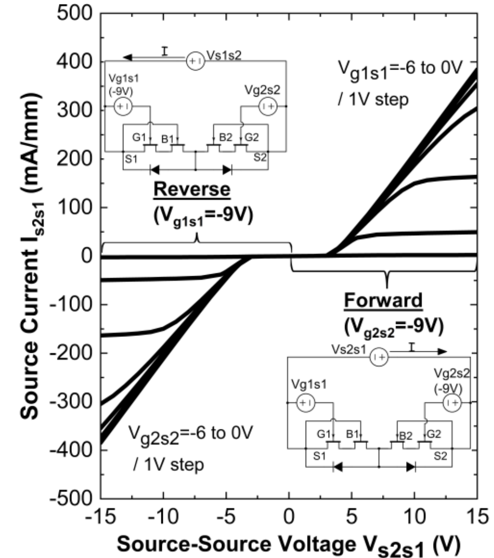


Figure 3: The simulated Is2-Vs2s1 characteristic with a negative gate2 voltage Vg2s2 of -9V (Vg2s2=-9V) in the forward region while -9V Vg1s1 in the reverse region.

respect to Source2 at -9V in the forward region while keeping V_{g1s1}=-9V in the reverse region. Source current I_{s2s1} in the forward and reverse bias condition is successfully controlled by Gate1 voltage (V_{g1s1}) and Gate2 voltage (V_{g2s2}) respectively, although the on-state voltage increases. The main reason for the increased 'forward' on-state voltage is that the 2DEG under Gate2 is fully depleted when the applied Gate2 voltage is negative, which is smaller than the threshold voltage. Therefore, the region under Gate2 performs as a diode depletion region. The calculated 'forward' on-state voltages at I_{s2} = 10mA/mm is 0.4 V (V_{g2s2} = 0 V) and 3.1 V (V_{g2s2} = -9 V) respectively. In the reverse region, the region under Gate1 is depleted.

Bias conditions			Device State
V_{s2s1}	V_{g1s1}	V_{g2s2}	
V_{s2s1}>0	On	On	On
	On	Off	V_{on} increase
	Off	On	Off
	Off	Off	Off
V_{s2s1}<0	On	On	On
	On	Off	Off
	Off	On	V_{on} increase
	Off	Off	Off

Table 1: Summarised device behaviour

According to the simulated results, the logic behaviour of bidirectional PSJ Schottky Gate HFETs in various bias conditions can be summarized in Table 1, which is in agreement with the simulation results reported in [5]. When V_{s2s1} is positive, Bi PSJ SG HFETs are controlled by Gate 1, while Bi PSJ HFETs are controlled by Gate 2 in a reverse bias condition.

Off-state Characteristic

Fig.4(a) shows the simulated off-state 2-D electrical potential distribution at a forward bias of $V_{s2s1}=8200V$, $V_{g1s1}=-15V$ *and* $V_{g2s2}=0V$ in an ideal case. The equipotential lines are distributed almost uniformly along the PSJ region. Under a forward bias of V_{s2s1}, G2 and S2 are connected as 'Drain' of three-terminal devices, and G1 is applied with -15V to turn off the device. The 2DHG and 2DEG of Bi PSJ SG HFETs are discharged through Base and 'Drain', respectively. Once the drift region between two bases of the Bi PSJ SG HFET is depleted, and flat electrical field distribution can be obtained over this region dur to charge balance between 2DHG and 2DEG. Fig.4(b) and Fig.4(c) are the 1-D potential distribution and the 1-D electric field along the x-coordinate at a position identified by the black dotted line (A-A') of Fig.4(a), respectively. As shown in Fig.4(c), the electric field is over the PSJ region, and the breakdown occurs at the edge of the Base. Under ideal forward blocking conditions, the simulated breakdown Voltage (BV) of Bi PSJ SG HFETs with 40µm-L_{PSJ} is 8260V at V_{g2s2}=0V, well above 3.3kV.

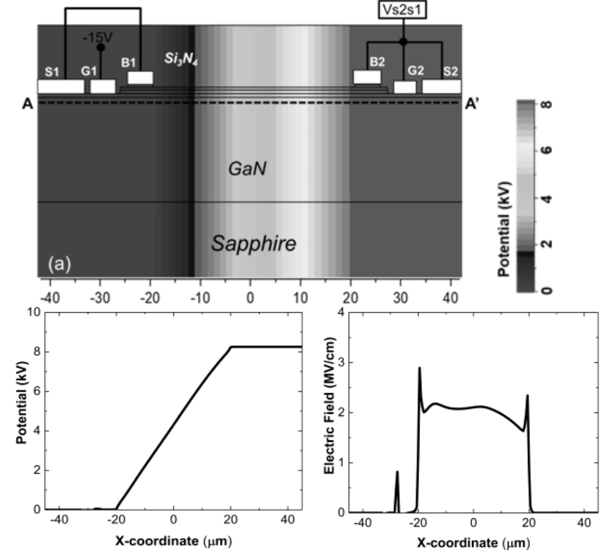


Figure 3: (a) The off-state 2-D electrostatic potential distribution at a forward bias of Vs2s1=8200V, Vg1s1=-15V and Vg2s2=0V. (b)The 1-D potential distribution and (c)The 1-D electric field intensity along the x-coordinate along the black dotted line (A-A') in Fig.4(a).

Previous results on unidirectional PSJ HFETs show a linear relationship between breakdown voltage and PSJ length ([4], [7]). Based on this, conservatively, it can be estimated that BV increases by 500 V for every 5µm increase in L_{PSJ}. Considering that the measured BV is around 2.5kV for a unidirectional PSJ HFET with 20µm-L_{PSJ} [13] on Sapphire, a bidirectional device with a 40µm-L_{PSJ} can be reasonably expected to withstand the voltage well above 3.5 kV.

EXPERIMENTAL RESULTS

Fig.5 shows the simplified cross-section of fabricated Bi PSJ SG HFETs with 40µm-L_{PSJ}. Generally, the GaN buffer layer of GaN HEMTs is doped by acceptors like Carbon (C), which can help prevent leakage through the buffer region by lifting the GaN conduction band upwards by better confining the 2DEG channel and preventing the 2DEG spillover effect in the buffer. In this study, in order to only observe the polarization superfunction related effects on 2DEG/2DHG charge control conventional background, Carbon acceptor

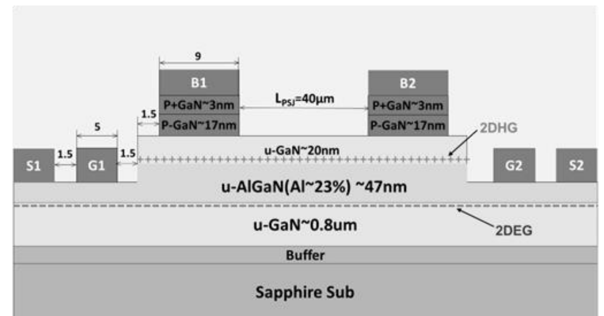


Figure 4: A simplified cross-section of fabricated Bi PSJ SG HFETS with 40µm-L_{PSJ}.

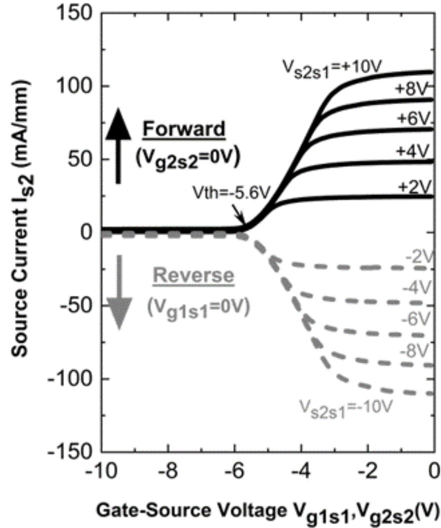


Figure 5: Measured transfer characteristics of fabricated Bi PSJ SG HFETs in both directions.

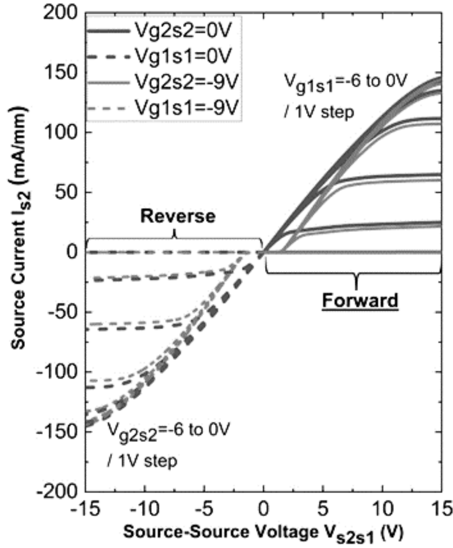


Figure 7: Measured Is2-Vs1s2 characteristics of fabricated Bi PSJ SG HFETs in both directions with various bias conditions.

doping is not used in the GaN buffer region. These Bi PSJ SG HFETs are built on undoped GaN/AlGaN/GaN double heterostructures grown on a sapphire substrate. It consists of an 0.8µm-thick undoped GaN buffer layer (u-GaN), a 47nm-thick un-doped AlGaN layer with an Al composition of 23%, and a 20nm-thick un-doped GaN layer. A 17nm-thick p-type doped GaN cap (P-GaN) layer with $5 \times 10^{19} cm^{-3}$ and a 3nm-thick P-GaN layer with $2 \times 10^{20} cm^{-3}$ have been grown on u-GaN, which enable an ohmic contact to 2DHG. Fabricated Bi PSJ SG HFETs on Sapphire substrate have four pads of Gate1, Gate2, Source1 and Source2. Two bases are connected to the adjacent source electrode, respectively.

Measurement of Fabricated Bi PSJ SG HFETs

Fig. 6 shows transfer characteristics of fabricated Bi PSJ SG HFETs with 40µm-L_{PSJ}. The Source current I_{s2} in the forward and reverse bias conditions are successfully controlled by Gate1 voltage (V_{g1s1}) and Gate2 voltage (V_{g2s2}), respectively. The threshold voltage V_{th} of Bi PSJ SG HFETs is 5.6V in both directions. Fig.7 shows I_{s2}-V_{s2s1} characteristics of the fabricated Bi PSJ SG HFET with 40µm-L_{PSJ}. Bias voltage settings are consistent with that in the simulation described earlier. As shown in the figure, the measured I_{s2}-V_{s2s1} characteristics are symmetrical in both directions and realize the logic functions of bidirectional switching shown in Table1. Calculated on-state voltages at I_{s2}=10mA/mm are 0.8 V (V_{g2s2} = 0 V) and 2.2 V (V_{g2s2} = -9 V) in the 'forward Region' at room temperature. Under different bias conditions, fabricated Bi PSJ SG HFETs can be operated as bidirectional switches, unidirectional HFETs with Drain Injection Transistor (DIT) mode and diodes in both directions.

Fig.8 shows the buffer leakage and the surface leakage of the inset structure in Fig.8. Without C-doping in GaN buffer layer, the unintentionally doped buffer layer ends up slightly n-type and causes buffer leakage issues. This buffer leakage is the dominant factor in the leakage current in the off state for Bi PSJ SG HFETs. The surface leakage, associated with poor passivation, surface states and sidewall damage, is reasonably low which suggests good process control. Due to the high buffer leakage, a slightly high leakage current of around 6mA/mm at 200V under forward blocking conditions was measured. Equipment compliance limits further forward blocking voltage measurement. Fig.9 shows the measured leakage currents between two bases of the device with 40µm-L_{PSJ}, with a measured value of about 19nA/mm at V_{B2B1}=100V.

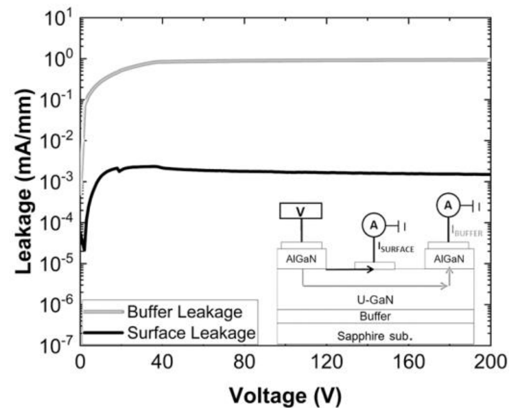


Figure 6: Measured buffer leakage and surface leakage.

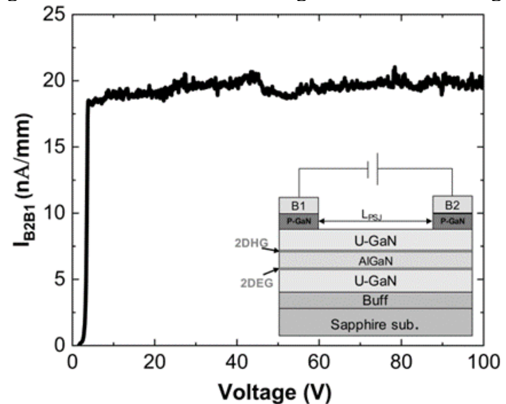


Figure 9: Measured leakage between B1 and B2.

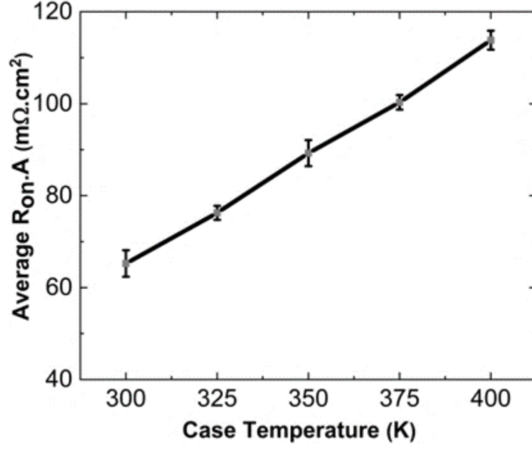


Figure 10: The average Ron. A of fabricated Bi PSJ SG HFETs with 40µm- L_{PSJ} at a temperature from 300K to 400 K.

This base leakage is obtained when keeping 2 gates floating and V_{s2s1} at 0V. The purpose of this study is to validate the device concept and functionality with different gate polarity control. Future work is needed with optimum epitaxial structure for demonstrating high voltage breakdown devices.

The average variation in Ron.A of 8 samples of Bi PSJ SG HFETs with 40µm-L_{PSJ} as a function of case temperatures are presented in Fig.10. When the temperature increases from 300K to 400K, Ron.A of Bi PSJ SG HFETs is found to increase from 65.24mΩ.cm2 to 113.82mΩ.cm2 in a linear fashion. The maximum discrepancy is within 5.31% of its mean value at 350K.

Calculation and Analysis on Ron.A

Under on-state conditions, the source current is flowing through the 2DEG and is controlled by Gate1 in the forward region and Gate2 in the reverse region. According to differences in the sheet carrier density and the mobility of 2DEG and 2DHG, Bi PSJ SG HFETs can be divided into different areas. As shown in Fig.11, along the dashed line which the current flow direction, the device can be divided into seven regions, namely the PSJ region, channel regions, gap regions, and contact regions. Gap regions consist of 2 areas between the source and the adjacent gate. Regions under 2 bases are defined as

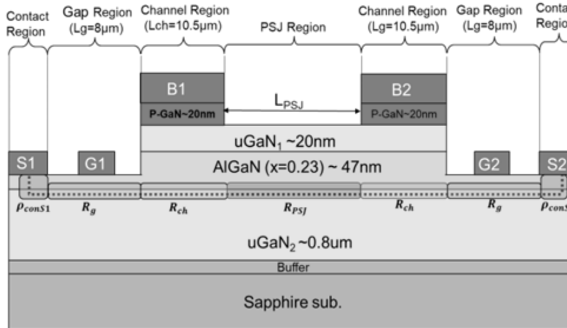


Figure 7: The calculated and measured Ron.A of Bi PSJ SG HFETs and PSJ OG HFETs with L_{PSJ} from 5µm to 40µm at room temperature.

channel regions, and contact regions are under source electrodes. Therefore, the total specific ON-state resistance (Ron.A) can be considered as the sum of the PSJ region resistance (R_{PSJ}), two channel region resistance (R_{ch}), and two gap regions resistance (R_g) multiplies the device area (A) and then plus the contact resistivity (ρ_{conS1} and ρ_{conS2}), as shown in Equation (1).

$$R_{on}A = (R_{PSJ} + 2R_{ch} + 2R_g) \times A + \rho_{conS1} + \rho_{conS2} \quad (1)$$

The contact resistivity of the Source1 and the Source2 electrode ($\boldsymbol{\rho_{conS1}}$ *and* $\boldsymbol{\rho_{conS2}}$) can be measured and calculated by the transmission line method (TLM), as shown in

$$\rho_{conS1} = \rho_{conS2} = R_c \times L_T \times W = 0.26\, m\Omega \cdot cm2 \quad (2)$$

The resistance of other regions can be expressed as

$$R = \frac{L}{q\mu\sigma W} \quad (3)$$

Where q is the electron charge, W stands for the device width. μ stands for the mobility of 2DEG and σ is the 2DEG sheet density. L is the length of the region, which is shown in Fig.11.

In the calculation, the 2DEG mobility (µ) is set around 700cm^2/Vs same as the measured value, and the device width is assumed constant. The resistance of the PSJ region, gap regions and channel regions are determined by the length (L) and the sheet density (σ) of each region. The sheet density (σ) can be calculated by using analytical models of sheet carrier densities in PSJ HFETs[13], which is influenced by the thickness of PSJ layers and Al mole fraction. Considering that partial carriers are captured by traps which have gained high kinetic energy after being accelerated by the electric field, the sheet density of 2DEG is adjusted with experimental results.

Fig.12 presents the calculated and measured Ron.A of Bi PSJ SG HFETs with L_{PSJ} from 5µm to 40µm at room temperature. The identical Vg (Vg1) = 0V is applied to the calculation and measurement. As presented in Fig.12, calculated Ron.A of Bi PSJ SG HFETs fits well with the experimental results when altering PSJ length from 5 to 40µm. Factors like the fabrication misalignment between processes and random measurement errors attribute to differences in Fig.12. In addition, it should be noted that the 2DEG mobility for each region is assumed as constant in calculations, unlike actual devices, which can be affected by some factors, such as charge concentration and electrical field. The resistance of 2 gap regions (R_g) and 2 channel regions (R_{ch}) contribute to additional resistance for Bi PSJ SG HFETs, because of the thin AlGaN layer, the low Al mole function and the long region length. Table 2 shows the calculated resistance component ratio to the total Ron.A of Bi PSJ SG HFETs with L_{PSJ} from 5µm to 40µm. With the decrease in L_{PSJ}, the percentage of R_{ch} and R_g to the total Ron.A becomes large.

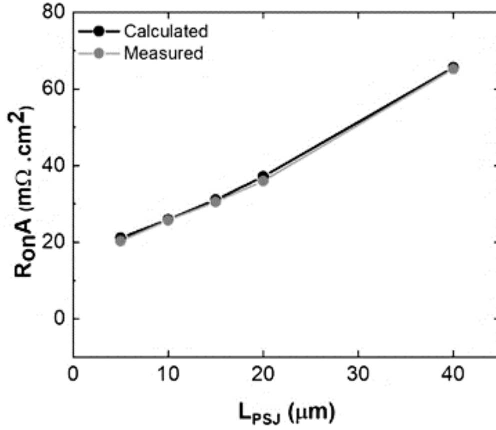


Figure 8: The calculated and measured Ron.A of Bi PSJ SG HFETs with L_{PSJ} from 5μm to 40μm at room temperature.

L_{PSJ} (μm)	Component Ratio (%)			ρ_{conS} (mΩ.cm^2)	Ron.A (mΩ.cm^2)
	R_{PSJ}	R_g	R_{ch}		
5	10	46	44	0.26	21.07
10	19	42	40		25.91
15	26	38	36		31.26
20	32	35	33		37.12
40	48	27	25		65.64

Table 2: Each component ratio to the total Ron in the Analytical model.

CONCLUSIONS

In this paper, the performances of compact bidirectional HFETs with Schottky Gate using the PSJ concept are presented. These devices share the same drift region in operation in the first and third quadrants and therefore can be one of the most compact bidirectional switches reported to date. The simulated and measured electrical characteristics display logic functions of bidirectional switching in various bias conditions. The simulated off-state I_{s2}-V_{s2s1} shows Bi PSJ SG HFET with a 40μm length can withstand the voltage well above 8 kV in an ideal condition. In any case, based on measured data of unidirectional PSJ HFETs fabricated on Sapphire using similar material configurations, off-state performances in excess of 3.3 kV are reasonable. The average measured area-specific on-state resistance Ron.A of Bi PSJ SG HFET with L_{PSJ}=40μm is 65.24 mΩ.cm2. The linear increase in the Ron.A as a function of temperature of Bi PSJ HFETs as well as the on-state resistance versus L_{PSJ} show that the device can be scaled easily scaled in both voltage and currents. We also built the analytical model of on-state resistance of Bi PSJ SG HFETs to calculate and analyze its components.

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REFERENCE

[1] M. A. Khan, A. Bhattarai, J. N. Kuznia, and D. T. Olson, “High electron mobility transistor based on a GaN-AlGaN heterojunction,” vol. 63, no. August 1993. 2001.

[2] A. Nakajima, K. Adachi, M. Shimizu, and H. Okumura, “Improvement of unipolar power device performance using a polarization junction,” Appl. Phys. Lett., vol. 89, no. 19, pp. 10–13, 2006.

[3] A. Nakajima, Y. Sumida, M. H. Dhyani, H. Kawai, and E. M. Narayanan, “GaN-based super heterojunction field effect transistors using the polarization junction concept,” IEEE Electron Device Lett., vol. 32, no. 4, pp. 542–544, 2011.

[4] H. Kawai et al., “Low-cost high voltage GaN polarization superjunction field effect transistors,” Phys. Status Solidi Appl. Mater. Sci., vol. 214, no. 8, 2017.

[5] A. Nakajima et al., “GaN-based bidirectional super HFETs using polarization junction concept on insulator substrate,” Proc. Int. Symp. Power Semicond. Devices ICs, no. June, pp. 265–268, 2012.

[6] J. W. Kolar, “Monolithic Bidirectional Switches-Opening new horizons in Power Electronics,” in ICSCRM Plenary talk, 2022.

[7] F. Heinke and R. Sittig, “The monolithic bidirectional switch (MBS),” IEEE Int. Symp. Power Semicond. Devices ICs, pp. 237–240, 2000.

[8] A. Mojab, J. Bu, J. Knapp, A. Sattar, and D. Brdar, “Operation and Characterization of Low-Loss Bidirectional Bipolar Junction TRANsistor (B-TRANTM),” Conf. Proc. - IEEE Appl. Power Electron. Conf. Expo. - APEC, pp. 205–209, 2022.

[9] S. Chowdhury, C. Hitchcock, R. Dahal, I. B. Bhat, and T. P. Chow, “High Voltage 4H-SiC Bi-Directional IGBTs,” pp. 463–466, 2016.

[10] K. Han et al., “Monolithic 4-Terminal 1.2 kV/20 A 4H-SiC Bi-Directional Field Effect Transistor (BiDFET) with Integrated JBS Diodes,” Proc. Int. Symp. Power Semicond. Devices ICs, vol. 2020-September, pp. 242–245, 2020.

[11] G. M. B. Switch and U. Normally-off, “650 V 3.1 mΩcm2 GaN-based monolithic bidirectional switch using normally-off gate injection transistor,” IEDM Tech. Dig., pp. 97–98, 2007.

[12] A. Nakajima, M. H. Dhyani, E. M. S. Narayanan, Y. Sumida, and H. Kawai, “GaN based Super HFETs over 700V using the polarization junction concept,” Proc. Int. Symp. Power Semicond. Devices ICs, no. d, pp. 280–283, 2011.

[13] H. Yan, Y. Du, P. Luo, X. Tan, and E. M. S. Narayanan, “Analytical Modeling of Sheet Carrier Density and

on-Resistance in Polarization Super-Junction HFETs," IEEE Trans. Electron Devices, vol. 68, no. 11, pp. 5714–5719, 2021.
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