Adapted Temperature Calibration for Schottky p-GaN Power HEMTs

[1]Maximilian Goller, [1]Jörg Franke, [1]Max Fischer, [2]Samir Mouhoubi, [2]Gilberto Curatola, [1]Josef Lutz, [1]Thomas Basler

[1]Chemnitz University of Technology, Chair of Power Electronics, Germany

[2]Huawei Nuremberg Research Center

Abstract

The determination of the junction temperature in power semiconductor devices is an important but challenging task. For GaN HEMTs, no universal temperature sensitive electrical parameter (TSEP) is available. In this study, different GaN HEMTs with Schottky p-GaN gate were subjected to stress by positive gate bias and temperature. The gate leakage current is one parameter to determine the junction temperature of Schottky p-GaN gate devices. An adapted calibration routine is applied to stabilize the desired TSEP of different GaN HEMTs. The gate current method can be applied to GaN Systems devices. Furthermore, the investigations indicate stability of the on-state resistance of Innoscience devices and threshold voltage of EPC devices, respectively.

Keywords: GaN HEMT, Schottky contact, p-GaN gate, TSEP, adapted temperature calibration.

INTRODUCTION

Gallium Nitride (GaN) power HEMTs are key components to design power electronic systems with high efficiency and smaller volume. The wide band gap (3.39 eV), the high critical electric field strength and low device capacitances enable small drift layers and high frequency operation. Thereby, switching- as well as conduction losses can be reduced. Currently, devices with Schottky gate are available from several manufactures in the voltage range from 15 V to 700 V [1]–[5]. The device concept enables normally-off operation with a voltage controlled gate. However, due to the lateral concept, the package and chip-near interconnections differ significantly from vertical power electronic devices made of Si (IGBTs, diodes) as well as from SiC (MOSFETs, diodes). Instead of thick-wire wedge bond technologies, nailhead technologies [6], [7] or low-inductive integration [8] are used. Precise knowledge of the junction temperature is relevant for lifetime modelling in e. g. power cycling, but also for the measurement of the transient thermal impedance. Therefore, the use of temperature sensitive electrical parameter (TSEPs) is established [9]. In Schottky p-GaN devices no pn-junction is directly accessible and the forward gate leakage current was introduced as alternative [10]. During this process, the Schottky p-GaN junction at the gate is biased in reverse direction. This is a simultaneous gate stress test within datasheet limits. No hard failures were observed, but device parameters tend to shift [3], [11]. The calibration of temperature at constant gate bias V_{GS} is used to stress the device at high temperatures and static device parameters are monitored.

TEMPERATURE CALIBRATION

In the following, temperature determination in power electronics for reliability testing is discussed. Furthermore, an introduction of the devices and the temperature determination by using the Schottky junction is given.

Temperature Sensitive Electrical Parameters

The temperature of the power electronic chip is usually referred to as junction temperature. Indirect or contactless measurement of these is possible by means of optical processes or electrical methods. Optical measurements for example infrared thermography are challenging in practice, because they require access to the chip surface. Electrical methods like the $V_{CE}(T)$ method utilize the temperature dependency of chip internal parameters like the diffusion voltage of the pn-junction (see **[12]**) for determination of the temperature:

$$V_{bi} = \frac{kT}{q} \cdot \ln(\frac{N_D \cdot N_A}{n_i^2}) \qquad (1)$$

Equation (1) is dominated by the intrinsic carrier concentration n_i, which results in a negative temperature coefficient behavior. Therefore, a constant measurement current is applied to the devices and one obtains the voltage across the total active area. It is also referred to as the virtual junction temperature T_{VJ}. The maximum of the junction temperature cannot be determined by TSEPs, but by simulation or optical methods. In gate injection transistors (GITs); the pn-junction of the gate can be biased at constant gate current of e.g. 10 mA (Figure 1).

The curve can be fitted accurately with a second order polynomial function.

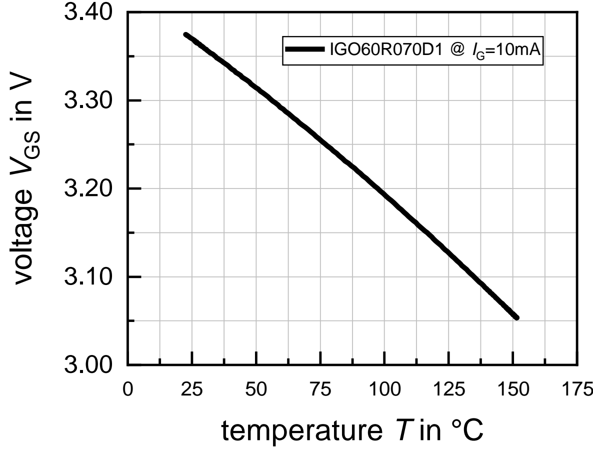

Figure 1: Temperature calibration curve of a GIT IGO60R070D1 from Infineon

Alternatively, on-chip temperature sensors [13] or the internal gate resistance as another TSEP [14] can be used. In contrast to an average value like the virtual junction temperature, on-chip sensors provide local temperatures and permit a measurement also during load current of the device. Overall, on-chip sensing can offer very unique and valuable information, but they are strongly dependent on the sensor positioning.

Schottky p-GaN HEMTs

The schematic cross-section of GaN HEMTs with Schottky p-GaN gate is displayed in Figure 2. The two-dimensional electron gas (2DEG) is depleted by a p-GaN at the gate. The Schottky gate metal results in two back-to-back diodes between gate and source. In MOSFETs, an alternative TSEP is given by the body diode [9]. Despite the fact, that there is no body diode in GaN HEMTs, an inverse barrier forms at zero gate voltage in reverse operation [15]. While the inverse barrier was found to be stable for GITs [16], no stable operation of the V_{SD}(T) voltage was demonstrated for devices with Schottky gate. The back-to-back diode structure has the property that one of the diodes is always operated in the reverse direction. For positive gate bias, the Schottky junction is operating in blocking- and the AlGaN pn-diode in forward direction. In low current regime, below the V_{bi} of the AlGaN pn-diode (approx. 3 V), the current is limited through this. Above, the blocking Schottky p-GaN junction dominates the behavior with its leakage and breakdown behaviour.

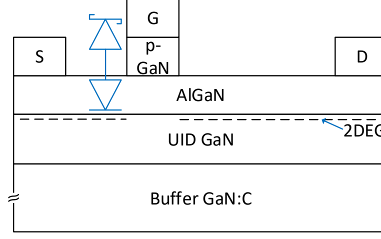

Figure 2: Schematic cross-section of a Schottky p-GaN HEMT

In [10], the possibility of utilizing the reverse leakage current of the Schottky junction at positive gate bias was introduced as TSEP. Therefore, instead of a constant current, a constant gate voltage is to be applied and the temperature dependent gate current I_G(T) is monitored. The gate leakage current of MOSFETs is usually given as I_{GSS} for shorted drain-to-source. Thereby, both capacitances C_{GS} and C_{GD} are biased simultaneously, which theoretically results in a higher overall gate leakage current. However, there is hardly any change between the open-drain and drain-to-source short configuration visible at a nominal voltage of $V_{GS} = 6$ V (see Figure 3). For online junction temperature determination e.g. in a power cycling test, the additional shortening would represent an increased effort. Hence, the drain can be left open for the temperature calibration, but should be shorted to drain for the gate stress tests. The temperature dependency of the gate leakage current of the Schottky junction can be described by the saturation current in reverse operation [12]

$$j_s = A^* \cdot T^2 \cdot e^{\frac{q(V_B - \Delta\Phi)}{kT}} \quad (2)$$

Here, A* is the effective Richardson constant and qV_B is the contact barrier height. Under reverse bias operation, the potential is lowered and the image force **ΔΦ** must be considered. Hence, the temperature dependency of the reverse leakage current follows ideally a quadratic dependency.

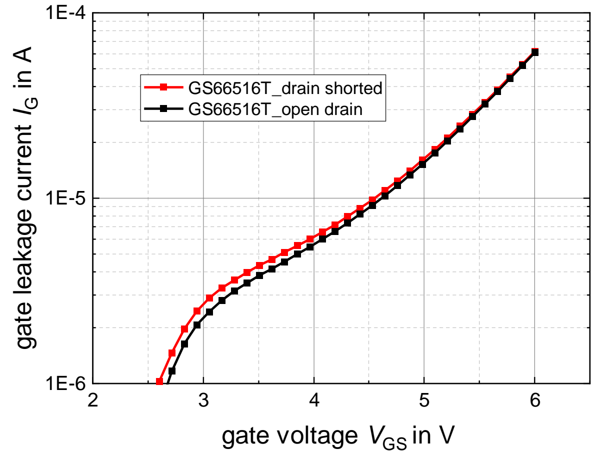

Figure 3: Gate leakage current in drain-to-source short and open-drain configuration for devices GaNSystems GS66516T at T= 25°C

EXPERIMENTAL RESULTS

The gate current method I_G(T) was so far applied to GaNSystems devices in the voltage class of 650 V [7], [10]. Nevertheless, there are still some uncertainties to its validity. Particularly, the possibility of the degradation in the gate leakage current and instabilities in threshold voltage [11]. Here, three devices from different manufacturers and of different voltage class are under investigation. The behavior of the Schottky gate is to be observed under forward bias with respect to temperature, degradation and shift of parameters.

Gate I-V Characteristics

An overview of the devices and selected device parameters are displayed in Table 1. The level of the gate current varies due to the significantly different R_{DSon} that correlates to the gate width of the device and the active area.

Table 1. Investigated devices and selected device parameters

Manufacturer	Device	V_{BD} [V]	V_{GSnom} [V]	R_{DSon} [mΩ]
GaN Systems	GS-065-011-2-L **[17]**	650	6	150
Innoscience	INN650D350A **[18]**	650	6	350
EPC	EPC2302 **[19]**	100	5	1.8

The gate I-V characteristics of all three types of devices are displayed with respect to temperature in Figure 4, Figure 5 and Figure 6. The drain and source were shorted to acquire I_{GSS}. The gate current per mm was calculated using the estimated device gate width. The influence of the AlGaN diode is clearly visible for GaNSystems in Figure 4, but is less pronounced at Innoscience (Figure 5) or EPC device (Figure 6). At nominal gate voltage, the device from EPC has the lowest gate leakage current density.

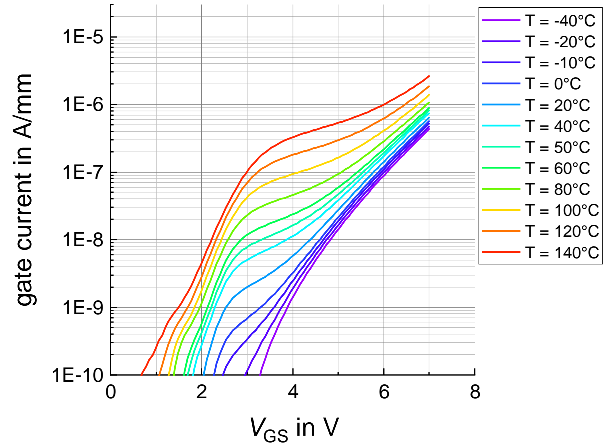

Figure 4: GaNSystems GS-065-011-2-L - gate leakage current at shorted drain-source for various temperatures

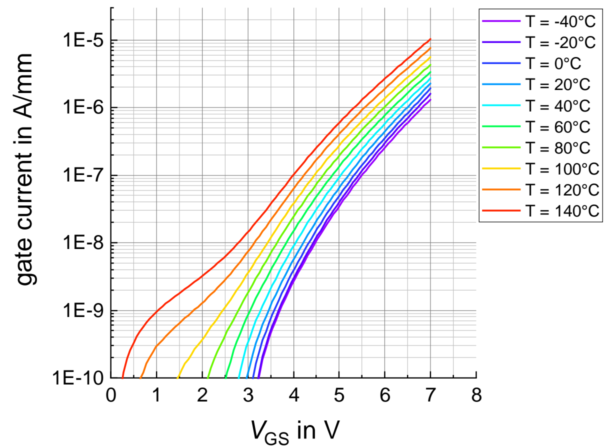

Figure 5: Innoscience INN650D350A - gate leakage current at shorted drain-source for various temperatures

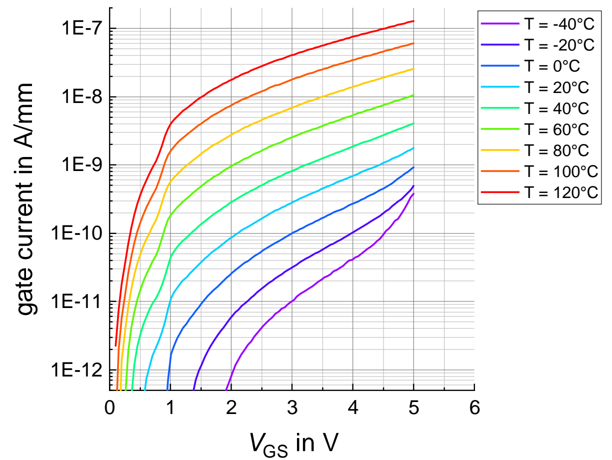

Figure 6: EPC 2302 - gate leakage current at shorted drain-source for various temperatures

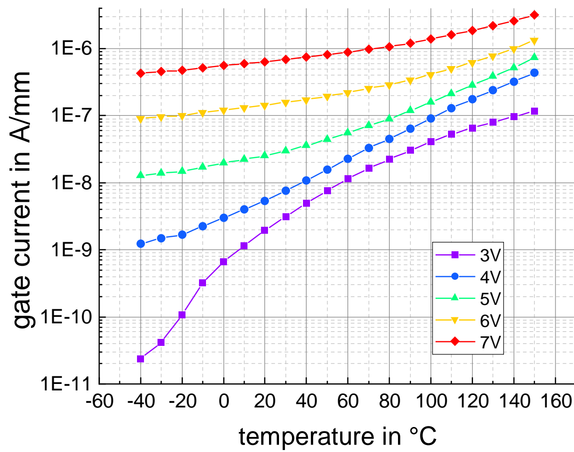

Figure 7: GaNSystems GS-065-011-2-L temperature dependent gate leakage current at shorted drain-source for different gate voltages

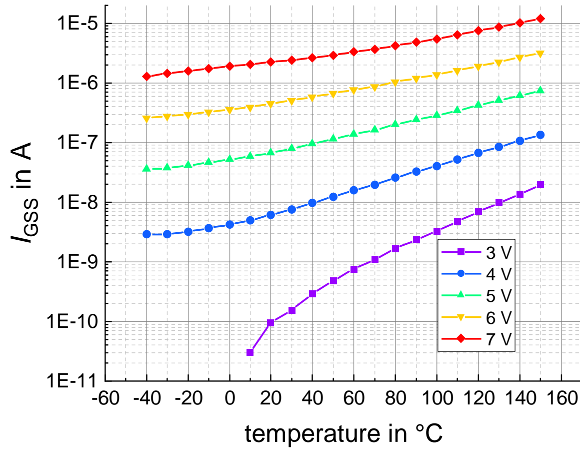

Figure 8: Innoscience INN650D350A temperature dependent gate leakage current at shorted drain-source for different gate voltages

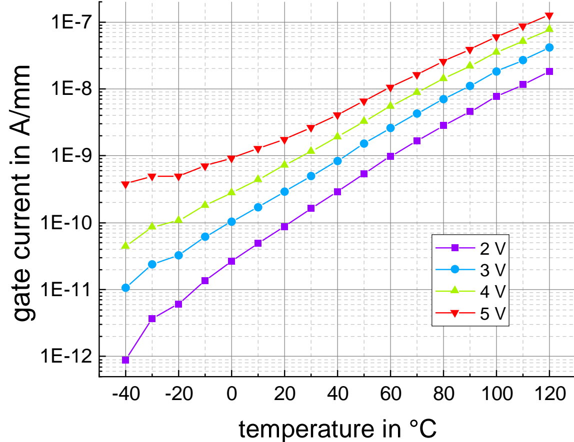

Figure 9: EPC 2302 temperature dependent gate leakage current at shorted drain-source for different gate voltages

The GaNSystems device in Figure 7 shows a strongly increasing gate leakage current tendency at higher temperatures and gate voltages. However, the influence of the gate voltage on the gate leakage reduces with increasing current and the curves are closer together at 150°C than at -40°C. Furthermore, at a gate voltage of 3 V, the influence of the temperature dependency of the pn-junction at low temperature is significant. Similar behavior is observed for the Innoscience device. It must be noted that the device – from on-state resistance point of view – is approximately 3 times smaller than the investigated GaNSystems device. For gate voltages of 4 V to 7 V a nearly parallel shift is identified. The EPC device in Figure 9 indicates a much stronger, highly exponential behavior across the complete temperature range. At 2 V, the gate current increases by five orders of magnitude from -40°C to 120°C. This increase reduces for larger gate voltages.

Ideally, the nominal gate voltage should be used for the temperature determination to achieve a high saturation current and low on-state resistance. From the perspective of curve fitting, the gate current method can be applied to all three devices at their nominal gate drive condition.

Degradation under Positive Gate Bias

In this work, the focus is on further exploring the methodology for temperature calibration by the Schottky gate leakage current, which is often implicating parameter deviations [11]. The degradation of the gate current during positive gate stress test is depending on the process technology, temperature and level of applied bias [11], [20]. Depending on the condition, the gate current either increases or decreases [20]. At high temperatures and high gate bias, a logarithmic increase of the gate current was observed [7]. At nominal gate voltage of V_{GS} = 6 V and temperature of 120°C, an increase by 13% is observed for the GaNSystems device (Figure 10). After 2 hours of continuous constant stress, I_{GSS} becomes almost stable.

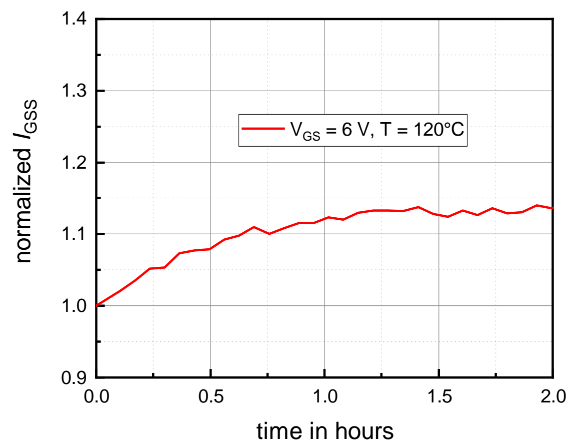

Figure 10: Course of the gate leakage current I_{GSS} for GaNSystems device at 120°C and 6 V over 2 hours

Calibration Routine and Parameter Deviations

Consequently, the temperature calibration itself can also introduce a drift at high temperature and constantly applied positive gate voltage. The temporal course of the applied temperature during the calibration is shown in Figure 11. During the calibration process, the gate voltage is only applied after the maximum temperature is reached. In power cycling tests, the initial maximum temperature is set at the limit of the datasheet and can increase by degradation of the device. Hence, the temperature calibration can exceed the maximum temperature ratings to cover the entire temperature range in the later test. After the devices reached 25°C in the calibration, the gate voltage is removed again. The devices stayed for less than 0.2 hours above 150°C. In order to monitor possible parameter deviation, a calibration and characterization flow was introduced for a comprehensible investigation (see Figure 12). A second, revised temperature calibration is introduced to verify the first temperature calibration.

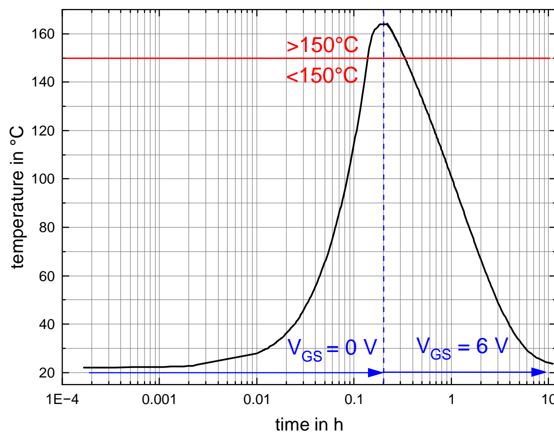

Figure 11: Temperature course with applied gate voltage and critical gate voltage

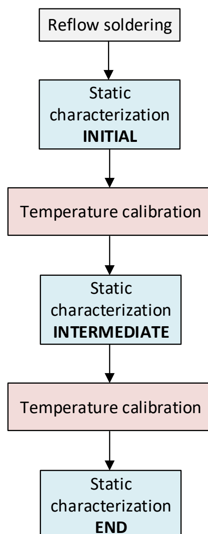

Figure 12: Flow of the temperature calibration and characterization

The described routine of the calibration was applied to all three types of devices. The parameters threshold voltage V_{Gth}, drain leakage current I_{DSS}, gate leakage current I_{GSS}, and on-state resistance R_{DSon} were monitored at initial, intermediate and end state. The results for GaNSystems are given in Figure 14. The first calibration introduces a shift of the static device parameters, but no significant further changes are visible due to the second calibration. The resulting temperature calibration curves are depicted in Figure 13. Except of one device (green), all obtained curves are very comparable. Moreover, the difference between the two calibrations is within measurement accuracy. Hence, the temperature calibration can be utilized to initialize the devices and the $I_G(T)$ method is applicable for GaNSystems. While the gate leakage increased by 22%, the threshold voltage decreased by approx. 24%. The latter corresponds to a maximum of 0.43V, which is within acceptable limits.

For the Innoscience and the EPC devices, further changes are present from first to the second stress by temperature calibration. In Figure 15, the gate leakage current of the Innoscience device increased further and only the R_{DSon} remained stable. The temperature determination by on-state resistance could be an alternative for this component, especially with such high R_{DSon} (350 mΩ). However, if degradation of the assembly and interconnection technology occurs, the calibration curve is only valid as long as an ideal chip sense contact is present.

In contrast to these results, a reduced gate leakage current was observed for the EPC devices (Figure 16). The threshold voltage and on-state resistance remained stable. With an on-state resistance of 1.8 mΩ, the latter is rather unsuited as TSEP. The stable threshold voltage indicates that the inverse barrier V_{SD} indeed might be the parameter of choice.

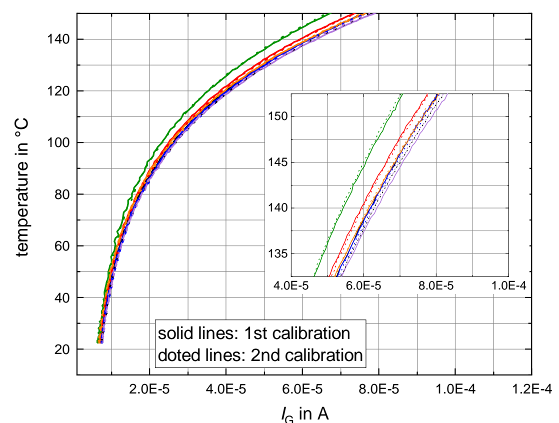

Figure 13: GaNSystems temperature dependent gate leakage current of six devices for two repeated calibrations at V_{GS} = 6 V

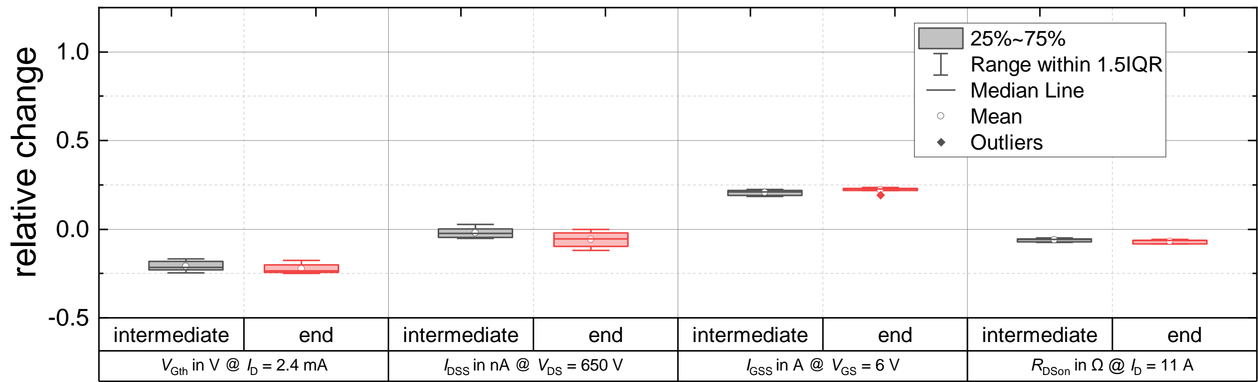

Figure 14: GaNSystems (6 devices) - relative change of parameters after the first and second calibration referred to the initial value

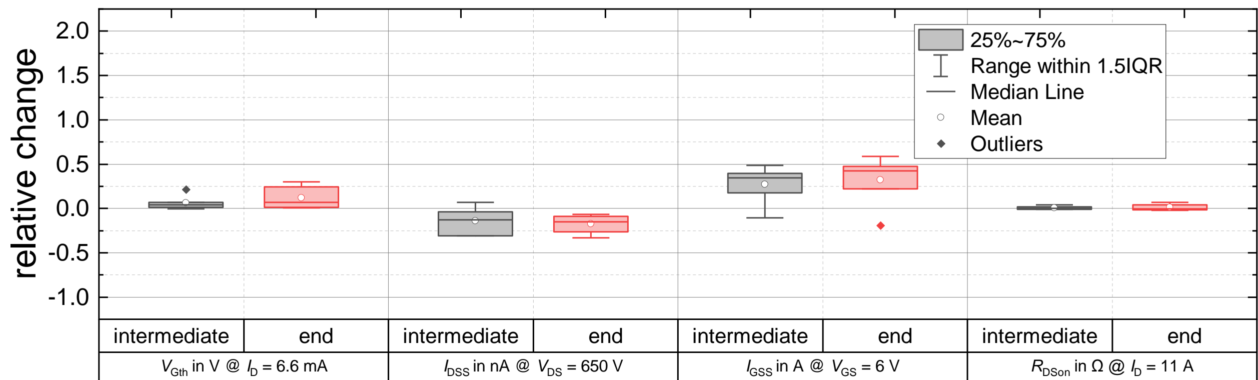

Figure 15: Innoscience (6 devices) - relative change of parameters after the first and second calibration referred to the initial value

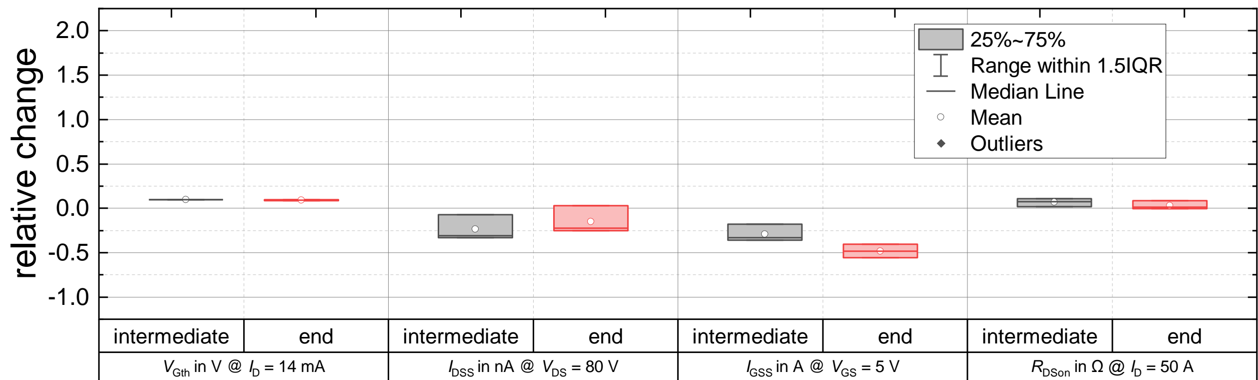

Figure 16: EPC (3 devices) - relative change of parameters after the first and second calibration referred to the initial value

CONCLUSION

The forward gate characteristic of Schottky p-GaN devices was characterized depending on temperature and gate voltage. The strong temperature dependency of the Schottky gate leakage current was pointed out.

During temperature calibration, shifts of device parameters are created under combined stress by gate voltage and temperature (similar effects could happen under power cycling). No universal, reliable parameter for temperature determination was found for GaN HEMTs. Already a temperature calibration can degrade and wear-in the components at once. The $I_G(T)$ method is applicable for GaNSystems devices. Further, potential TSEPs are the on-state resistance for the Innoscience device and the inverse barrier for the EPC device. Further investigations on the degradation of the Schottky gate GaN HEMTs are necessary. For the calibration, a pulsed method is recommended to reduce the gate stress during the calibration procedure. In order to assess the influence of degradation during the power cycling test a recalibration is recommended.

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