

Novel Constant Surface Concentration Depletion Mechanism and Its Experiments in Homogenization Field LDMOS

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Abstract

A novel constant surface concentration depletion (CSD) mechanism for the homogenization field (HOF) LDMOS is proposed and experimentally demonstrated in this paper. Because the depletion of the HOF LDMOS is independent on the P-substrate, the surface doping concentration of the HOF LDMOS can keep constant and thus the total doping dose of the N-drift region can increase with the junction and trench depths. Based on the CSD mechanism, a CSD HOF LDMOS with 15 μm trench depth was designed and experimentally fabricated. The doping dose of the N-drift region is increased up to $8 \times 10^{12} \text{ cm}^{-2}$. As a results, a measured low specific on-resistance $R_{\text{on,sp}}$ of $15.6 \text{ m}\Omega\text{-cm}^2$ was observed under a breakdown voltage V_B of 420 V, realizing a high figure of merit $\text{FOM} = V_B^2 / R_{\text{on,sp}}$ of 11.3 MW/cm^2 and a reduction of 53.3% compared with the theoretical limit of the triple RESURF technology under the same V_B . $R_{\text{on,sp}}$ of the CSD HOF LDMOS also realizes a reduction of 20.8% when compared with that of the best-in-class HOF LDMOS.

Keywords: Homogenization field, LDMOS, Breakdown voltage, Specific on-resistance, Constant surface concentration depletion

I. INTRODUCTION

To achieve higher breakdown voltage V_B and lower specific on-resistance $R_{\text{on,sp}}$, integrated power devices have been developed from the single reduced surface field (RESURF) to double and triple RESURF technologies [1]-[3]. Furthermore, the superjunction concept was introduced into the integrated devices to further enhance the doping concentration in the drift region and reduce $R_{\text{on,sp}}$ [4]-[9]. Drift regions of these devices are mainly depleted by PN junctions with charge balance between immobile positive and negative ionized charges. As a result, there exists a theoretically fixed optimized doping dose D_N for a given region, such as the well-known RESURF dose:

$$D_N = 1 \times 10^{12} \text{ cm}^{-2} \quad (1)$$

For the device formed through implantation annealing processes, the drift region exhibits a Gaussian distribution. It is revealed from (1) that D_N of the RESURF device is independent on the junction depth. Then, the surface doping concentration N_s of the device decreases with an increase in the depth of the doping junction. The different constant doping doses has also been discussed by both analytical models and experiments [8]-[11]. This phenomenon is referred to as constant dose depletion in this paper.

Recently, a new type of homogenization field (HOF) devices have been reported [12]-[14]. The HOF devices feature periodic MIS structures in the drift region to fully deplete the highly doped N-type region. Consequently, the depletion in the HOF device is relatively independent of the PN depletion, showing a self-charge balance by the discrete MIS arrays. However, the depletion mechanism of the HOF device has not been deeply researched, yet.

In this paper, a novel constant surface concentration depletion (CSD) mechanism for the HOF laterally diffused metal oxide semiconductor (LDMOS) is proposed and experimentally demonstrated. Section II gives the HOF structure and CSD mechanism. Section III presents experiments and discussions.

II. STRUCTURE AND MECHANISM

2.1 HOF Structure

The structure of the HOF LDMOS is shown in Fig. 1, which is characterized by the deep insertion of periodically discrete MIS trenches into the drift region. MIS trenches, located at an equal distance from the source end, are connected through surface metal

interconnects, forming a MIS depletion array that effectively depletes the entire drift region. The depletion region of the HOF structure is determined by the depth of the MIS trenches. As a result, the depletion mechanism of the HOF device is different from that of the conventional (Con) LDMOS.

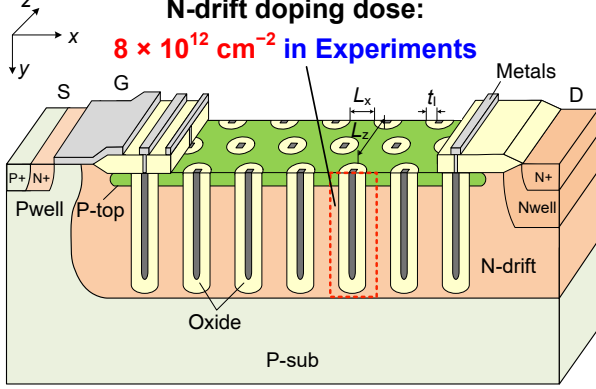


Fig. 1 Structure of CSD HOF LDMOS. The periodic discrete MIS trenches are introduced deep into the drift region to form the constant surface concentration depletion. A high D_N up to $8 \times 10^{12} \text{ cm}^{-2}$ was demonstrated in experiments.

2.2 CSD Mechanism

Since the depletion of the drift region in HOF devices is independent of the P-substrate and primarily depends on the trench depth, a deeper trench enables the depletion in deeper region into the device. Under a Gaussian distribution, a constant surface doping concentration N_s can be maintained while increasing the depth of the junction in the drift region, i.e., increasing the standard deviation σ , thus achieving a continuously increased D_N . The CSD mechanism is shown in Fig. 2.

Fig. 2(a) presents the schematic diagram of the CSD mechanism based on 3-D MIS assisted depletion. The constant N_s in the HOF LDMOS is maintained, while the D_N is increased as the junction depth of the N-drift and trench depth increase. The analytical model for the HOF device has been reported in [12]. The design formula for N_s is as follows:

$$\frac{\varepsilon_s E_c}{qT} \tanh\left(\frac{L_x}{2T}\right) \leq N_s \leq \frac{\varepsilon_s E_c}{qT} \quad (2)$$

where ε_s is the dielectric constant of the silicon and q is the electron charge. L_x is the distance between trenches in the x -direction. E_c and T are the critical electric field and characteristic thickness that can be calculated by:

$$\begin{cases} T = \sqrt{\frac{L_z^2}{8} + \frac{\varepsilon_s}{2\varepsilon_l} t_l L_z} \\ E_c = 6.645 \exp(1.636 L_d^{-0.1269}) \end{cases} \quad \text{with } L_z, L_d, t_l \text{ and } \varepsilon_l \text{ being}$$

the distance between trenches in the z -direction, the drift region length, the thickness and dielectric constant of the

oxide. Under the Gaussian doping distribution, D_N can be obtained by integrating the doping concentration in the y -direction of the drift region as follows:

$$D_N = \int_0^\infty N_s \exp\left(-\frac{y^2}{2\sigma^2}\right) dy = \sqrt{\frac{\pi}{2}} N_s \sigma \quad (3)$$

D_N of the HOF device increases monotonically with the junction depth or σ , with $D_N \propto \sigma$. Then, D_N of the HOF device can be significantly increased to reduce $R_{\text{on,sp}}$. In contrast to this, the Con device based on 1-D substrate assisted depletion, with $D_N \approx \text{constant}$, cannot introduce more conduction carriers by increasing the junction depth alone, as shown in Fig. 2(b).

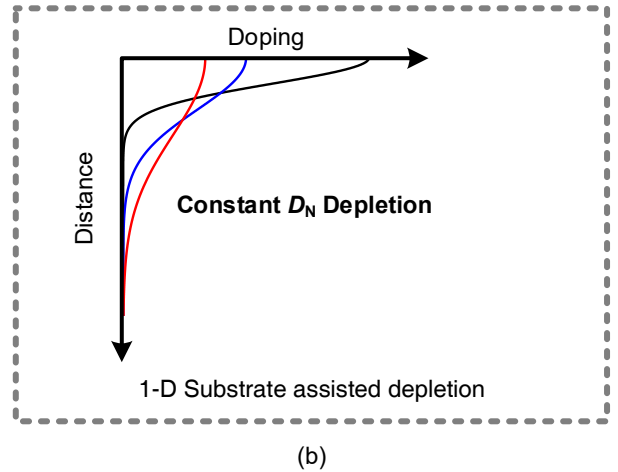
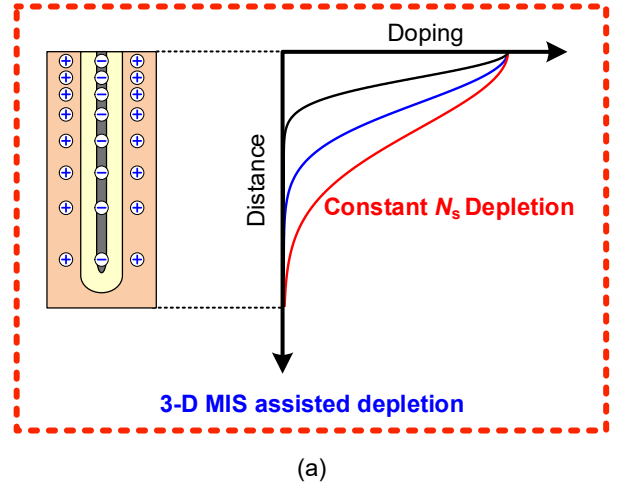


Fig. 2(a) CSD mechanism of the constant N_s depletion. N_s of the HOF LDMOS can keep a constant and the D_N is increased with the increases of the junction depth of the N-drift and trench depth; (b) The constant D_N depletion in the Con RESURF LDMOS with increase junction depth and reduced N_s .

III. DESIGN AND EXPERIMENTS

3.1 Design of CSD HOF LDMOS

Design formula (3) provides a very simple guideline for the HOF devices, where improving device characteristics can be achieved by simply increasing the junction and trench depths in the drift region. Compared with our previous work [14], the trench depth is increased from 12 μm to 15 μm and the corresponding D_N is increased from $6.8 \times 10^{12} \text{ cm}^{-2}$ to $8 \times 10^{12} \text{ cm}^{-2}$. Based on the CSD mechanism, it is possible to achieve a predictable decrease in $R_{\text{on,sp}}$ while maintaining a constant V_B .

Fig. 3 compares the equipotential line distributions of CSD HOF LDMOS and Con LDMOS at breakdown. In the CSD HOF LDMOS device, the drift region is fully depleted by the MIS deep trench, resulting in a uniform distribution of the equipotential lines throughout the device. In contrast, the Con LDMOS exhibits an obvious neutral region, which leads to premature breakdown at the source end of the device.

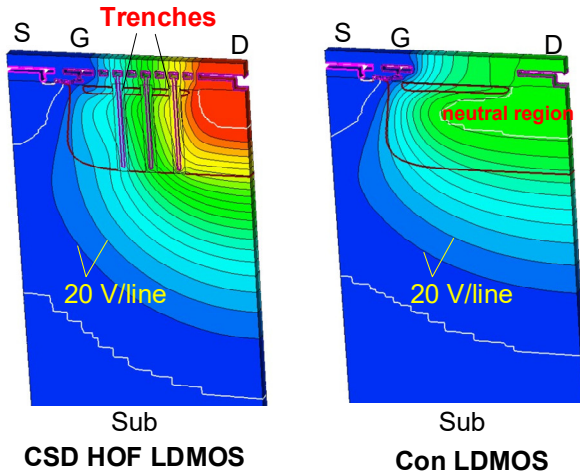


Fig. 3 Equal-potential lines of CSD HOF LDMOS and Con LDMOS. The drift region of the HOF LDMOS is fully depleted because of the CSD mechanism and an obvious neutral region is observed in the Con LDMOS.

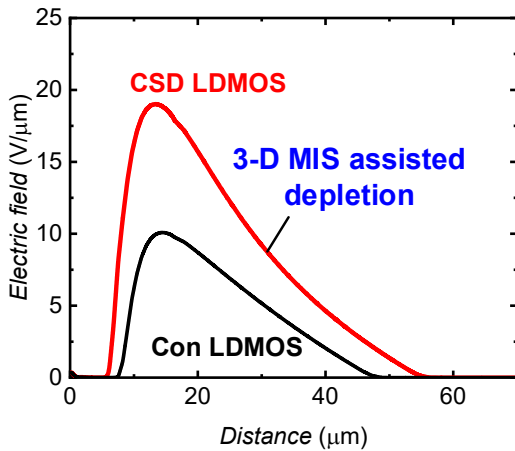


Fig. 4 Vertical electric field distributions of CSD HOF LDMOS and Con LDMOS. The peak field of the CSD HOF LDMOS is increased from 10 $\text{V}/\mu\text{m}$ of the Con LDMOS to 20 $\text{V}/\mu\text{m}$ by the 3-D MIS assisted depletion.

Fig. 4 compares the electric field distributions under the drain of CSD HOF LDMOS and Con LDMOS. The CSD HOF LDMOS demonstrates a peak electric field of 20 $\text{V}/\mu\text{m}$ because of the 3-D MIS assisted depletion. In contrast, the vertical electric field of the Con LDMOS is limited to 10 $\text{V}/\mu\text{m}$ due to the premature breakdown at the surface. Compared with the Con LDMOS, the simulated V_B of CSD HOF LDMOS is increased from 212 V to 439 V, showing a significant 107% improvement, as illustrated in Fig. 5.

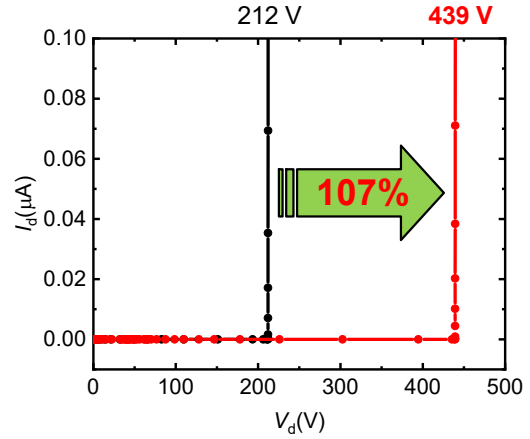


Fig. 5 Simulated V_B of CSD HOF LDMOS and Con LDMOS. V_B of the CSD HOF LDMOS is increased by 107% when compared with that of the Con LDMOS.

3.2 Experiments of CSD HOF LDMOS

Based on the 0.5 μm Central Semiconductor Manufacturing Corporation (CSMC) process platform, a CSD HOF LDMOS was fabricated. Fig. 6 presents the micro photo and layout of the drift region for the CSD HOF LDMOS, featuring the introduction of 7 trench arrays in the drift region. In comparison to the device in [14], the HOF device designed using the CSD mechanism incorporates 15 μm deeper trenches to deplete a higher D_N of $8 \times 10^{12} \text{ cm}^{-2}$.

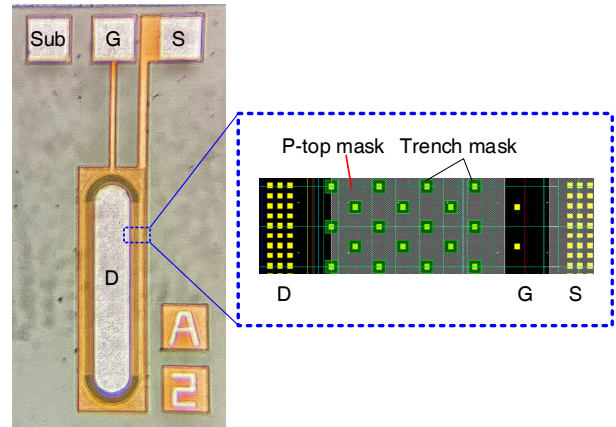


Fig. 6 Micro photo and layout of CSD HOF LDMOS. Deep trenches of 15 μm were formed in the drift region with 7 trench arrays.

Fig. 7 illustrates the measured $I_d - V_d$ curves of the CSD HOF LDMOS device in the off-state and on-state. The testing results reveal a V_B of 420 V and an $R_{on,sp}$ of $15.6 \text{ m}\Omega \cdot \text{cm}^2$. This achievement corresponds to a high figure of merit FOM of $11.3 \text{ MW}/\text{cm}^2$, calculated using the formula $FOM = V_B^2 / R_{on,sp}$.

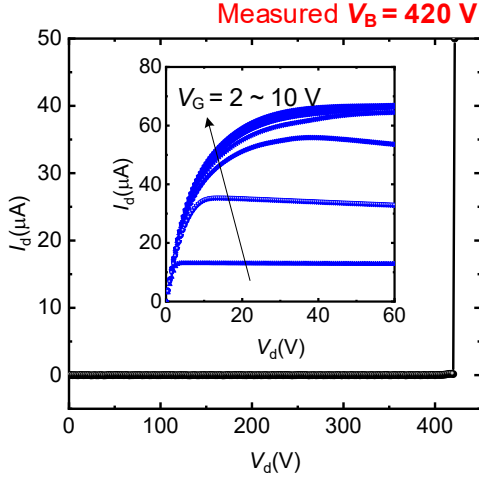


Fig. 7 Measured off-state and on-state $I_d - V_d$ lines. The measured low $R_{on,sp}$ of $15.6 \text{ m}\Omega \cdot \text{cm}^2$ was observed under a V_B of 420 V, realizing a high $FOM = V_B^2 / R_{on,sp}$ of $11.3 \text{ MW}/\text{cm}^2$.

Fig. 8 compares the measured $R_{on,sp} - V_B$ characteristics of the CSD HOF LDMOS and other reported devices [3]-[8], [14]-[15] in a logarithmic scale. The $R_{on,sp}$ characteristic of the CSD HOF LDMOS is better than those of the recently reported devices, exhibiting a 20.8% improvement over the best-in-class $R_{on,sp}$ of the previously reported HOF device [14] while maintaining the same V_B . Furthermore, this achievement signifies a remarkable reduction of 53.3% compared with the theoretical limit achievable with the triple RESURF technology [3] at the same V_B .

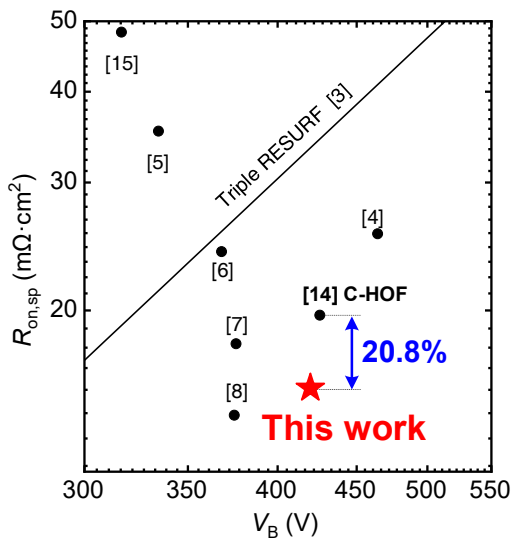


Fig. 8 $R_{on,sp} - V_B$ characteristics of the CSD HOF LDMOS and reported experiments [3]-[8], [14]-[15]. The CSD HOF LDMOS realizes a $R_{on,sp}$ reduced by 20.8% when compared with the HOF LDMOS we reported in [14].

IV. CONCLUSION

This paper proposed and experimentally demonstrated the new CSD mechanism for HOF devices. Compared with the conventional constant D_N depletion mechanism in PN junction depleted devices, the HOF device achieved complete MIS-assisted depletion in the drift region, allowing for a constant surface concentration depletion. By increasing the junction and trench depths, the doping dose of the N-drift region was increased up to $8 \times 10^{12} \text{ cm}^{-2}$. This resulted in a $R_{on,sp}$ of $15.6 \text{ m}\Omega \cdot \text{cm}^2$, measured at a V_B of 420 V. Consequently, the CSD HOF device achieved a high FOM of $11.3 \text{ MW}/\text{cm}^2$ and a remarkable 53.3% reduction compared with the theoretical limit of triple RESURF technology at the same V_B . Additionally, the CSD HOF LDMOS demonstrated a 20.8% reduction in $R_{on,sp}$ compared with the best-in-class HOF LDMOS. The CSD mechanism presented a simple and feasible approach for improving the characteristics of HOF devices.

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REFERENCES

- [1] Disney, D.R., Paul, A.K., Darwish, M., Basecki, R. and Rumennik, V.: A new 800 V lateral MOSFET with dual conduction paths, Proc. ISPSD'01 (Osaka, 2001), 399-402
- [2] Hossain, Z., Imam, M., Fulton, J. and Tanaka, M.: Double-RESURF 700 V n-channel LDMOS with best-in-class on-resistance, Proc. ISPSD'02 (Sante Fe, 2002), 137-140
- [3] Iqbal, M.M.-H., Udrea, F. and Napoli, E.: On the static performance of the RESURF LDMOSFETS for power ICs, Proc. ISPSD'09 (Barcelona, 2009), 247-250
- [4] Zhang, W. et al: Optimization and experiments of lateral semi-superjunction device based on normalized current-carrying capability, IEEE Electron Device Letters, **40**, 2019, 1969-1972
- [5] Lin, M.-J., Lee, T.-H., Chang, F.-L., Liaw, C.-W. and Cheng, H.-C.: Lateral superjunction reduced surface field structure for the optimization of breakdown and conduction characteristics in a high-voltage lateral double diffused metal oxide field effect transistor, Jpn. J. Appl. Phys., **42**, 2003, 7227-7231
- [6] Duan, B., Cao, Z., Yuan, X., Yuan, S. and Yang, Y.: New superjunction LDMOS breaking silicon limit by electric field

modulation of buffered step doping, IEEE Electron Device Letters, **36**, 2015, 47-49

[7] Duan, B., Cao, Z., Yuan, S. and Yang, Y.: Complete 3D-reduced surface field superjunction lateral double-diffused MOSFET breaking silicon limit, IEEE Electron Device Letters, **36**, 2015, 1348–1350

[8] Antoniou, M., Udrea, F., Tee, E.K.C. and Hölke, A.: High-Voltage 3-D Partial SOI Technology Platform for Power Integrated Circuits, IEEE Transactions on Electron Devices, **69**, 2022, 3296-3301

[9] Udrea, F., Deboy, G. and Fujihira, T.: Superjunction Power Devices, History, Development, and Future Prospects, IEEE Transactions on Electron Devices, **64**, 2017, 713-727

[10] Zhang, W. et al: Optimization of Lateral Superjunction Based on the Minimum Specific ON-Resistance, IEEE Transactions on Electron Devices, **63**, 2016, 1984-1990

[11] Nassif-Khalil, S.G., Li Zhang Hou and Salama, C.A.T.: SJ/RESURF LDMOST, IEEE Transactions on Electron Devices, **51**, 2004, 1185-1191

[12] Zhang, W. et al: Analytical model and mechanism of homogenization field for lateral power devices, IEEE Transactions on Electron Devices, **68**, 2021, 3956-3962

[13] Zhang, W. et al: Experiments of homogenization field LDMOS with trench-stopped depletion, IEEE Transactions on Electron Devices, **69**, 2022, 2528-2533

[14] Zhang, W. et al: Experiments of a lateral power device with complementary homogenization field structure, IEEE Electron Device Letters, **42**, 2021, 1638-1641

[15] Honarkhah, S., Nassif-Khalil, S. and Salama, C.A.T.: Back-etched super-junction LDMOST on SOI, Proc. ESSCIRC'04 (Leuven, 2004), 117-120

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