

Comparison of IGBT Junction Temperature Determination using an On-Chip Sensor and the $V_{CE}(T)$ Method

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Abstract

This paper investigates the factors responsible for the differences in the IGBT virtual junction temperature $T_{vj,max}$ determined using the established $V_{CE}(T)$ method and the temperature recorded using an on-chip temperature sensor (T_j sensor) mounted in the centre area of the IGBT chip. The impact of each of the influential factors are quantified using experimental and analytical methods. Increase in power loss density was found to cause an increase in the difference between the two temperatures at a rate of 2 Kelvin per W/mm^2 as per measurement results. The selection of the measurement delay was found to additionally contribute to the deviation between the estimated $T_{vj,max}$ by the two methods in the range of a few Kelvin. Furthermore, increase in thermal resistance contributes to an increase in the deviation. By adding several influential factors, an impact of up to 50% difference in power cycling lifetime estimation is possible depending upon the operating conditions.

Keywords: IGBT Junction Temperature, T_j sensor, Power Cycling, On-Chip temperature sensor.

INTRODUCTION

Accurately determining the IGBT junction temperature is an essential precondition for establishing an accurate load cycling lifetime model as well as for defining parameters such as those required for setting the over temperature protection function. The junction temperature of the IGBT (T_j) can be determined using several methods which chiefly fall under two major categories – indirect measurement and direct measurement. Indirect measurement methods refer to the utilization of temperature sensitive electrical parameters (TSEP) for estimating the junction temperature. Several TSEPs exist [1] and each TSEP presents an opportunity to estimate the IGBT junction temperature. The $V_{CE}(T)$ method [2] is one such indirect method which is standard for T_j estimation especially for the purpose of life time estimation. Direct T_j determination refers to methods where temperature as the input parameter is acquired directly from the IGBT chip. One such direct measurement method is to utilize an on-chip temperature sensor (T_j sensor) which is integrated in the centre area of the chip [3]. An example of one such IGBT chip is shown

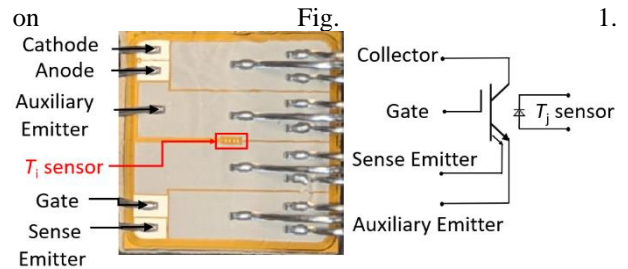


Figure 1: The IGBT die with the T_j sensor

As evident in the IR camera image in Fig. 2, when the IGBT chip (in healthy condition) conducts current, there is a lateral temperature gradient over the chip. The hotspot is located on the centre of the chip and the periphery is cooler. According to the automotive qualification guideline AQG324 the temperature registered using the $V_{CE}(T)$ method is the so-called virtual junction temperature (T_{vj}). In this paper, the maximum temperature determined through an on-chip sensing diode will be referred to as hotspot temperature $T_{hotspot}$ and the maximum temperature determined through $V_{CE}(T)$ method will be called maximum virtual junction temperature $T_{vj,max-VCE}$. The difference between the two is an indication of the overall temperature gradient on the chip and will be called $T_{difference}$.

$$T_{difference} = T_{hotspot} - T_{vj,max-VCE} \quad (1)$$

In this study, the experiments were conducted where either the thermal resistance from junction to ambient ($R_{th,j-a}$) was measured or the thermal resistance from junction to heatsink ($R_{th,j-s}$) was measured. The measured

quantities are described accordingly. Unless otherwise mentioned, the junction temperature for the thermal resistance measurement uses the standard $V_{CE}(T)$ method.

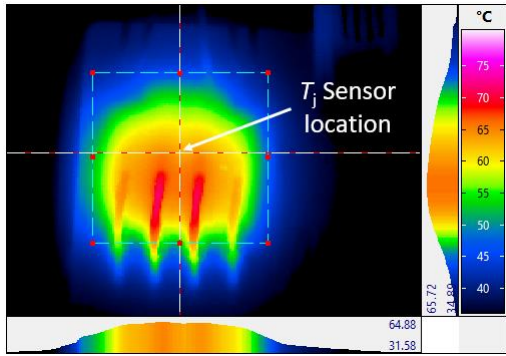


Figure 2: IR Camera image of the DUT. $I_c = 100$ A, $t_{on} = 5$ s.

The typical profiles and location of these temperatures are shown in Fig. 3.

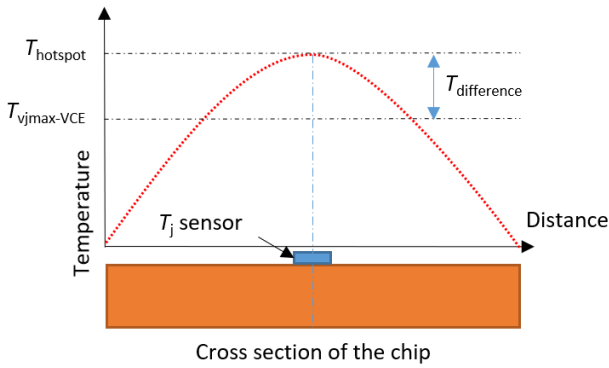


Figure 3: An example of the temperature profile over the chip

The study in [4] has analysed the suitability of the T_j sensor for determining the T_j during power cycling tests. This paper analyses the differences between the IGBT junction temperature established using the $V_{CE}(T)$ method and the T_j sensor method. The motivation is to understand the utility of the T_j sensor method as a means to achieve on-line monitoring of the T_j and to understand the impact of using the T_j sensor method in estimating load cycling lifetime. In power cycling tests, the maximum virtual junction temperature is measured using a TSEP method such as the $V_{CE}(T)$ method and is considered as an important stressing factor. However, the sensing diode integrated on the IGBT chip only determines the hotspot temperature (at the centre of the chip). It is therefore important to determine how these two temperatures compare and which parameters influence their difference. Three important parameters are identified and analysed in this paper: power density (P_V), overall thermal resistance ($R_{th,j-a}$) and delay time (t_{md}) in the $V_{CE}(T)$ measurement method. The absolute value of $T_{difference}$ is found to increase with increasing P_V , $R_{th,j-a}$ and t_{md} . The first part of this paper introduces the two junction temperature measurement approaches and highlights the fundamental differences between them. The second part presents the measurement results and

analysis of the dependency of $T_{difference}$ with the above mentioned parameters.

TEMPERATURE CALIBRATION AND KEY DIFFERENCES BETWEEN THE T_j SENSOR AND THE $V_{CE}(T)$ METHOD

Calibration using the on-chip temperature sensor

The on-chip temperature sensor (T_j sensor) consists of a series of diodes manufactured/processed on the top surface (emitter side) of the IGBT die. As seen in Fig 1, the T_j sensor is located in the centre area of the IGBT chip. The forward characteristics of this string of sense diodes was measured at different temperatures for sense current currents in the range of $1 \mu A$ to $300 \mu A$.

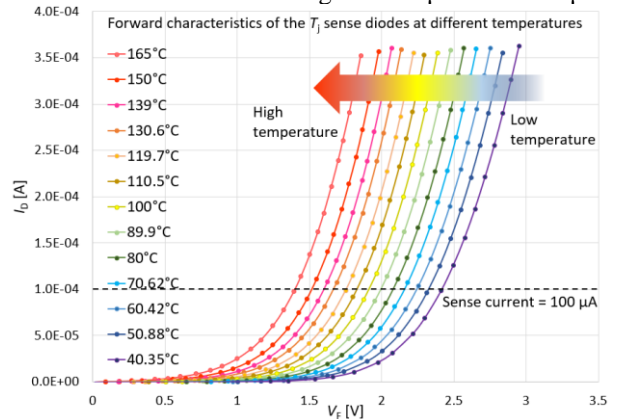


Figure 4: Forward characteristics of the T_j sense diodes at different temperatures

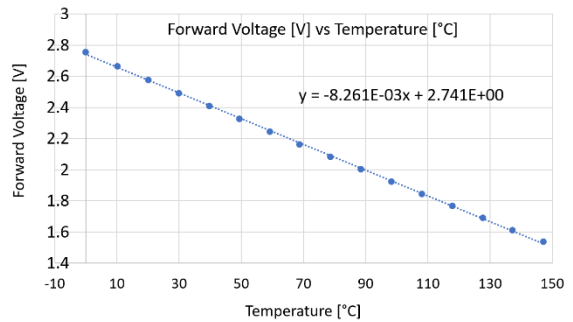


Figure 5: Calibration of the T_j sensor

As evident from Fig. 4, the T_j sensor has a negative temperature coefficient. A sense current has to be selected for measurement. At high sense currents, the impact due to self-heating of the sense diodes will be higher. At low sense currents, the impact due to noise in the measured signal will be higher. A sense current of $100 \mu A$ was selected and the T_j sensor has been calibrated at 16 points between $0^\circ C$ and $150^\circ C$. As seen in Fig. 5, a first order linear interpolation of the forward voltage versus temperature reveals a slope of about -8.26 mV/K.

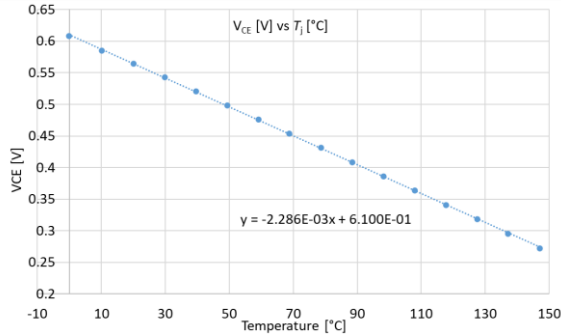


Figure 6: Calibration of the DUT using $V_{CE}(T)$ method

Differences in measurement method: T_j sensor method and $V_{CE}(T)$ method

Established guidelines for calibration and measurement using the $V_{CE}(T)$ method are available in [2] and [5]. The DUT which is a 1200 V/ 150 A (single die) IGBT was calibrated using a 100 mA sense current. A first order linear interpolation of the forward voltage versus temperature reveals a slope of about 2.28 mV/K (refer Fig. 6). The following are some key differences between the T_j sensor and the $V_{CE}(T)$ method:

1. **Nature of data acquired** – the data acquired by the T_j sensor method corresponds to the local temperature at the centre of the chip where the T_j sense diodes are located. On the other hand, the $V_{CE}(T)$ method uses the IGBT chip itself as a temperature sensor and as described in [2] the data acquired are close to the area related average temperature of the IGBT chip.
2. **Sensitivity and temperature resolution** – the calibration curves of the T_j sensor and the $V_{CE}(T)$ method indicate that the T_j sensor has about 4 times higher temperature sensitivity or temperature resolution for a given probe sensitivity.

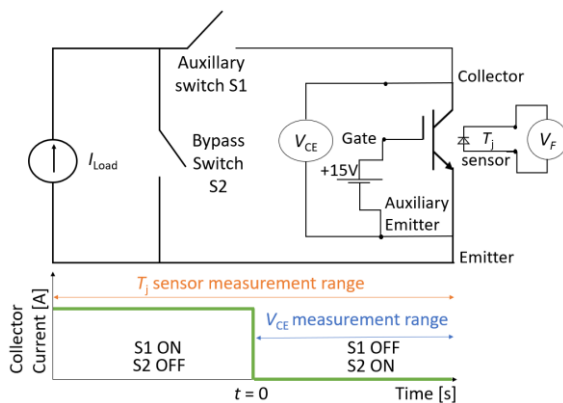


Figure 7: $V_{CE}(T)$ and T_j sensor measurement setup.

3. **Online temperature monitoring** – the $V_{CE}(T)$ method is not suitable for online temperature monitoring as the collector-emitter voltage drop is measured using the sense current after the load current has been cut-off. There exists a certain minimum recombination time of the carriers in the IGBT chip after the collector current of the IGBT has

been passively turned off [6]. Therefore, a certain measurement delay (t_{md}) is maintained after the turn-off of the collector current through the IGBT. For the T_j sensor method, the temperature measurement method is decoupled from the electrical path of the chip as the anode and cathode terminals of the sense diodes are isolated from the terminals of the IGBT. Therefore, data from the T_j sensor is available for online monitoring. Fig. 7 shows the test setup for IGBT junction temperature measurement using the T_j sensor as well as using the $V_{CE}(T)$ method (load current turned off at $t = 0$ s, $t_{md} = 300 \mu\text{s}$ for $V_{CE}(T)$ data). The results are shown in Fig. 8.

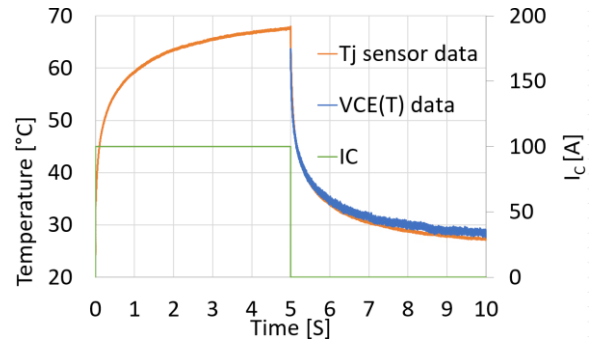


Figure 8: T_j sensor and $V_{CE}(T)$ data. $I_c = 100$ A and $t_{on} = 5$ s.

MEASUREMENT RESULTS AND ANALYSIS OF DEPENDENCIES

Motivation for estimation of $T_{vj,max}$: Power cycling lifetime models for IGBT modules can be expressed in terms of number of cycles (N_f) versus the junction temperature ripple ΔT_j [7] as proven by statistical analysis shown in [8]. Fig. 9 is an example of the power cycling lifetime model as per [8].

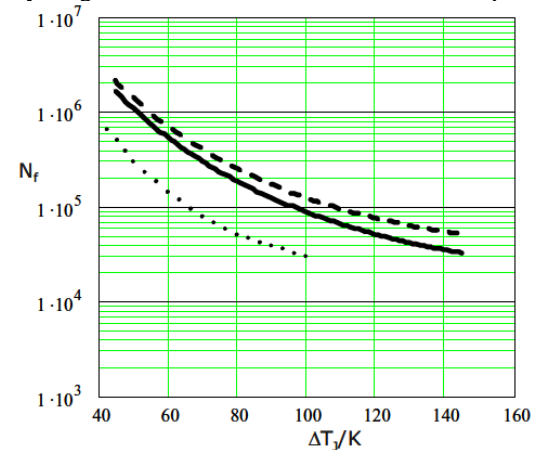


Figure 9: $N_f - \Delta T_j$ curves from the CIPS'08 model [8]. Lower dotted trace: former curve (LESIT model) of modules for industrial application at $T_{j,max} = 125^\circ\text{C}$. Solid line: Estimated N_f according to a new model for modules with IGBT4/1200V at $T_{j,max} = 150^\circ\text{C}$, $t_{on} = 1.5$ s, $I = 10$ A; dashed line – same as solid line but $T_{j,max} = 125^\circ\text{C}$.

Since the junction temperature ripple ΔT_j is the difference between the maximum ($T_{j,max}$) and minimum junction temperatures ($T_{j,min}$), determination of the maximum junction temperature analysis assumes a significant role in power lifetime analysis of IGBT modules.

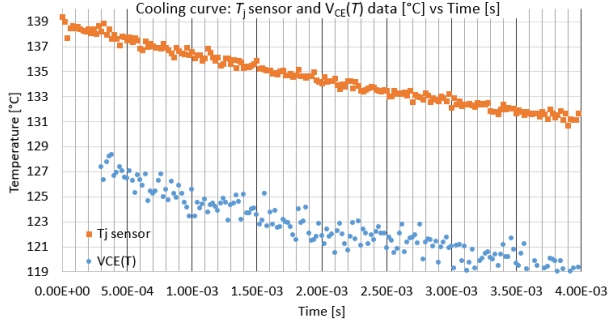


Figure 10: Plot of $V_{CE}(T)$ and T_j sensor data using $I_C = 200$ A, $t_{on} = 5$ s, $t_{md} = 300$ μ s. Total chip area = 134. 56 mm². Power dissipated per unit area (active area) P_V/A during heating = 3.53 W/mm².

$T_{j,max}$ estimation method: Fig. 10 is an example for the maximum junction temperature determination using the T_j sensor and the $V_{CE}(T)$ method. In this experiment, a collector current I_C of 200 A was applied for 5 s. A difference of about 11 Kelvin is seen in the maximum temperatures measured using the T_j sensor versus the $V_{CE}(T)$ method. The DUT utilised for this study is a 1200 V/ 150 A IGBT chip which is packaged in an IGBT module. The cross section of the IGBT module is represented in Fig. 11. The IGBT chip is mounted on a ceramic substrate which is soldered to a copper baseplate. The IGBT module is mounted on a water cooled heatsink via thermal grease.

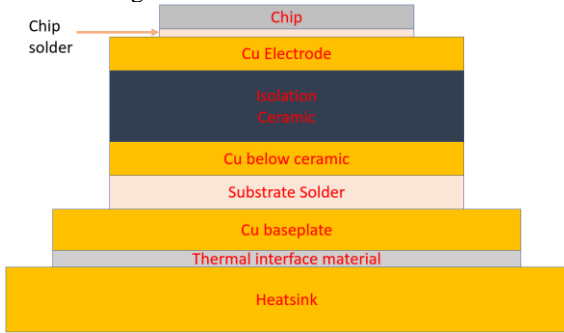


Figure 11: Cross section of the power module

Factors influencing the $T_{difference}$: The $T_{difference}$ can be resolved into two time-dependent spatial components: $T_{difference} = \text{Lateral temperature gradient } (t) + \text{Vertical temperature gradient } (t)$

The lateral and vertical temperature gradients depend upon the input parameters such as power density (P_V), overall thermal resistance ($R_{th,j-a}$) and delay time (t_{md}) in $V_{CE}(T)$ measurement method. Additionally, the thickness of the chip influences the vertical temperature gradient and therefore the $T_{difference}$. Fig. 12 represents the relationship between the key factors and $T_{difference}$.

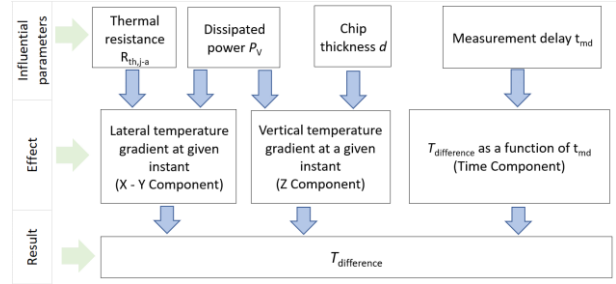


Figure 12: Summary of factors influencing $T_{difference}$

Interrelationship between P_V , T_j and $R_{th,j-a}$: The rise in junction temperature from ambient ΔT_{j-a} depends on the dissipated power (P_V) and the thermal resistance from junction to ambient ($R_{th,j-a}$).

$$\Delta T_{j-a} = P_V \cdot R_{th,j-a} \quad (2)$$

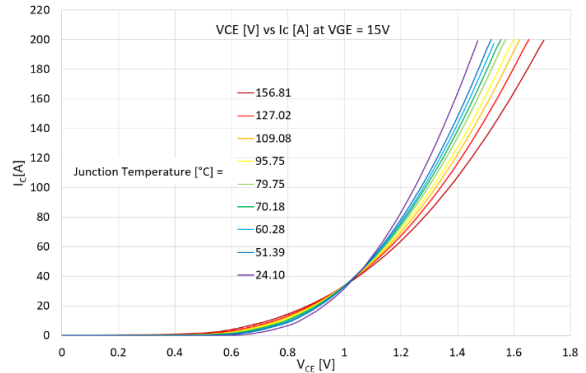


Figure 13: V_{CE} versus I_C of the DUT at different temperatures showing positive temperature coefficient of the DUT above the temperature compensation point (TCP) which is 38 A.

In order to study the impact of P_V and $R_{th,j-a}$, the interdependency of these two parameters must be understood. As per (2), when the P_V of the DUT is increased (for example by increasing the I_C), the ΔT_{j-a} of the DUT must increase resulting in the increase of the absolute T_j of the DUT.

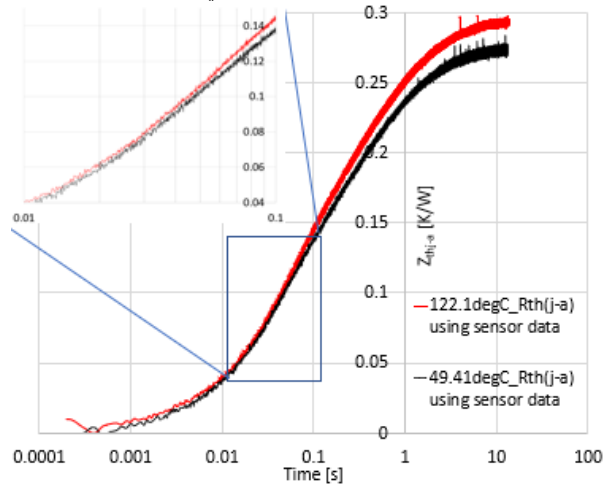


Figure 14: Measurement of $Z_{th,j-a}$ using T_j sensor data and different heatsink temperatures. $I_C = 38$ A (TCP).

The R_{th} of the constituents of the IGBT module has a positive temperature coefficient [6]. As a result, overall $R_{th,j-a}$ increases when the absolute temperature increases. On the other hand, higher $R_{th,j-a}$ leads to higher ΔT_{j-a} and

results in an increase of the absolute T_j of the DUT. Since the IGBT has a positive temperature coefficient as seen in Fig. 13, the P_V is expected to increase for any given I_C . In order to confirm the temperature dependency of the $R_{th,j-a}$, an experiment was conducted at the TCP of the DUT ($I_C = 38$ A) by setting the heatsink to different temperatures. At the TCP, the power loss of the chip does not depend on the applied temperature, so the resulting $R_{th,j-a}$ is purely a function of the temperature coefficient of the constituents of the IGBT module. In this experiment, the data from the T_j sensor was utilised. The ΔT_{j-a} and the $Z_{th,j-a}$ were calculated accordingly. As it can be seen from Fig. 14, the overall $R_{th,j-a}$ increases with increase in temperature. Additionally, the deviation starts at the time domain between 0.01 s and 0.1 s which generally corresponds to the R_{th} variation of the chip solder plus substrate layers. An FEM simulation with ANSYS was conducted using a model of the DUT to understand the impact of the R_{th} variation of only the substrate isolation sheet. The thermal conductivity of the isolation ceramic layer was varied and the $Z_{th,j-a}$ was plotted using the maximum junction temperature. Fig. 15 confirms that when the thermal conductivity of the substrate layer is modified, a variation is expected in the time domain between 0.01 s and 0.1 s.

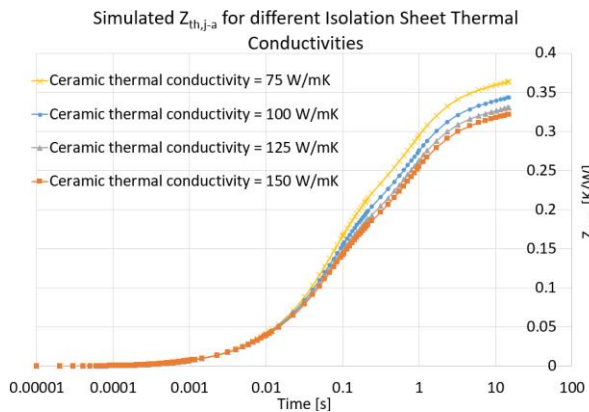


Figure 15: Simulated $Z_{th,j-a}$ for different thermal conductivities of the isolation sheet.

In Fig. 16, the $Z_{th,j-s}$ has been plotted utilising the T_j sensor data and the heatsink temperature data to confirm the hypothesis that when the P_V increases, the T_j increases and as a result the $R_{th,j-s}$ of the power module increases.

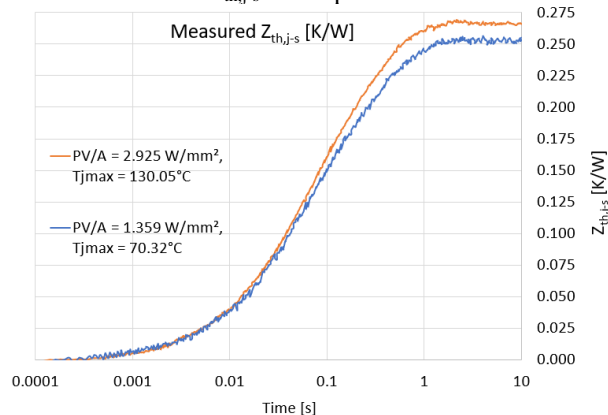


Figure 16: Measured $Z_{th,j-s}$ for different P_V/A using T_j sensor data

A summary of the relationship between the P_V and the $R_{th,j-a}$ is presented in Fig. 17.

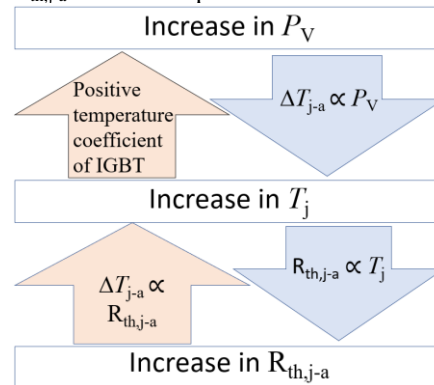


Figure 17: A summary of the interrelationship between P_V , T_j and $R_{th,j-a}$

Impact of dissipated power P_V on $T_{difference}$

For a given absolute value of P_V , the $T_{difference}$ also depends on the active area (A) of the chip. Therefore, the parameter to be considered for this analysis is the power density P_V/A in W/mm^2 . A measurement was conducted where the I_C through the DUT was increased in steps to increase the P_V/A . As explained via Fig. 17, the $R_{th,j-s}$ (thermal resistance to sink) of the system is expected to have a positive correlation with P_V/A . The $T_{hotspot}$ was the highest temperature occurring immediately at turn-off of I_C and T_{vj,max_VCE} was acquired for different t_{md} . The measurements were repeated with different thermal interface materials to obtain different $R_{th,j-s}$ of the set-up. The $T_{difference}$ has been plotted for points having similar $R_{th,j-s}$ and same t_{md} .

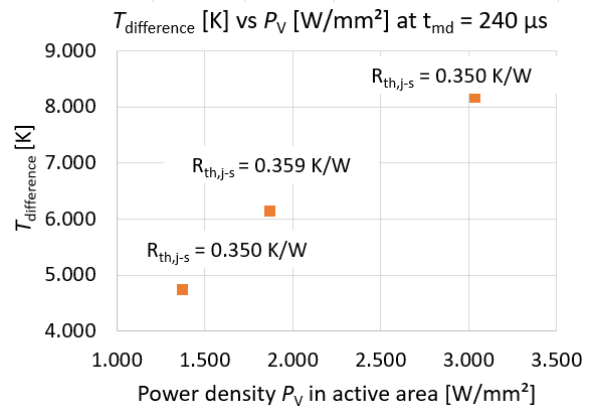


Figure 18: $T_{difference}$ versus P_V/A for points having similar $R_{th,j-s}$

Referring to Fig. 18, at $R_{th,j-s} = 0.35$ K/W, the analysis shows a slope of about 2 Kelvin increase for an increase of 1 W/mm^2 .

Impact of thermal resistance $R_{th,j-a}$

While (2) is true for the overall ΔT_{j-a} , the difference between the $T_{hotspot}$ and the T_{vj,max_VCE} is to be analysed with respect to the effective $R_{th,j-a}$. Measurements were conducted where the thermal interface material between the power module and the heatsink was modified in 3 steps. In this experiment, the $R_{th,j-s}$ was measured. At each

step, the $T_{\text{difference}}$ was registered for different t_{md} . The initial measurements were conducted using a thermal grease as the thermal interface material. By adding one layer of a thermally conductive foil, the overall $R_{\text{th},j-s}$ increased by about 42% and by placing two layers of the same thermally conductive foil, the overall $R_{\text{th},j-s}$ increased by about 66%. Fig. 19 shows the $T_{\text{difference}}$ versus $R_{\text{th},j-s}$ for different t_{md} at similar P_V/A .

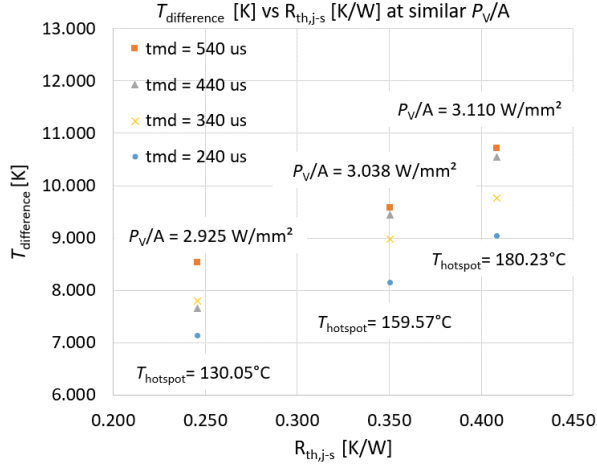


Figure 19: A plot of $T_{\text{difference}}$ versus $R_{\text{th},j-s}$ for similar P_V/A and various t_{md}

As per the results seen in Fig. 19, a positive correlation of $T_{\text{difference}}$ versus $R_{\text{th},j-s}$ is established. Additionally, an FEM simulation with ANSYS using the mechanical model similar to that of the DUT was conducted. The R_{th} of the TIM in the simulation was modified and its impact was analysed. The explanation for the positive correlation observed in Fig. 19 is as follows:

1. The higher R_{th} of the TIM impacts the R_{th} not only in the vertical direction (Z direction - from junction to heatsink), but also on the lateral (X-Y) plane affecting the temperature profile. This hypothesis has been verified using an FEM simulation with ANSYS where the thermal resistance of the TIM was changed and the difference between the maximum temperature and the average temperature on the surface of the chip was measured (Fig. 20). However, the effect is not too big.
2. As observed in Fig. 14, the R_{th} of the interconnections is temperature dependent. Fig. 21 shows the thermal profile in the cross section of the module. Fig. 22 shows the temperature profile on the substrate isolation layer. A lateral temperature profile exists on the interconnections such as the substrate. The result is a higher thermal resistance directly below the centre of the chip versus the periphery of the chip.

The FEM simulation does not include the temperature coefficient of R_{th} of the materials. Additionally, the simulation does not consider the positive temperature coefficient of IGBT power loss since this is not easy to implement in ANSYS. The simulation results in Fig. 20

are based on a simplified model.

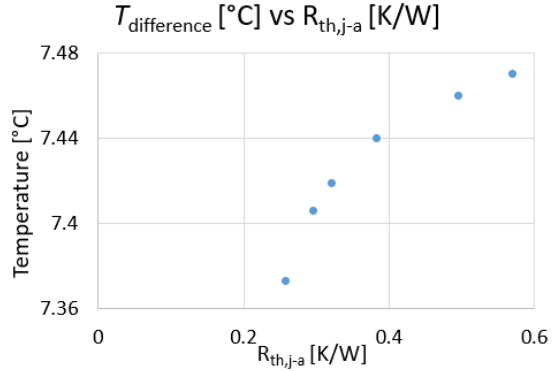


Figure 20: Simulation showing $T_{\text{difference}}$ for different $R_{\text{th},j-a}$ by changing the thermal resistance of the TIM

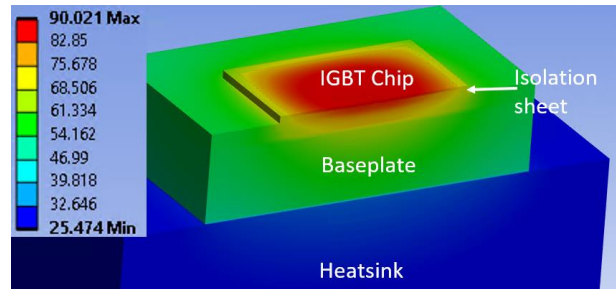


Figure 21: FEM simulation result showing the cross section of the module and the internal temperature profile

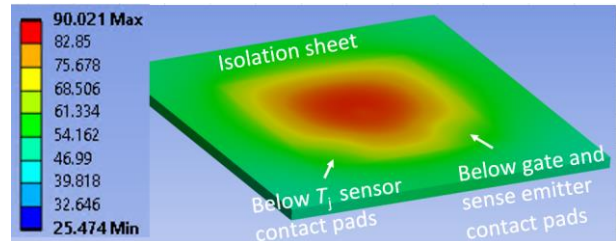


Figure 22: FEM simulation result showing the temperature profile over the ceramic isolation sheet. The regions below the contact pads (cathode and anode pads of the T_j sensor, gate pad, sense emitter pad,) are roughly indicated. The pads are inactive regions on the IGBT chip and their locations influence the appearance of the temperature profile.

Conclusion: Based on several measurements, the slope of the $R_{\text{th},j-s}$ versus $T_{\text{difference}}$ indicates the following: an increase of 1 K/W in $R_{\text{th},j-s}$ would result in an increase in $T_{\text{difference}}$ of around 15 Kelvin for a chip with area of 134.5 mm². This experiment was able to achieve up to 66% increase in $R_{\text{th},j-s}$ and record a maximum of about 3 Kelvin variation in $T_{\text{difference}}$. Further analysis with a wider range of $R_{\text{th},j-s}$ is necessary to confirm the correlation factor. In addition, the impact due to the absolute temperature should be considered if a temperature independent correlation factor is to be applied.

Impact of the chip thickness d

The $V_{\text{CE}}(T)$ method is based on the voltage drop occurring at the p-n junction of the IGBT chip (refer Fig. 23). The p-n junction side (bottom side) is cooled better

than the top side where the T_j sensor is located.

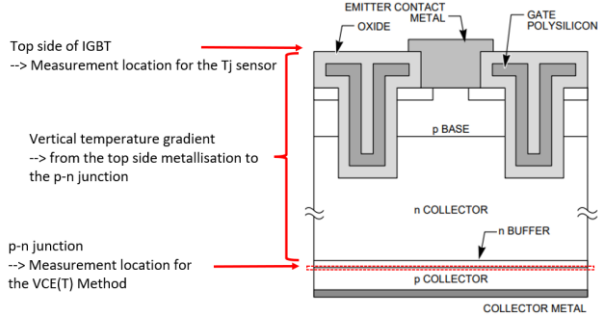


Figure 23: A cross section of a typical IGBT chip from [12]

The study in [9], has analysed the top side average temperature versus the p-n junction temperature ($V_{CE}(T)$ method). The factors influencing the vertical temperature gradient are the chip thickness d and power loss density P_V . The temperature difference was found to be 4.1 Kelvin for a 600 V IGBT ($d = 70 \mu\text{m}$) at $P_V/A = 2.827 \text{ W/mm}^2$. For $P_V = 2.021 \text{ W/mm}^2$ the 4.5 kV IGBT ($d = 470 \mu\text{m}$), the temperature difference was found to be 8.9 Kelvin. As explained in the study, a linear approximation can be applied to estimate the temperature difference using the data points at $P_V = 1.271 \text{ W/mm}^2$ and 2.021 W/mm^2 . Thus the 4.5 kV IGBT is estimated to have a temperature difference of 10.727 Kelvin at $P_V/A = 2.827 \text{ W/mm}^2$. By increasing the thickness from 70 to 470 μm , the temperature difference increases from 4.1 Kelvin to 10.7 Kelvin. For a linear interpolation between 70 to 470 μm chip thickness, it can be roughly considered that at $P_V/A = 2.827 \text{ W/mm}^2$, every 100 μm in additional thickness adds about 1.65 Kelvin in temperature difference.

Impact of the Measurement Delay (t_{md})

As discussed in the previous section, when the $V_{CE}(T)$ is applied, a certain measurement delay t_{md} has to be maintained. It has been explained in [2] and in [10] that the t_{md} should be in range of 300 μs for 1200V IGBTs. Additionally, the t_{md} selection plays a role in the maximum temperature estimated using the $V_{CE}(T)$ method [11]. The focus of this study is to analyse the impact of t_{md} on $T_{\text{difference}}$.

Definition: $T_{\text{difference}} = T_{\text{hotspot}} (\text{occurring } t = 0) - T_{V_{j,\text{max-VCE}}} (\text{function of } t_{md})$

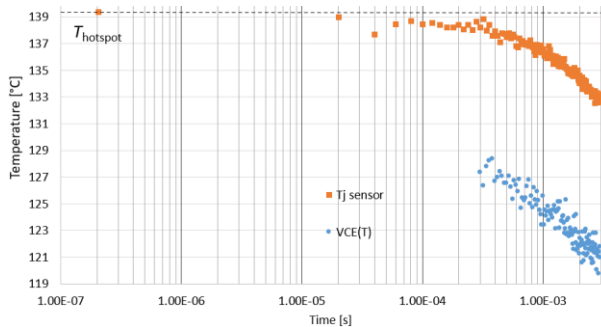


Figure 24: T_j sensor data and $V_{CE}(T)$ data for $I_C = 200 \text{ A}$, $t_{on} = 5 \text{ s}$, $t_{md} = 300 \mu\text{s}$. Definition of T_{hotspot} is shown.

Fig. 24 indicates that T_{hotspot} is about 139 °C whereas the $V_{CE}(T)$ data begins from about 128 °C after the t_{md} of 300 μs . The same figure shows the $V_{CE}(T)$ for the first 3 ms after turning-off the load current. In this example, if the selected t_{md} is 600 μs the difference with respect to T_{hotspot} is around 12.5 to 13 Kelvin.

Cooling down of active area until 1 millisecond:

Fig. 25 is an FEM simulation showing the cool-down of the top surface of the active area of the chip until 1 ms.

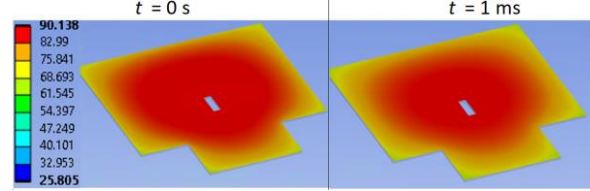


Figure 25: FEM simulation result showing the cool-down of the active area in the interval $0 < t < 1 \text{ ms}$.

The T_j sensor data occurring at $t = 0 \text{ s}$ is the relevant data for the $T_{\text{difference}}$ estimation. From t_{md} (300 μs) until about 1 ms, the $V_{CE}(T)$ in Fig. 24 indicates a temperature reduction in the range of 3 to 3.5 Kelvin. The average temperature of the chip is a time dependent parameter.

Quantification of $T_{\text{difference}}$ vs t_{md} : Fig. 26 shows the evolution of $T_{\text{difference}}$ versus time after t_{md} for measurements conducted with $t_{md} = 200 \mu\text{s}$. Data at different P_V/A and different $R_{th,j-s}$ were utilised for this analysis.

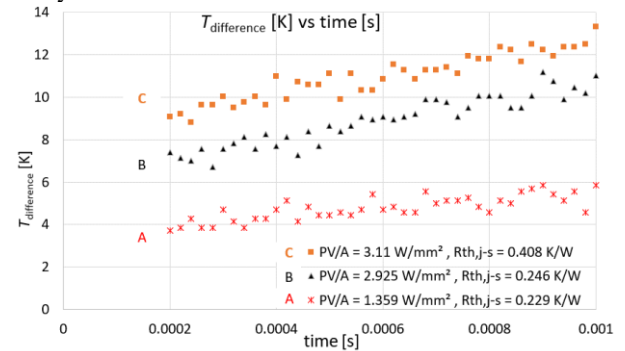


Figure 26: A plot of $T_{\text{difference}}$ for different $R_{th,j-s}$ and different P_V/A . Data from $t_{md} = 200 \mu\text{s}$ onwards.

By comparing the curves A, B and C, the following tendencies can be observed:

1. Curves A and B: similar $R_{th,j-s}$ but different P_V/A . The slope for curve B is higher and it can be understood that higher P_V leads to higher slope in $T_{\text{difference}}$ versus time.
2. Curves B and C: similar P_V/A but different $R_{th,j-s}$. The absolute value of the $T_{\text{difference}}$ is higher for higher $R_{th,j-s}$. However, the slopes for both B and C are in the same range.

Summary: For higher P_V/A the increase in the slope of $T_{\text{difference}}$ has been established. At $P_V/A = 2.925 \text{ W/mm}^2$, and $R_{th,j-s} = 0.246 \text{ K/W}$, the $T_{\text{difference}}$ increases by about 0.465 Kelvin per 100 μs .

CONCLUSION

Impact of the influential factors on $T_{\text{difference}}$:

This study has established the impact of the key factors on the difference in temperature between a dedicated temperature sensor and the virtual junction temperature method ($T_{\text{difference}}$). Power density P_{v}/A has emerged as a key parameter determining the $T_{\text{difference}}$ for a given DUT. At $R_{\text{th,j-s}}$ of about 0.35 K/W, the $T_{\text{difference}}$ would increase by 2 Kelvin for every W/mm². In addition, for a chip with a total area of 134.56 mm², the $T_{\text{difference}}$ has been found to increase with increase in $R_{\text{th,j-s}}$. The increase in $T_{\text{difference}}$ is estimated to be around 15 Kelvin for every K/W increase in $R_{\text{th,j-s}}$. Furthermore, the selection of the t_{md} has shown to have an impact of about 0.4 to 0.5 Kelvin per 100 μs . When a chip of higher voltage range (for example 3.3 kV or 4.5 kV) is used, in addition to the aforementioned factors, every 100 μm increase in chip thickness add about 1.65 Kelvin to $T_{\text{difference}}$.

Relevance of $T_{\text{difference}}$ confirmation in lifetime estimation: Higher $T_{\text{difference}}$ means higher deviation between the real $T_{\text{vj,max}}$ and the estimated $T_{\text{vj,max}}$. The implication for power cycling lifetime estimation can be understood using two scenarios A and B.

A. Impact on lifetime consumption in a real application: For example, an application having $P_{\text{v}}/A = 3 \text{ W/mm}^2$ could have a $T_{\text{difference}}$ of about 8 Kelvin when the $R_{\text{th,j-s}}$ is about 0.35 K/W. Due to load cycling stresses, progressive degradation is expected (such as substrate solder degradation or chip solder degradation), and the overall $R_{\text{th,j-a}}$ is expected to increase. Additional factors such as TIM degradation or reduction of cooler efficiency would contribute the overall increase in thermal resistance. As the lifetime of the DUT rapidly deteriorates, the $T_{\text{difference}}$ increases. An intermediate measurement (or estimation) of the ΔT_{j} performed using the $V_{\text{CE}}(T)$ would not reveal the real ΔT_{j} .

B. Impact on power cycling lifetime models: Power cycling tests are conducted typically at high P_{v}/A in order to achieve high ΔT_{j} . Under such circumstances, the $T_{\text{difference}}$ is high. Considering the solid line in Fig. 9 at $\Delta T_{\text{j}} = 70$ Kelvin, the expected lifetime is 3×10^5 cycles, but at $\Delta T_{\text{j}} = 60$ Kelvin the expected lifetime is between 5.5 and 6×10^5 cycles. Thus, if the $T_{\text{difference}}$ is about 10 to 15 Kelvin, depending up on how the ΔT_{j} is defined, ($V_{\text{CE}}(T)$ method or hotspot method) there could be difference of up to factor 2 in the estimated lifetime.

Limitations of this study:

1. The impact of $R_{\text{th,j-s}}$ was quantified with up to 66% variation versus initial condition. In addition, the TIM was modified to obtain different overall $R_{\text{th,j-s}}$. The impact of change in the R_{th} of the chip solder layer or substrate solder layer has to be verified.
2. The impact due to change in chip thickness was approximated based on the study in [9].

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