Channel Potential Modification induced Displacement Current during the Trench-Gate IGBT Switching

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Abstract

During the switching process of the IGBT, the Miller plateau can be observed on the gate voltage waveform. The present understanding of the Miller plateau is the Miller capacitor induced displacement current at the collector-emitter voltage transient, which is compensated by the gate current from the driver unit. Hence, the gate voltage remains constant.
*In this paper, a novel finding of the **C**hannel **P**otential Modification **i**nduced Displacement **C**urrent (CPiC) is proposed. It has been found that during the Miller plateau, the displacement current is not only provided by the Miller capacitor, but also by inner parts of the gate-emitter capacitor due to the channel potential modification. This novel finding extends the existing descriptions for the IGBT switching behavior and provides a more comprehensive understanding of the Miller plateau.*

Keywords: IGBT, Hard Switching, Miller Effect

Introduction

During the hard switching process of IGBTs, the chip internal parasitic capacitances must be charged and discharged, determining the maximum switching speed of the device. During the collector-emitter voltage transient, the voltage across the Miller capacitor C_{GC} also varies, generating the displacement current. The gate current from the gate drive unit will compensate for this displacement current. Hence, the charging of the gate-emitter capacitor C_{GE} is delayed, and the gate voltage V_{GE} remains at a constant value during this interval, which is known as the Miller plateau [1][2].
Figure 1 (a) shows the turn-on process of a 1.2 kV, 40 A discrete IGBT (IKY40N120CH3) as an instance. A slow switching speed was used to measure the gate current and calculate the gate charge accurately. As shown in the figure, the Miller plateau on the gate voltage waveform can be divided into two parts: a fast negative dV_{CE}/dt part (green shaded area) and the low V_{CE} regime with a much slower dV_{CE}/dt (blue shaded area). The gate current during the plateau is also constant and given by the on-state gate voltage $V_{GE,on}$ of the driver and the gate turn-on loop resistor $R_{G,on}$:

$$I_{G,miller} = \frac{V_{GE,on} - V_{GE,Miller}}{R_{G,on}} \qquad (1)$$

During the fast dV_{CE}/dt from $V_{CE} \approx 575$ V to about 20 V, the gate charge Q_G calculated by the gate current (35.6 nC) should be equal to the Miller capacitor charge Q_{GC} (33 nC). It basically matches the corresponding integration of the static C_{GC} - V_{CE} measurement in Figure 1 (b).

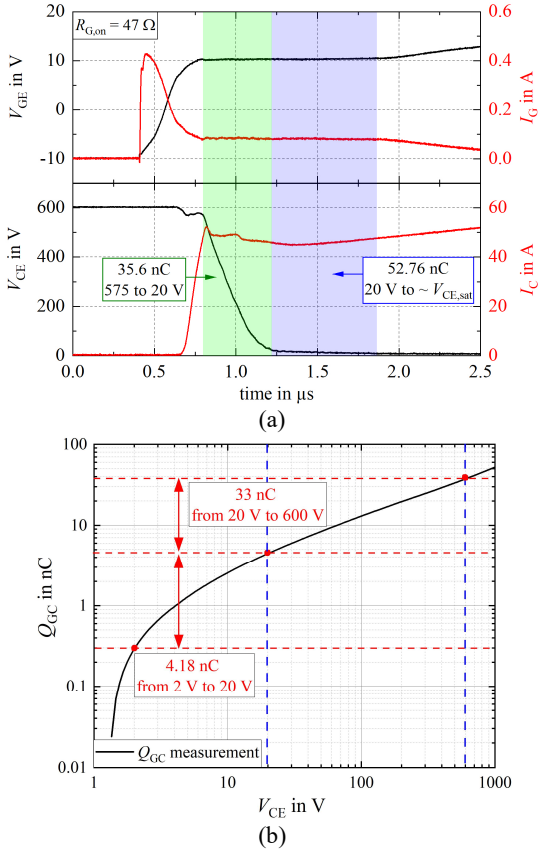


Figure 1: (a) turn-on behavior of IKY40N120CH3, the Miller plateau is divided into two parts; V_{CE} = 600 V, $R_{G,on}$ = 47 Ω, I_C = 40 A. (b) Integration of the static C_{GC} - V_{CE} measurement

However, in the slow dV_{CE}/dt phase, the calculated charge from the dynamic measurement is much higher than the value in the static test. V_{CE} drops slowly from about 20 V to near the saturation voltage $V_{CE,sat}$. The calculated charge value in this interval is 52.76 nC, and much higher than the 4.18 nC of the static C_{GC} - V_{CE} test. There may be an inevitable measurement error due to the gate current measurement, the integration interval selection, and the delay between the measurement probes. However, the overall trend is clear. A similar phenomenon can also be found in the small dV_{CE}/dt phase for the turn-off behavior. Therefore, the focus of this paper is to explain the origin of excess charge in the Miller plateau phase, especially in the low V_{CE} regime.

Dynamic Miller Effect at Low Collector-Emitter Voltage Regime

The composition of the Miller capacitor C_{GC} (orange colour) and the gate emitter capacitor C_{GE} (blue colour) without applied voltage for a trench-gate IGBT is shown in Figure 2 (a). The larger part of the Miller capacitor is the oxide capacitor of the trench side walls and the trench bottom. The field oxide is much thicker compared to the gate oxide layer; therefore, the contribution to the total C_{GC} is smaller. During the Miller plateau of the IGBT turn-on, the gate voltage is almost constant and determined by the threshold voltage $V_{G,th}$, load current I_C and the transconductance g_{fs} of the device:

$$V_{GE,Miller} = V_{G,th} + \frac{I_C}{g_{fs}} \tag{2}$$

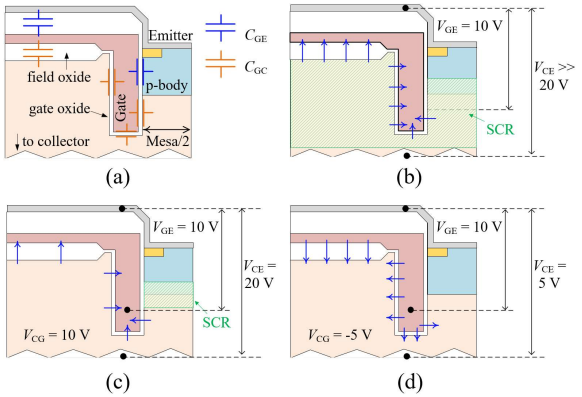


Figure 2: Simplified dynamic estimation of the Miller capacitance at different V_{CE}; (a) composition of C_{GC} and C_{GE} for a trench gate IGBT without voltage; (b) beginning of the Miller plateau $V_{CE} \approx V_{DC}$; (c) at low V_{CE} regime, $V_{CE} > V_{GE} = 20$ V; (d) $V_{CE} < V_{GE} = 5$ V

Assuming that the amplitude of the Miller plateau is 10 V, at the beginning of the plateau, the V_{CE} is still high and close to the DC-link voltage V_{DC}. At high V_{CE}, the collector potential is much higher than the gate. Inside the oxide layer, the electric field points from the collector to the gate, as indicated by the blue arrows in Figure 2 (b). The space charge region (SCR) inside the low-doped drift layer (w_{SCR}) is at this time point fully established and takes over the voltage. Therefore, the junction capacitor C_J is in series with the oxide capacitor C_{Ox} and results in a smaller Miller capacitor:

$$C_{GC} = \frac{C_{Ox} \cdot C_J}{C_{Ox} + C_J} = \frac{C_{Ox} \cdot \frac{\varepsilon \cdot A}{w_{SCR}}}{C_{Ox} + \frac{\varepsilon \cdot A}{w_{SCR}}} \tag{3}$$

After V_{CE} decreases to a lower value, e.g., 20 V, the junction capacitor becomes much higher and increases C_{GC} according to Equation (3). Hence, the dV_{CE}/dt is limited. An electric field is still inside the oxide layer, but the strength is much weaker, see Figure 2 (c). With further decreased V_{CE}, e.g., $V_{CE} = V_{GE}$, the space charge region vanishes, and the Miller capacitor becomes the pure oxide capacitor and reaches the maximum value. In the final stage of the Miller plateau, when $V_{CE} < V_{GE}$ (Figure 2 (d)), any small reduction in V_{CE} must discharge the whole oxide layer of the Miller capacitor. Therefore, a large displacement current is still required, even if the changing rate of V_{CE} is much less.

Therefore, when V_{CE} is low, e.g. close to the saturation voltage, the result obtained through the static C_{GC} - V_{CE} test cannot accurately estimate the required gate charge during the dynamic processes. Because for static C_{GC} - V_{CE} measurement, the gate and the emitter of the tested device are shorted, and $V_{CE} = V_{CG}$. As V_{CE} rises, the SCR is established instantly at the emitter pn-junction. Therefore, the value of the Miller capacitance will start to decrease. However, when the IGBT operates in the switching mode, the voltage difference between the gate and the collector has to be considered.

According to the definition, the change of electric field strength in the capacitive medium can be used to describe the displacement current:

$$I_{dis} = \varepsilon_0 \cdot \frac{dE_{Ox}}{dt} + \frac{dP_{Ox}}{dt} \approx \varepsilon_0 \cdot \frac{dE_{Ox}}{dt}. \tag{4}$$

Where P is the polarization in the medium (SiO_2), and remains constant. Therefore, to more intuitively describe the Miller effect generated displacement current at the low V_{CE} regime, a two-dimensional half-cell trench-gate IGBT model was developed in Synposis TCAD and calibrated according to the measured device. The front side design is shown in Figure 3, the thickness of the gate oxide layer is 100 nm.

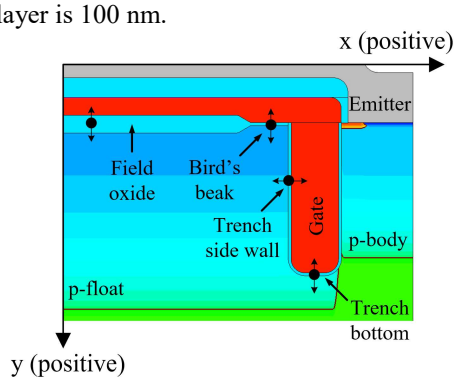


Figure 3: Front side design of the IGBT model and the extraction points for the electric field strength in the oxide layer of C_{GC}; the positive direction for x- and y-direction is given

After that, TCAD simulations were carried out to extract the internal electric field of the oxide layer with up-swept V_{CE} from 0 to 1000 V. Because the junction capacitance is in series with the oxide capacitance, the displacement current (from ΔE_{Ox}) in the oxide can be used to represent the current flow through the Miller capacitance. The V_{CE} is swept upwards with 1 V/s, which is similar to the static test. The perpendicular electric field strength of the oxide layer was extracted. The selection of extraction points is shown in Figure 3. The gate voltage was set to 0 V or positive 10 V. When V_{GE} = 0 V, it simulates the static small signal C_{GC} - V_{CE} test situation. V_{GE} = 10 V is analogous to the IGBT turn-on, where the gate voltage is in the Miller plateau level and holds in a steady state.

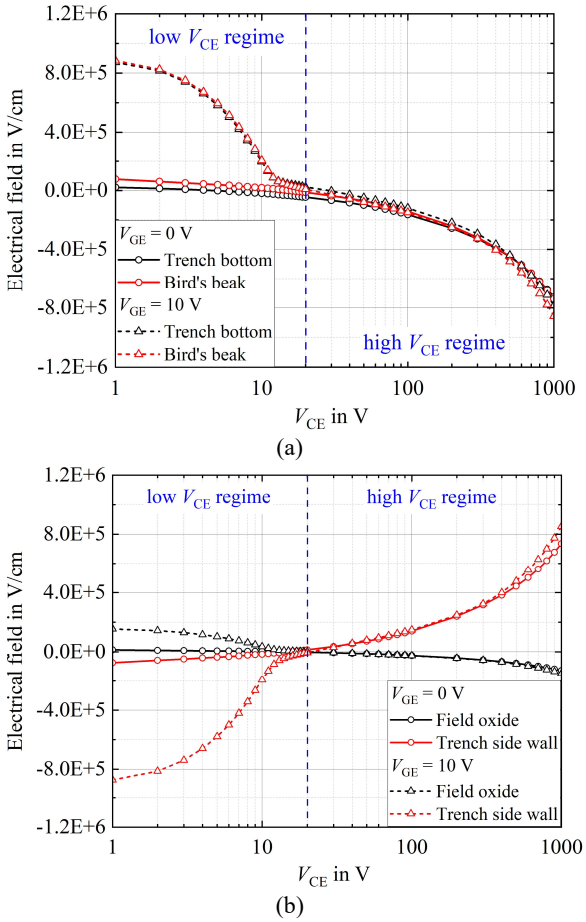


Figure 4: Electric field at the different oxide layer parts for Miller capacitor with different V_{GE} and V_{CE}

Figure 4 (a) shows the electric field at the trench bottom and the bird's beak in the y-direction with respect to V_{CE}. It can be seen that when V_{GE} is 10 V and V_{CE} is small, there is a large potential difference between the gate and the collector. Therefore, the electric field strength in the oxide layer is high. When V_{CE} = 1 V, the electric field strength in the oxide layer is about $8.8 \cdot 10^5$ V/cm in both the trench bottom and the bird's beak area. Here a positive electric field in the y-direction represents that potential of the gate is higher than the collector.

When the gate voltage is 0, the electric field strength is close to 0. It is not exact zero due to the difference in surface potential between the highly doped poly-gate and the p-float region [2][3].

In the low voltage region (V_{CE} up to 20 V), the electric field modification (ΔE_{Ox}) due to the potential difference between the gate and the collector is much higher than at V_{GE} = 0 V. If the absolute value of ΔE_{Ox} is considered, from 1 to 20 V it is almost the same change in V_{CE} as from 20 to 1000 V (high V_{CE} regime). Hence, the charge generated from the displacement current is also close, see Equation (4). Therefore, the dynamic Miller effect at low voltage is much stronger than estimated by the static small signal C_{GC} - V_{CE} test.

When V_{CE} is higher than about 20 V, the collector voltage will dominate the electric field strength of the oxide layer. Therefore, the gate voltage has almost no influence anymore. In Figure 4 (b), the situation on the trench side wall is similar. For the field oxide layer, due to the higher thickness, the electric field strength is lower than that of the gate oxide layer. However, the influence of this part should not be neglected because of the large area.

The depletion region formation/expansion process inside the device at different gate voltages is shown in Figure 5. If the gate and the emitter are shorted (V_{GE} = 0 V), there is no influence/impact from the gate voltage, the space charge region between the p-float and the drift region has already been created at V_{CE} = 2 V. Consequently, the junction capacitance is formed and in series with the oxide capacitance, reducing the Miller capacitance. When V_{CE} reaches 20 V, the depletion region reaches about 20 µm in the drift region.

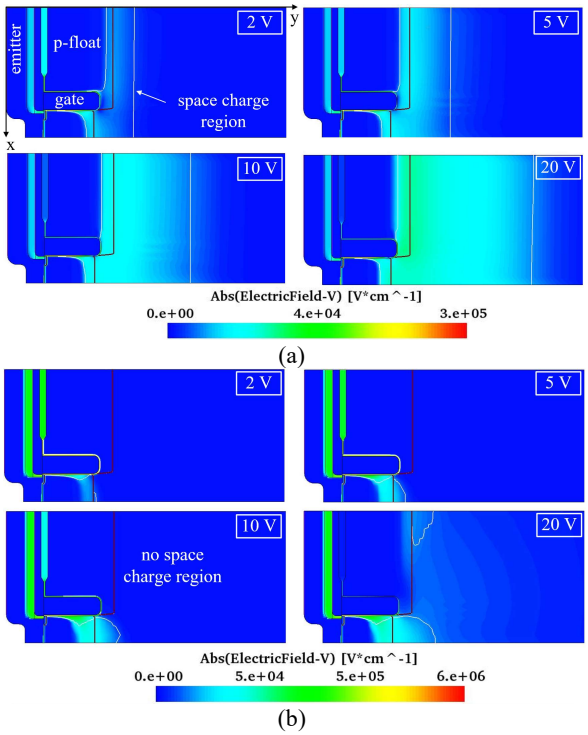


Figure 5: The formation and expansion of depletion region inside the device at different gate voltages, V_{CE} from 2 V to 20 V. (a) V_{GE} = 0 V, (b) V_{GE} = 10 V

When V_{GE} = 10 V, due to the potential difference between the gate and collector and the load current, the space charge region cannot be established at the pn-junction

immediately. The electric field strength inside the oxide layer is higher compared with V_{GE} = 0 V. With increased V_{CE}, the collector potential is opposite to the gate, thus reducing the electric field strength in the oxide layer. No space charge region can be formed since the gate potential is still higher. Until V_{CE} reaches 20 V, the formation of a space charge region can be observed at the pn-junction. Before that, the Miller capacitor is mainly the oxide layer capacitor.

Channel Potential Modification induced Displacement Current (CPiC) in the Gate-Emitter Capacitor

In addition to the displacement current generated by the Miller capacitance, during the low V_{CE} regime, the drop of V_{CE} will cause a voltage change close to the channel region. The on-state voltage of the IGBT can be expressed by:

$$V_{CE,on} = V_{pn} + V_{drift} + V_{mesa} + V_{CH} \qquad (5)$$

Where V_{pn} is the built-in voltage of the pn-junction at the collector side, V_{drift} the voltage drop in the drift region, V_{mesa} the voltage drop in the mesa region in between the trenches (where no channel is present) and the channel voltage drop V_{CH}, see Figure 6. For the turn-on process, the voltage in each part decreases and vice versa for the turn-off. At this time, since V_{GE} is stabilized at the Miller plateau level, it can be seen from Equation (4) that when the channel potential V_{CH} changes, displacement current will be generated in the gate-emitter capacitor. When the V_{GE} is greater than the threshold voltage $V_{G,th}$ and the inversion channel has been formed, C_{GE} is mainly the oxide layer capacitance due to the existence of the high conductive inversion layer, and it is large. Therefore, the displacement current generated by C_{GE} is high, too [3].

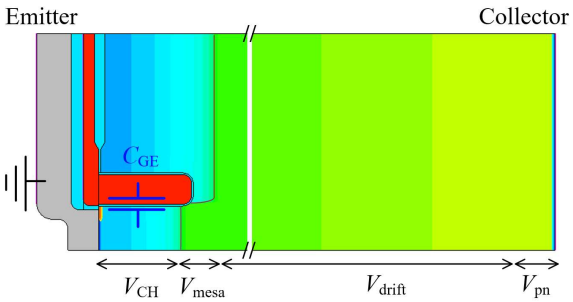


Figure 6: On-state voltage distribution of the trench-gate IGBT

Figure 7 shows the simulated switching process and the variation of the channel potential V_{CH}. The simulated results match well with the measurements, and two stages of dV_{CE}/dt during the Miller plateau can be clearly seen. The channel potential is extracted from the emitter metallization to the end of the channel, as shown in Figure 6. It changes significantly in the low V_{CE} regime, where dV_{CE}/dt is also small. For the turn-on process, the Miller plateau voltage stabilizes at approximately 10 V.

In the low dV_{CE}/dt region (blue shaded area) the channel potential drops from 8.85 V to 2.65 V. If we wait for V_{GE} to reach the 15 V, V_{CH} is much smaller with 1.08 V. For the turn-off process, this voltage rises from 1.705 V to 8.87 V.

Four time points from t_1 to t_4 at the low V_{CE} regime are selected in Figure 7 to observe the displacement current inside the device. The primary focus is on the current in the gate-emitter capacitor due to the V_{CH} modification. Hence, only the displacement current density perpendicular to the oxide layer of C_{GE} (in the x-direction) is illustrated in Figure 8. At the bottom of the trench, the displacement current is mainly in the y-direction, hence, almost zero in the x-direction.

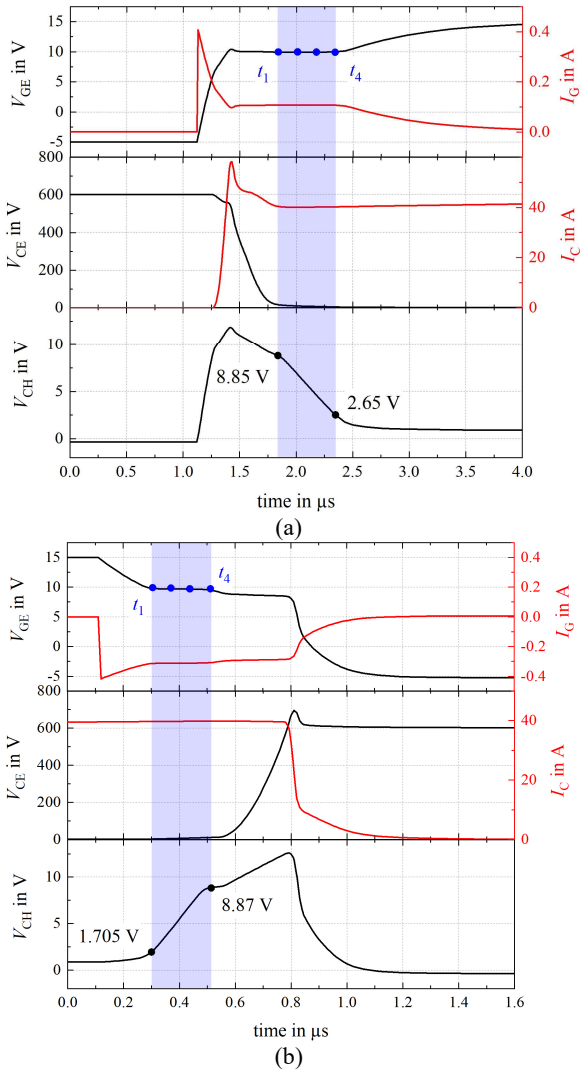


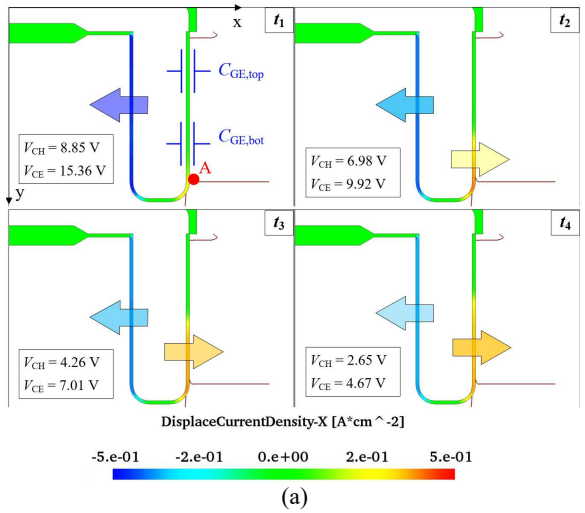
Figure 7: Simulated switching behavior with extracted V_{CH}; V_{DC} = 600 V, $R_{G,on}$ = $R_{G,off}$ = 47 Ω, I_C = 40 A, T = 300 K. (a) turn-on, (b) turn-off

The oxide layer´s displacement current density for turn-on and turn-off in the x-direction for each time point is shown in Figure 8. The corresponding channel voltage and V_{CE} are given. The direction of the arrows indicates the direction of the displacement current flowing through the oxide layer. The intensity of the colour represents the magnitude of the current density. Point A is noted as the

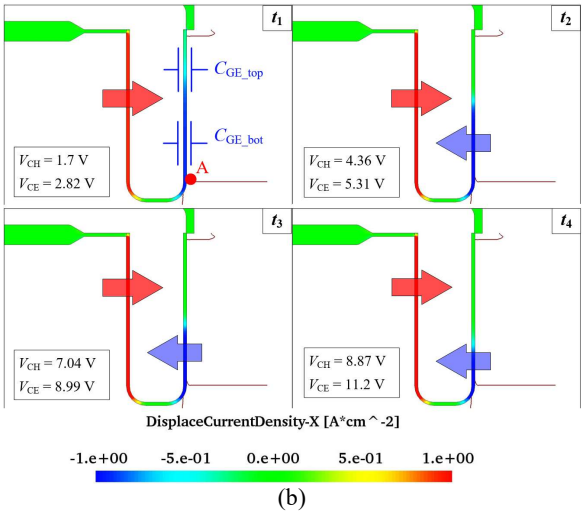
end of the channel. C_{GE} is divided into top and bottom parts for convenience of description.

At the beginning of the turn-on process t_1, a small positive displacement current is generated in the mesa region and is close to the end of the channel due to the slightly decreased V_{mesa} and V_{CH}. The direction is from the gate to the channel (emitter). Afterwards from t_2 to t_4, V_{CH} keeps decreasing, and the CPiC generated near to $C_{GE,bot}$ becomes more significant. Since the current direction is out of the gate, it is compensated by the charging gate current from the gate driver.

In addition, a negative displacement current can be seen for the left trench side wall, which is from the gate to the collector. This current belongs to the displacement current generated by the Miller capacitor causing the Miller plateau from the conventional understanding. In the upper part of the gate capacitor, CPiC is not apparent since the V_{CH} change is small in the upper part of C_{GE}.



(a)



(b)

Figure 8: Displacement current density j_{Dis} in x-direction in the oxide at different time points in Figure 7 during the switching; (a) turn-on, (b) turn-off

For the turn-off process, V_{CH} increases during the low V_{CE} regime. Therefore, the direction of CPiC generated in the gate capacitance is opposite and flows into the gate from the channel. Similarly, this current, along with the current generated by the Miller capacitance, is compensated by the discharge current from the gate driver.

The above analysis shows that the Miller plateau is not only a consequence of the Miller capacitor. The gate capacitor will also affect this process and should therefore also affect the device's switching speed. During the Miller plateau phase, the gate current can be considered as the displacement current from the whole oxide layers of C_{GC} and C_{GE}.

$$I_{G,Miller} \approx I_{Ox} = I_{GC,total} + I_{GE,total} \tag{6}$$

Therefore, by extracting the current of the entire oxide layer, the ratio between CPiC and the displacement current from the Miller capacitor can be quantitatively analysed.

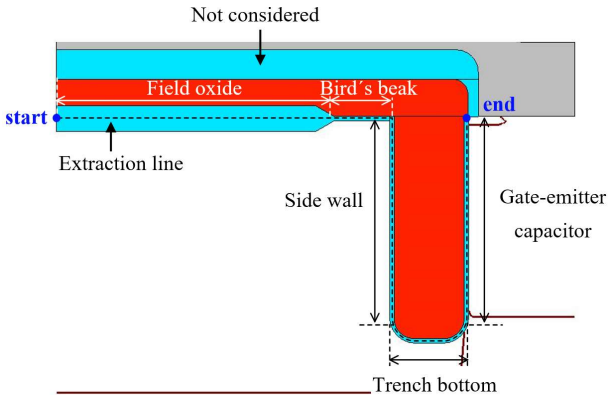


Figure 9: The extraction line (black dashed) of the displacement current through the oxide layer of C_{GC} and C_{GE}

The extraction line is shown in Figure 9. The starting point is the left edge of the field oxide layer, and then along the field oxide layer to the right, through the bird's beak area, the left trench side wall, the bottom of the trench, and finally reaches the emitter n^+-region through the right trench side wall. The part from the trench bottom to the n^+-region can be approximately considered as the C_{GE} region, generating CPiC:

$$I_{GE,total} = I_{CPiC} = I_{GE,bot} + I_{GE,top}. \tag{7}$$

The sum of the displacement currents in the oxide layer in other regions is the displacement current generated by the Miller capacitance:

$$I_{GC,total} = I_{GC,field\_Ox} + I_{GC,birdsbeak} + I_{GC,side\_wall} + I_{GC,trench\_bot}. \tag{8}$$

The displacement current in the top part gate oxide layer is not considered because the potential modification in the gate is negligible during the Miller plateau.

The IGBT model in TCAD is a two-dimensional model, but the default depth in the z-direction is 1 µm. Therefore, the length of the extraction line in Figure 9 corresponds to the area of the oxide layer A_{Ox} in µm^2. Thus, the displacement current in the oxide layer can be

obtained by integrating the displacement current density from the "start" point to the "end" point:

$$I_{G,Miller} \approx I_{Ox} = \int_{start}^{end} j_{Dis,Ox} \cdot dA_{Ox} \,. \qquad (9)$$

Figure 10 shows the distribution of the displacement current in the oxide layer at the turn-off time t_1 and the turn-on time t_4. The orange parts represent the Miller capacitance and the generated displacement current. The blue colour parts represent gate-emitter capacitance and CPiC effect. It can be seen that at t_1 for turn-off, CPiC accounts for about 25.5% of the total gate current. And it is about 19.4% at t_4 for turn-on.

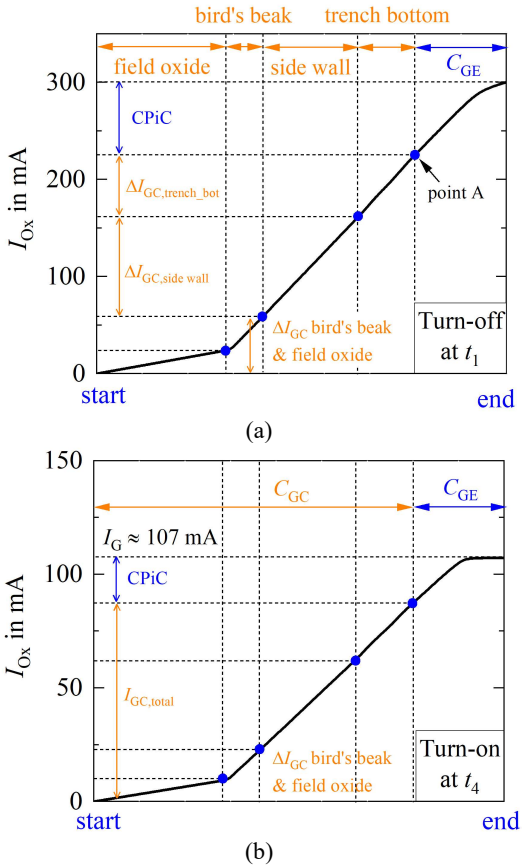


Figure 10: The displacement current through the corresponding part of the oxide layer I_{Ox}, (a) at turn-off t_1, (b) at turn-on t_4

		$I_{G,Miller} \approx I_{Ox}$	$I_{GC,total}$	CPiC	% of CPiC to I_{OX}
turn-off	t_1	300.4	223.6	76.8	**25.5**
	t_2	311.8	254.1	57.7	**18.5**
	t_3	311.8	267.7	44.1	**14.1**
	t_4	310.7	281.3	29.4	**9.5**
turn-oon	t_1	107.8	105.3	2.5	**2.3**
	t_2	107.7	97.02	10.7	**9.9**
	t_3	107.6	91.7	15.9	**14.8**
	t_4	107.2	86.4	20.8	**19.4**

Table 1: Displacement current generated by C_{GE} and C_{GC} at different time points and proportions to the total oxide current I_{Ox} during the Miller plateau with slow dV_{CE}/dt, current in mA

Table 1 summarizes the CPiC fraction from t_1 to t_4 during turn-on and turn-off. The main reason for the additional charge at the end of the Miller plateau is still the charging and discharging of the Miller capacitor. However, the CPiC generated in C_{GE} plays an essential role in the Miller plateau, too. This knowledge could be taken into account in the device design for further optimization of the switching (esp. dv/dt phase).

Conclusion

In this paper, the Channel Potential Modification induced Displacement Current during the Miller plateau of the trench-gate IGBT was introduced and verified by the TCAD simulation. Due to the channel voltage variation, the gate capacitance also generates a displacement current in the Miller plateau which is (eventually) compensated by the gate current. Therefore, the Miller plateau is also affected by the gate-emitter capacitance. The cell-design of the IGBT, especially the length of the channel, will have a significant impact on the CPiC.
In some scenarios, such as low-inductive short circuit type II, where the electron current in the channel changes sharply, the channel potential will also be affected by CPiC, and leads to an increased gate voltage overshoot [4].

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