Low forward voltage gate controllable diode for 6.5 kV HVDC application

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Abstract

Gate-Controllable Diode (GCD) allows charge carrier modulation at the anode region, by gate terminal biasing, to gain plasma control. This is used to achieve low-saturation mode and high-speed mode of the diode. Apart from the two operating modes, the anode side plasma control can also be utilised to desaturate the diode during commutation, to lower the overall switching losses. This paper is continuation work of earlier demonstrated GCD. The diode is designed as Si bi-polar power diode for 6.5 kV HVDC applications. In the current paper, a design consideration depending on various doping profiles of GCD was made. Thereby, a detailed study of switching behaviour with the switching pattern were conducted, to reduce the overall switching loss and improve the efficiency.

Keywords: Controllable diode, low-saturation, high-speed, desaturation, reverse recovery

Introduction

The diode is critical part in Modular Multilevel Converter (MMC) sub-module of a HVDC system, which is used as a free-wheeling diode (FWD) for the IGBT. A lot of research has been made towards improvement in the performance of the IGBT. To increase the overall efficiency of the total converter, the diode must compliment the IGBT. For 6.5 kV modules, a better performing Si pin-diode is required for free-wheeling application. Apart from improved efficiency, a FWD must have a soft turnoff during reverse recovery, better over current and over voltage peak, better performance at low current and low temperature.

Typically, in an HVDC system the inverter and rectifier operations demand different diode characteristics to have better efficiency. Switching losses dominate the high side diode operation in both rectifier and inverter mode, whereas conduction losses dominate the low side diode in rectifier mode and switching losses on the low side diode during inverter mode. To improve the overall converter performance, a low on-state voltage diode must be equipped as FWD on low side of the rectifier. A high-speed diode must be equipped on the high side of the rectifier, and on both high side and low side of the inverter. This requirement demands two separate characteristic pin-diodes which can be adapted to achieve both low-saturation and high-speed mode or a single controllable diode. This requires reducing the on-state voltage drop, meanwhile lowering the switching losses as well.

Although various controllable diode ideas have been studied before, literature [1],[2], exhibit a planar gate approach where it gets difficult to lead the diode to low forward voltage behaviour, hence not suitable for above mentioned requirement. Paper [3] demonstrates a difficult diode design for realization in practicality. Previously a gate controllable diode [4], was proposed based on submicrometric trench technology similar to literature from [5],[6], which is a robust technology and enables efficient on-state and commutation behaviour.

Controlling charge carriers on the anode side by variation in gate potential allows the operation of low-saturation and high-speed modes, as discussed in [4]. This is helpful in defining the diode operations on high side and low side of the MMC submodule. The aim of this paper is

to further improve the properties, by realizing even lower on-state voltage drop, and optimize switching losses of GCD. A Sentaurus TCAD based, numerical device level simulation of GCD is demonstrated in this paper.

Design considerations of new GCD

The p-n junction of the diode is parallel to the MOS channel area, which will be created beside the oxide of the gate in the vertical direction. With the positive potential, less than V_{bi} or with a negative potential applied to the gate, channel remains closed, and the diode behaves as a normal pin-diode. To reduce the on-state voltage of GCD from [4], the doping of p^+ layer is increased to a higher value of 1e18 cm^{-3} from the earlier value of 5e16 cm^{-3}. Instead of a flat charge carrier profile of [4], this creates a negative gradient of charge carrier density. Typically, with negative potential on gate, an enhancement of charge carriers from the highly doped p^+ layer is seen increasing the plasma on the anode side, leading to low-saturation mode.

Increasing V_{GA} to a positive potential, an electron channel is induced beside the oxide layer, creating a current path parallel to the p-n junction. By keeping the resistance components of this current path lower than set-in voltage, p-n junction is nearly shorted allowing external current to flow. To have a wide spread of plasma range between the low-saturation mode and high-speed mode, an additional high doped thin n^+ layer or n-buffer layer of doping 2.5e17 cm^{-3} is added beneath the p^+ layer, which is kept under the influence of the gate trench. The n-buffer layer lays a small resistance, thus, increasing the electron current and decreasing injection efficiency as described by the Eq. 1 [7]. Applied positive potential, doping of p^+ layer and n-buffer define the anode emitter efficiency and hence the plasma associated with the anode side. Therefore, the diode could be operated either in bi-polar mode with lower plasma on the anode side, or in the uni-polar mode like a MOSFET.

$$\gamma = 1 - \frac{j_n}{j} \qquad \text{Eq. 1}$$

Homogeneous approach

Fig. 1, gives a schematic representation of modified GCD, similar to the design from [4]. A submicrometric trench structure is designed with a mesa width of 0.4 µm (X_{MOS}) and a carefully selected mesa width to cell pitch ratio as in [8]. The model is simulated as a 4-cell model with an X_{MAX} of 6 µm. A 1.5 µm thick p^+ anode region and a 2 µm thick n-buffer region was realised into the sub-µm mesas between the trench gates. A homogeneous doping is maintained at the anode side. A very thin, highly doped p^+ layer is formed near the anode contact to make the region low ohmic. A 0.5 µm n^+ cathode layer of doping density 5e17 cm^{-3} is diffused into the n^- intrinsic base region, along with the field stop layer.

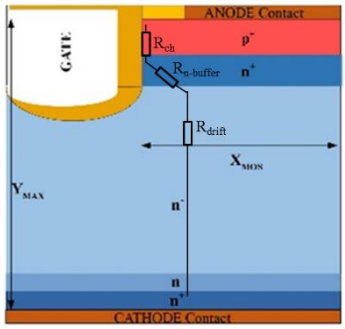

Fig. 1. Schematic cross section of a single cell homogeneous gate controllable diode.

Inhomogeneous approach

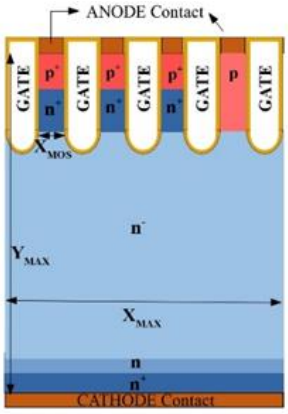

Fig. 2. Schematic cross section of a four cell inhomogeneous gate controllable diode.

A second approach to the design is considered with inhomogeneous doping in the cell level as shown in Fig. 2. The doping of p^+ layer and n-buffer layer, of the left part of the three cells are kept like the homogeneous model, whereas the right-side single cell's p layer doping is reduced to 6e16 cm^{-3} with a thickness of 4 µm and the n-buffer layer is removed. The ratio between high doped cells and low doped cell is kept in the

order of 3/1 for a total X_{MAX} of 6 µm. The principle remains similar to homogeneous approach, except for the right cell, where a free path for holes is created. Static on-state characteristics of homogeneous and inhomogeneous GCD compared with reference pin-diode is shown in Fig. 3 and corresponding charge carrier distribution is shown in Fig. 4.

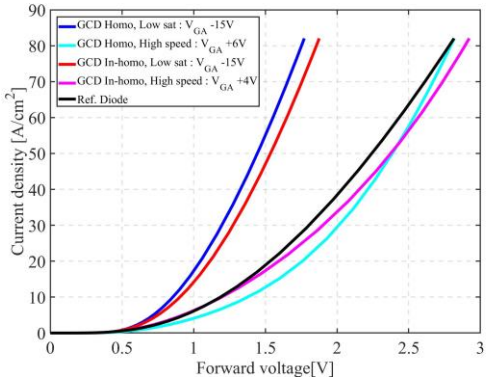

Fig. 3. Static on-state characteristics of homogeneous and inhomogeneous GCD at low-saturation and high-speed modes compared with reference diode. j_{nom} = 82 A/cm^2, T = 150 °C.

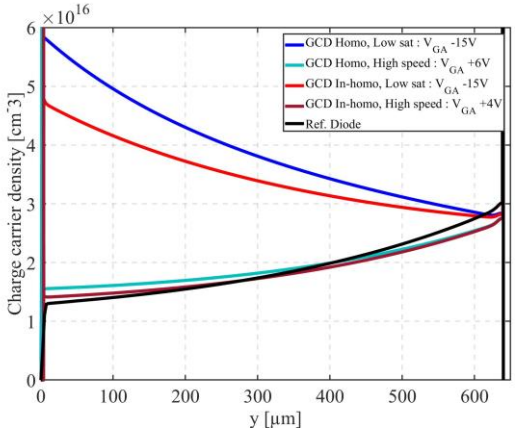

Fig. 4. Charge carrier density across the cross-section of homogeneous and inhomogeneous GCD at low-saturation and high-speed modes compared with reference diode under static condition. j_{nom} = 82 A/cm^2, T = 150 °C.

With the closed channel, at V_{GA} -15 V, anode terminal is flooded with charge carriers leading to lower on-state voltage drop of 1.8 V for homogeneous GCD and 1.85 V for inhomogeneous GCD. Auger recombination limits the reduction of forward voltage lower than 1.5-1.6 V for 6.5 kV device. With controlled anode injection efficiency, at a slightly low positive gate voltage of V_{GA} +6 V for homogeneous GCD and V_{GA} +4 V for inhomogeneous GCD, the charge carriers are brought to level equivalent to the reference pin-diode, which operates as high-speed mode with on-state voltage around 2.8-2.9 V. In this case, the current is established by both diffusion and drift current.

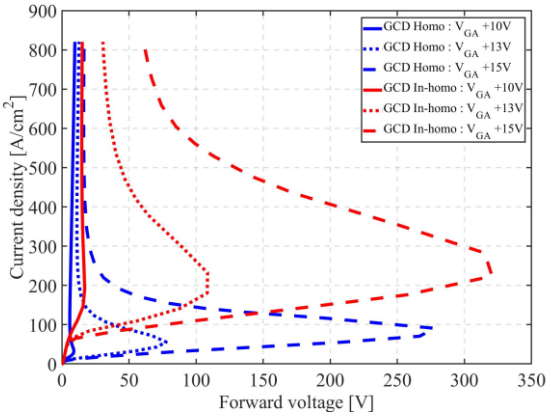

Fig. 5. Static on-state characteristics of homogeneous and inhomogeneous GCD. j_{nom} = 410 A/cm^2, T = 150 °C.

In the homogeneous approach, at higher gate voltages, for forward current densities lower than critical current, a MOSFET kind of behaviour is triggered. This leads to majority carrier mode and anode current mainly constitutes electron current with injection of holes being stopped. The current (I_{crit}) is determined by the resistance offered by the channel and the n-buffer (refer Fig. 1), which is given by Eq. 2 [9]. A snap back in the voltage is observed. In the inhomogeneous approach, due to opening of a path for holes to flow, a bi-polar behaviour prevails until twice the nominal current density, avoiding a snap back during nominal operating condition. Due to low doping concentration and smaller area distribution of the low doped p-region, snap back occurs at higher current densities. Fig. 5, shows the behaviour of homogeneous and inhomogeneous GCD at 5*j_{nom}, and higher gate voltages, +10 V, +13V, +15V.

$$I_{crit} = {V_{bi}}/{(R_{ch} + R_{n-buffer})} \qquad \text{Eq. 2}$$

Blocking behaviour of new GCD

The thickness (Y_{MAX}) of the model and doping concentration of the drift region is designed to handle a reverse blocking voltage of 6.5 kV. The static blocking characteristics of homogeneous and inhomogeneous GCD is simulated at 150 °C as shown in Fig. 6, where

the diode is seen to block the nominal blocking voltage of 6.5 kV.

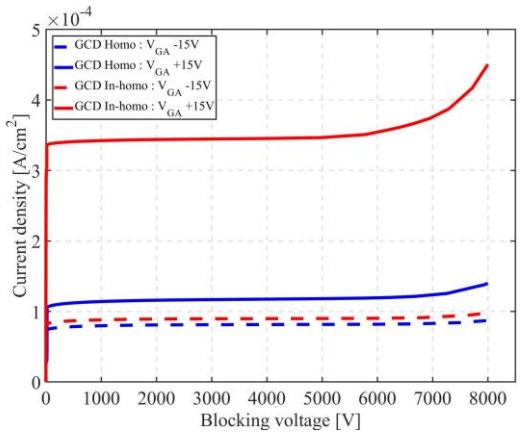

Fig. 6. Static blocking simulation of 6.5 kV homogeneous and inhomogeneous GCD, T = 150 °C.

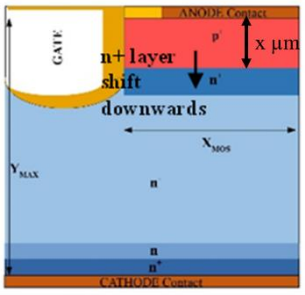

Fig. 7. Schematic cross section of a single cell GCD with n-buffer layer shift downwards by 'x' µm.

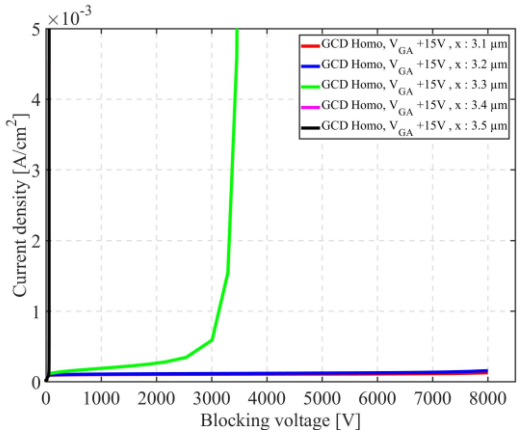

Fig. 8. Static blocking simulation of 6.5 kV homogeneous GCD dependent on 'x', T = 150 °C.

The placement of n-buffer layer underneath the p^+ layer has an influence on the blocking capability of the diode [7]. Fig. 7, shows the shift of n-buffer layer downwards by 'x' µm from the anode contact. This shift was simulated for both homogeneous and inhomogeneous GCDs. It is observed, if the n-buffer layer is placed out of the trench, i.e., when the peak doping concentration of n-buffer layer is outside the influence of the gate terminal, the current flows to the anode contact with loss of the 6.5 kV blocking capability. Fig. 8 and 9, show the static blocking characteristics of homogeneous and inhomogeneous GCDs respectively, at 150 °C for various 'x' from 3.1 µm to 3.5 µm. At 3.3 µm, homogeneous diode blocks only 3 kV, whereas inhomogeneous diode blocks almost 6 kV. Both the diodes, block only several 100 V past 3.4 µm.

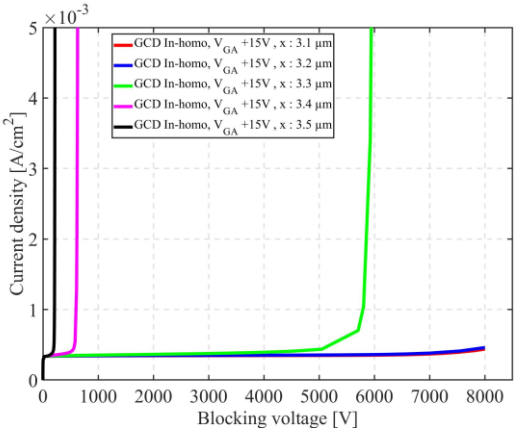

Fig. 9. Static blocking simulation of 6.5 kV inhomogeneous GCD dependent on 'x', T = 150 °C.

Dynamic behaviour

Low-saturation mode diode produces higher switching losses due to the amount of charge carriers and high-speed mode is equivalent to the reference diode. Significant improvement from the reference diode is only seen when the switching losses are reduced. Implementing the desaturation pulse concept described in [4], switching losses are reduced effectively, increasing the overall efficiency of the network.

Fig. 10 shows the static charge carrier distribution, taken across the cutline in y-direction at various V_{GA} for inhomogeneous device, simulated at nominal current density. Plasma on the anode side at V_{GA} +10 V has reached a low point in bi-polar operation with high voltage drop of around 7 V. A slightly higher V_{GA} of +13 V is used in the duration 'tdsat', during commutation. The doping of the GCD is set in such a way as to achieve a uni-polar characteristics at V_{GA} +15V, for study purpose. This approach of doping could be modified for practical applications.

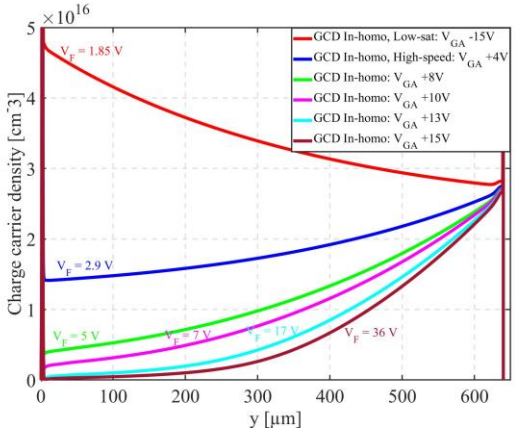

Fig. 10. Charge carrier density across the cross-section of inhomogeneous GCD at varying V_{GA}. j_{nom} = 82 A /cm^2, T = 150 °C.

It is to be noted that, the gate drive for such diodes gets complex. For HVDC applications with 150 Hz switching frequency, a gate drive demanding such desaturation times could be implemented with PWM controller. But for the gate drivers using hysteresis controller, the desaturation time is limited by shorter duration within the order of 20 µs.

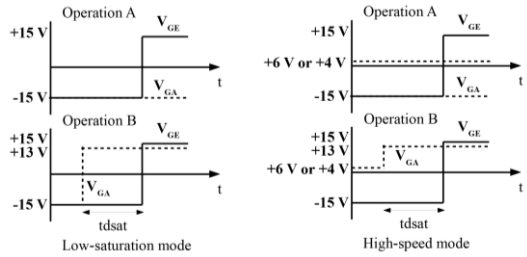

Fig. 11. GCD and IGBT, gate drive condition.

To understand the control strategy of the GCD and to reduce the overall losses, the driving condition of both diode and IGBT are considered as shown in Fig. 11. Operation A shows switching of IGBT alone from -15 V to +15 V, without any control of GCD. Operation B shows how the tdsat is applied for GCD while switching between conducting state (V_{GA} -15 V, +6 V or +4 V) to desaturation state (V_{GA} +13 V). Dynamic behaviour of GCD and IGBT were obtained with a boost circuit configuration. The simulations are performed for a nominal current density of 82 A/cm^2, a DC-link voltage of 3.6 kV, with a stray inductance of 1.6 µH, at a temperature of 150 °C. A 6.5 kV submicrometric trench IGBT was used similar to a model scaled from [4],[5],[8], where IGBT was simulated for half the current density of the diode. For standardization under nominal switching condition, the peak power on single diode was kept at a maximum of 150 kW.

Due to effects of recombination, diode takes at least 10 µs [7] to start reducing the reverse recovery charge during commutation. With introduction of tdsat, the switching time difference between IGBT and GCD, overall turn on losses reduces by a great margin. As seen from [4], operation A produced slowest dj_F/dt with highest switching loss on both IGBT and GCD, as there is not enough time for plasma desaturation. With increasing tdsat, we notice the loss reduction on both diode and IGBT.

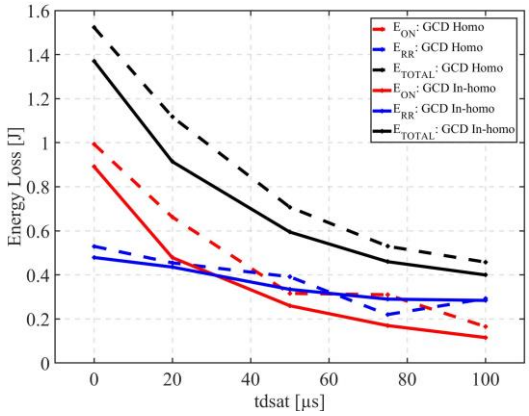

Fig. 12. Overall turn on loss comparison of low-saturation mode, distinguishing homogeneous and inhomogeneous GCD's E_{RR}, E_{ON}, E_{TOTAL} for tdsat= 0µs, 20µs, 50µs, 75µs, 100µs. V_{DC} = 3.6 kV, j_{nom} = 82 A/cm^2, T = 150 °C, L_S = 1.6µH, P_{RR} = 150 kW.

Fig. 12. shows the energy loss reduction (E_{TOTAL}, E_{ON}, E_{RR}) dependency on tdsat in low-saturation mode, for both homogeneous and inhomogeneous GCD. As the static I-V characteristics of homogeneous and inhomogeneous GCD is kept similar, their loss profile appears similar. A 70 % overall reduction in loss is observed between 0 µs and 100 µs. For a 6.5 kV voltage class bi-polar device, irrespective of IGBT or diode, the desaturation time required for optimal loss reduction is about 50-100 µs.

Similarly, Fig. 13, shows the tdsat dependency of loss reduction on both homogeneous and

inhomogeneous diode in high-speed mode. The stored charge during conduction in high-speed mode is considerably less than in the low-saturation mode, which is reflected in loss distribution at 0 µs, with around half the losses of low-saturation mode. Even in high-speed mode, loss reduction is observed with increasing tdsat, though not as significant as in low-saturation mode. With tdsat application, round about 50 % reduction in overall losses in noted in both homogeneous and inhomogeneous diode in high-speed mode.

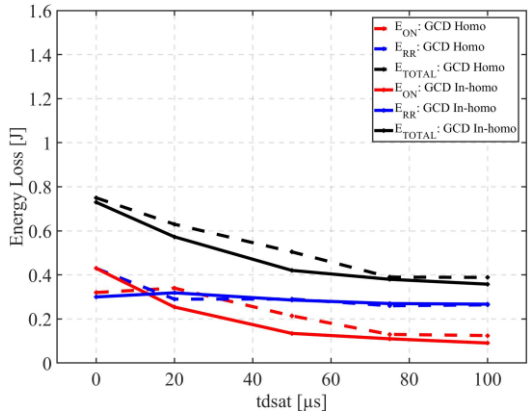

Fig. 13. Overall turn on loss comparisonin of high-speed mode, distinguishing homogeneous and inhomogeneous GCD's E_{RR}, E_{ON}, E_{TOTAL} for tdsat= 0µs, 20µs, 50µs, 75µs, 100µs. V_{DC} = 3.6 kV, j_{nom} = 82 A/cm^2, T = 150 °C, L_S = 1.6µH, P_{RR} = 150 kW.

It is noted that after tdsat of 50 µs, the reverse recovery losses of diode saturate, but losses on IGBT keeps lowering. To keep better softness of diode during turn-off, the charge carriers on the cathode side is kept high like in a reference diode. There is no control on cathode to remove this stored charge. Irrespective of any tdsat application, the cathode side plasma cannot be reduced further, and this is reflected on E_{RR} curve which stagnates around 0.3 J. A similar behaviour is observed in low-saturation mode. After about 75 µs, E_{RR} saturates around 0.3 J and loss reduction occurs only on the IGBT.

The characteristics of GCD at higher positive V_{GA} and longer tdsat pulse range has a negative influence on the dj_F/dt. From the Fig. 10, we notice the GCD at V_{GA} +15 V, runs into uni-polar mode with a high forward voltage drop. It is observed that during uni-polar mode, with application of longer tdsat times, dj_F/dt increases to high value reducing only the losses on IGBT drastically with minimal change in Q_{RR}. Fig. 14, shows variation in dj_F/dt and effect on Q_{RR} and E_{ON} for different gate drive conditions in low-saturation mode of inhomogeneous GCD. The last points on the right of the figure shows high dj_F/dt, in the order of 300 A/µs. The driving conditions for the three scenarios are higher tdsat and higher V_{GA}. The driving condition with either higher tdsat of 150 µs at V_{GA} +10 V or 100 µs at V_{GA} +13 V have a moderate dj_F/dt, and loss reduction is in the similar range of extreme dj_F/dt cases. Both homogeneous and inhomogeneous GCD behaves the same way. To infer from this, application of longer tdsat time in uni-polar mode of GCD must be avoided.

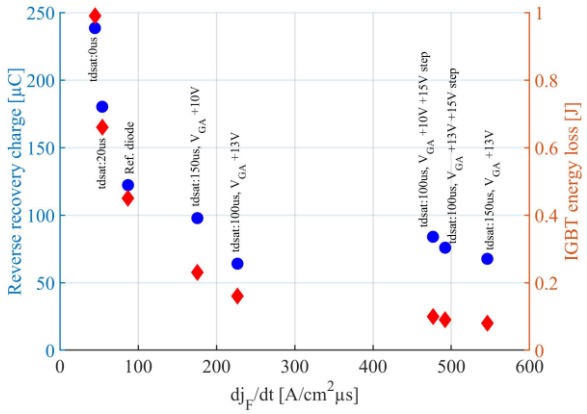

Fig. 14. dj_F/dt vs Q_{RR} vs Losses comparison of inhomogeneous GCD in low-saturation mode at different driving condition. V_{DC} = 3.6 kV, j_{nom} = 82 A/cm^2, T = 150 °C, L_S = 1.6µH, P_{RR} = 150 kW.

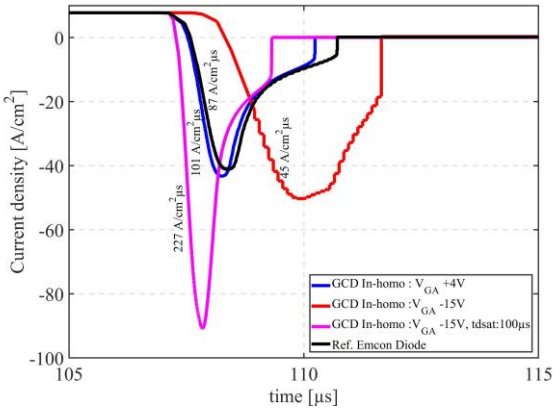

Fig. 15. Reverse recovery behaviour of inhomogeneous GCD, L_S = 1.6 µH, V_{DC} = 4.5 kV, j_{nom} = 8 A/cm^2, T = 25 °C.

As seen from the charge carrier density in Fig. 10, GCD at V_{GA} -15 V is designed for -dn/dx. This will lead to a snappy reverse recovery

behaviour. This is evident from the Fig. 15, where simulated reverse recovery waveforms are shown at 0.1*j_{nom} at 25 °C. The reverse recovery waveforms for GCD at V_{GA} +4 V or GCD V_{GA} -15V with 100 µs tdsat shows a soft turn-off behaviour like the reference diode.

The influence of changing diode current on tdsat was studied in previous paper, the same analysis can be extended in this case. Robustness of the submicrometric trench, in terms of shielding the electric field from reaching anode contact was also shown in paper [4]. The effect of p-cathode for ease of holes extraction, its effect on softness and the GCD short-circuit dependency was also studied in previous paper.

Conclusion

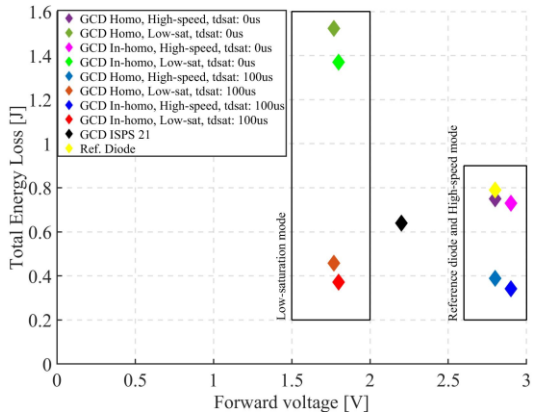

Fig. 16. Trade-off behaviour of homogeneous and inhomogeneous GCD, V_{DC} = 3.6 kV, j_{nom} = 82 A/cm^2, T = 150 °C.

A gate controllable diode concept was proposed in the previous paper. The static and dynamic characteristics of GCD is further improved in this paper, which can be seen from trade-off curve shown in Fig. 16. Along with that, the effects of n-buffer and inhomogeneity in doping of GCD were studied. Desired low-saturation mode and high-speed mode were established for an efficient operation of MMC sub-module in 6.5 kV HVDC system. It can be seen; a massive 70 % reduction of overall losses is seen in low-saturation mode. Around 50 % reduction in losses is seen in high-speed mode. This holds good wrt., reference diode as well, because both high-speed mode and reference diode have similar characteristics. Thus, a low forward voltage diode is designed, and homogeneous and inhomogeneous GCD is established.

Acknowledgments

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