New Power MOSFET and their use in Intermediate Bus Converters

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Abstract

This work investigates the performance of our latest trench power MOSFET technology in an Intermediate Bus Converter as widely used in telecom and data centre power supplies. Based on the advantages of a revolutionary new cell design combined with the benefits of an advanced manufacturing technology, the new devices combine the benefits of low conduction losses and superior switching performances with an extended SOA and good ruggedness. These features make the devices an ideal fit especially for high switching frequency applications. The recent release of 80 V and 100 V devices offers the potential for further optimization.

Keywords: power semiconductor, charge compensation, MOSFET, SMPS, IBC

INTRODUCTION

Since their introduction, MOSFET technologies have been noted as excellent candidates to be used as switches in power management circuits [1-9].
Vertical diffused MOSFET (VDMOS) structures, commercially available since the late seventies, first addressed the needs of a power switch (Fig. 1a) [1]. The superior switching performance together with a high input impedance placed the MOSFET as an attractive alternative to the bipolar technologies that dominated the power semiconductor arena at the time.
Nevertheless, the high on-state resistance limited the current-handling capabilities of the VDMOS and hence its use in power electronics applications. For medium-voltage devices, the total on-state resistance between drain and source was set by the intrinsic channel resistance, and by the JFET region between the body regions that limits the channel current flow into the drift region (Fig. 1a).
It took more than a decade of development in device design and process engineering to overcome these limitations in the late 1980s with the commercialization of the first trench gate power MOSFETs, which set a milestone for the broad adoption of field-effect transistors in the power electronics industry [1,10]. By aligning the channel along the vertical direction, the JFET region was virtually eliminated and the cell pitch dramatically reduced (Fig. 1b). The ultralow specific channel resistance achieved no longer prevented low on-state resistances, although as a result the substrate and

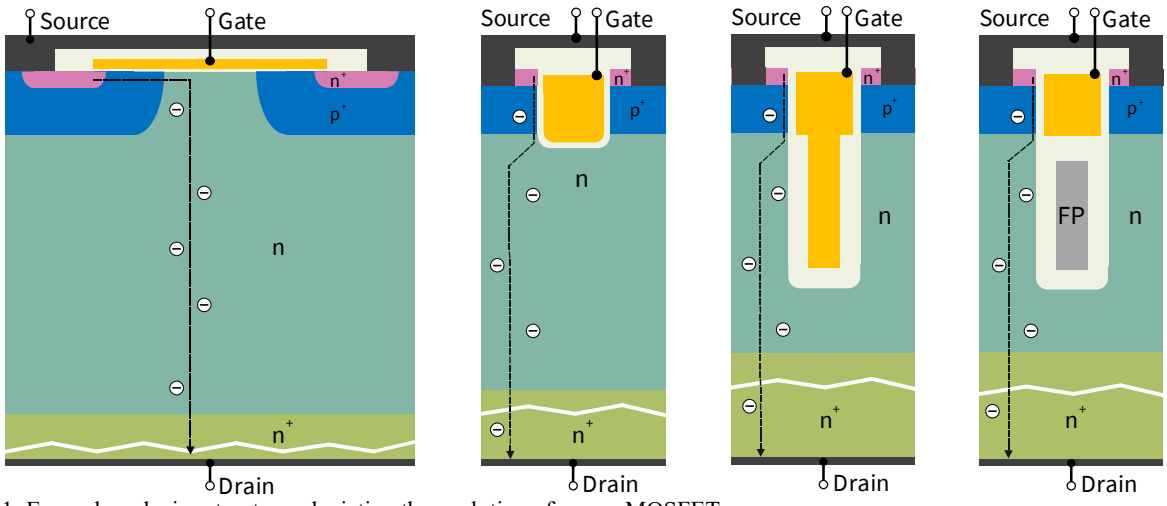

Fig. 1: Exemplary device structures depicting the evolution of power MOSFET:
a) VDMOS structure with lateral channel and planar gate
b) Trench MOSFET structure with vertical channel
c) Trench MOSFET with lateral charge-compensation by a gate-connected field plate
d) Trench MOSFET with lateral charge-compensation by an insulated field plate connected to source

package resistances became more significant contributors.
However, the remarkable increase in cell density has also brought to light significant disadvantages. The gate-drain capacitance and gate-source capacitance both increase linearly with the number of trenches, i.e. with the cell density. Together with a sublinear scaling in the on-resistance $R_{DS(on)}$, this significantly impacts the technology figure-of-merit $FOM_G = R_{DS(on)} \times Q_G$.
Since the MOSFET is uniquely controlled through its gate terminal, the gate driver circuitry has to provide the total gate charge Q_G required to turn on the transistor. In the case of high switching frequency applications, as found for switched-mode power supplies (SMPS), the lowest gate charge is desirable since it proportionally reduces the driving losses. A part of the total gate charge is associated with the gate-to-drain charge Q_{GD}, which governs the drain voltage transient. Larger values of the Q_{GD} impact the transient speed, result in an increase of the switching losses, and additionally force the use of longer dead-times. Additionally, another constraint is imposed by the Miller charge ratio: Q_{GD}/Q_{TH} must be lower than one. This is needed in order to ensure an intrinsic robustness against parasitic turn-on of the MOSFET under fast drain voltage transients [11].
The introduction of charge-compensated structures, exploiting the same principle as super junction devices, marked the beginning of a new era. The introduction of devices employing an insulated deep field plate as an extension of the gate electrode enabled the lateral depletion of the drift region in the off state (Fig. 1c) [2]. The lateral depletion alters the electric field distribution throughout the structure, and it is possible to block the same voltage within a shorter length. In turn, the electric field can now be supported by a thinner and more heavily doped drift region, which leads to a substantial reduction in the on-state resistance.
Unfortunately the field plate as an extension of the gate electrode leads to a significant increase of the gate-drain capacitance C_{GD} (hence also Q_{GD} and Q_G) and a nonlinear dependence on the drain voltage. This causes a sharp drop in the transfer capacitance as soon as the mesa region completely depletes.
These disadvantages were soon overcome by the use of a separated field plate, which was isolated from the gate electrode and instead electrically connected to the source potential (Fig. 1d). While the charge compensation principle operates as before, the buried field plate does not introduce any additional contributions to the gate-drain capacitance. Instead, the field plate shields the gate electrode from the drain potential, which reduces the gate-drain capacitance C_{GD} and related charges.
These devices, at the time of their introduction to the market, showed best-in-class performance with low gate charge and gate-drain charge characteristics, high switching speeds and good avalanche ruggedness [3]. While the presence of the field plate comes with the disadvantage of an increased output capacitance C_{OSS} and output charge Q_{OSS} (a consequence of the lateral charge-compensation), a careful device optimization enabled field plate-based power technologies with $FOM_{OSS} = R_{DS(on)} \times Q_{OSS}$ comparable to those of the standard trench MOSFET [12,13].

THE NEW MOSFET TECHNOLOGY.

Novel Cell Concept

New MOSFET devices are required to provide improvements across all figures of merit, as this is needed to enable high-frequency SMPS operation where losses are associated both with charges (switching) and on-state resistance (conduction). To meet these requirements, a novel cell-design approach was developed, which explores a true three-dimensional charge compensation.
State-of-the-art MOSFET technologies currently use an insulated deep field plate underneath and separated from the gate electrode. The gate electrodes employ a stripe

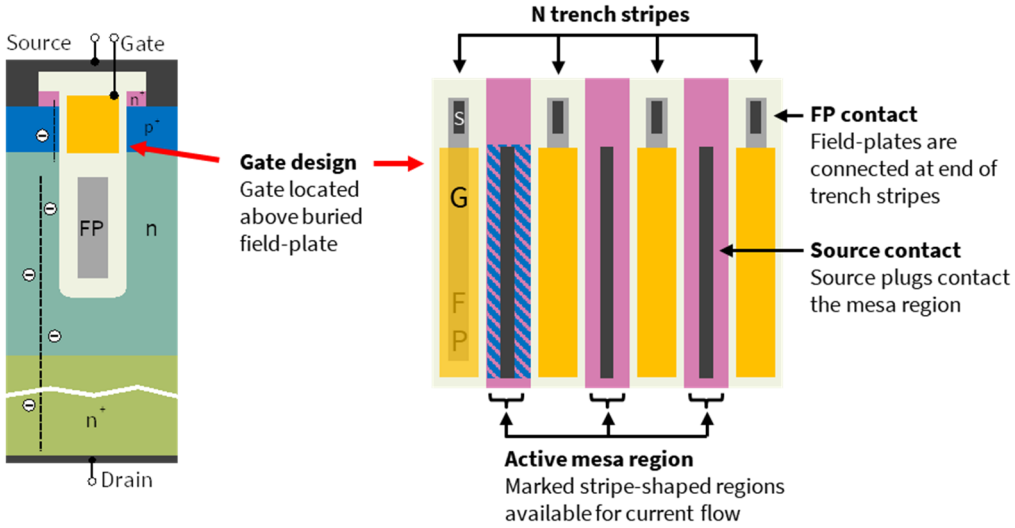

Fig. 2: Typical Trench MOSFET structure with lateral charge-compensation by an insulated field-plate connected to source (left) and commonly employed stripe layout approach in the chip design (right)

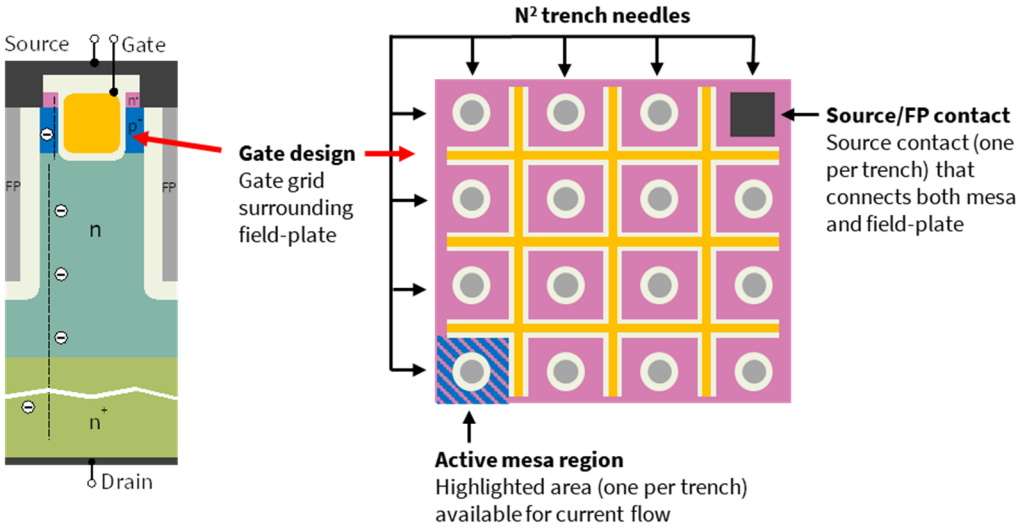

Fig. 3: Trench MOSFET structure with lateral charge-compensation by an insulated field-plate and separated gate trench (left) and the new grid-like layout approach in the improved chip design (right)

layout as depicted in Fig. 2. The new generation separates the field plate trench, which is now formed with a needle-like structure, from a grid like gate trench which surrounds the needles [14]. Fig. 3 depicts this changed layout and schematic cell cross section. This increases the silicon area available for current conduction, allowing for a further reduction in the overall on-resistance [14]. In order to further reduce the $FOM_G = R_{DS(on)} \times Q_G$ and $FOM_{GD} = R_{DS(on)} \times Q_{GD}$ values, the gate trench underwent a complete redesign to minimize its lateral extension. Fig. 4 summarizes the gained improvements in device parameters on product level.

However, the substantially shrunk dimensions of the gate impose a new challenge. The use of common polysilicon as gate material would result in unacceptably large internal gate resistances. Large values for the internal distributed gate resistance lead to a slowed-down switching behaviour, increased switching losses and inhomogeneous switching across the chip which may reduce device ruggedness, hence it is mandatory to avoid such an increase.

The introduction of gate fingers represents a common solution to reduce the chip's internal gate resistance. The disadvantage of this measure is a reduction of the available active area due to the space consumed, linked to an increase of the products on-resistance especially for smaller die and the use of several gate fingers. Fig. 5 illustrates this correlation between gate resistance and active area loss for a best-in-class chip in a PQFN 3.3 x 3.3 mm² package.

To avoid this loss in active area, a metal gate system was developed [14]. This not only eliminates the need for gate fingers, but also improves the gate resistance uniformity across the chip.

Improvements in device switching behaviour

Simulation approach. The new device concept offers substantial benefits in switching performance, providing reductions in the switching losses under both hard and soft switching conditions. The metal gate in combination with the use of a gate grid layout, together with a direct connection of the field-plates to the source metal, realizes a device set-up that ensures a very fast and homogeneous transition at turn-on and turn-off. This not only minimizes switching losses, but also reduces the risk of an unwanted dv/dt induced parasitic turn-on of the MOSFET. To enable an understanding of the differences

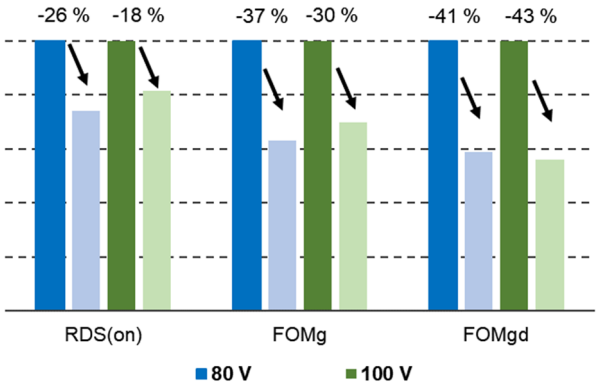

Fig. 4: Improvement of device parameters for best-in-class devices in the PQFN 5x6 package

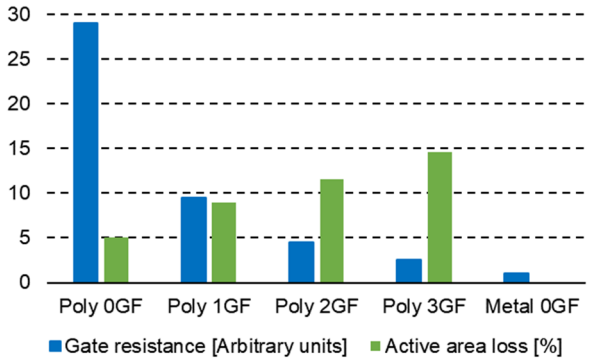

Fig. 5: Reduction of gate resistance with the number of gate fingers (GF) and lost active area loss [14]

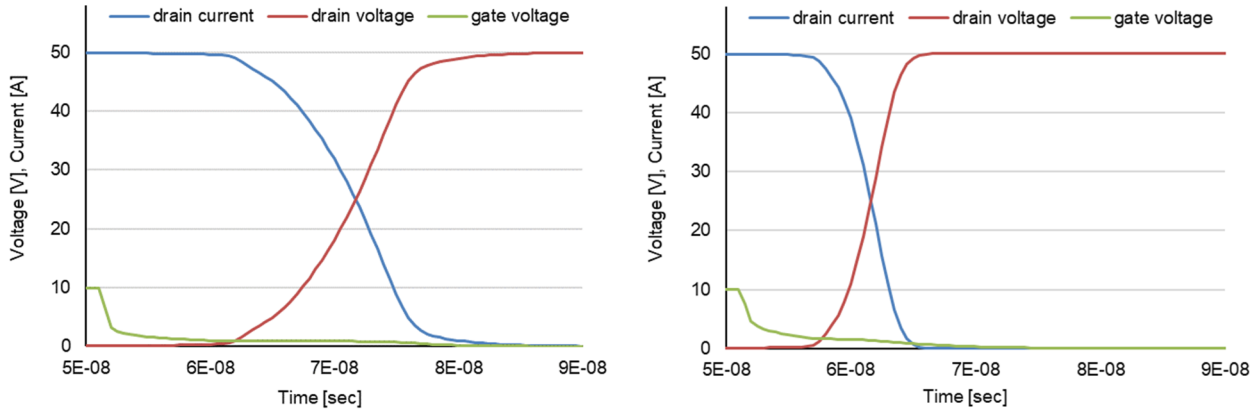

Fig. 6: Comparison of the simulated turn-off characteristics of the previous (left) and new (right) device technologies

in the switching behavior between a traditional stripe layout and the grid layout approach used in the new technology, the potential distribution during the switching of the device is studied based on circuit simulations representing the chip. This approach uses a distributed SPICE model of the transistor and connects 25 x 30 transistor elements within a grid network, which extends across the chip in both directions. The connections between local gate, source and field-plates are modelled by resistive elements.

The values of the resistors represent the material properties of the material used and the geometric dimensions of the respective electrode or layer. The transistor cells, which are located on the crossing points of the resistor network, scale with the fraction of the chip area that results from the chosen number of elements in the grid. Other functional elements, like the gate-pad or gate and source runners, are added to the circuit as necessary for a more precise description of the chip.

Simulation results. A transient simulation of the distributed SPICE model now allows a realistic study of the chip behavior. In contrast to the case of simple RC networks, this approach includes full device models for active cells. As such, this approach correctly considers the voltage-dependence of capacitances as well as feedback effects due to the miller capacitance, and yields the local signal propagation over the chip. Fig. 6 shows the simulated turn-off waveforms for the two approaches, assuming for both cases a chip size of 12 mm². The characteristics show that the new technology with the grid-like gate layout enables a shorter delay time, and clearly switches faster. It only needs approximately half the time of the previous generation.

Figs. 7 & 8 give the simulated distribution of the gate and field-plate potential across the chip for the predecessor technology with a common stripe layout, and for the new technology with a grid-like layout, at several points in time with reference to the waveforms shown in Fig. 6.

In the case of the stripe design, the gate potential over the chip clearly reveals inhomogeneous distributions during the first half of the turn-off process. The gate potential is highest in the middle of the chip where the distance to the gate runners at the upper and lower side of the chip is largest. During the second half of the turn-off process, it is the field-plate potential distribution that becomes strongly inhomogeneous, with the highest potential at the upper and lower sides of the chip where the distance to the source runner in the middle of the chip is biggest.

Due to the combination of a metal gate with the gate grid layout, the new device shows a clearly improved homogeneity of the gate potential across the chip, supporting faster switching of the chip. The strongly improved homogeneity of the gate potential is also advantageous for device robustness, for example avalanche ruggedness, by reducing the probability that a part of the chip is affected by gate signal delays [15] or parasitic turn-on. In former transistor generations, both gate signal delay and parasitic turn-on degrade the device ruggedness as power dissipation is limited to just a part of the chip.

The distribution of the field-plate potential across the chip is actually completely flat for the new device approach. This supports fast transitions and is beneficial for achieving a high avalanche ruggedness, as an increased local field-plate potential may alter the local breakdown voltage [16] and can lead to an inhomogeneous power dissipation over the chip area. The direct connection between the source and field-plate also minimizes resistive losses while charging and discharging the output capacitance.

IMPACT ON CONVERTER EFFICIENCY

The Intermediate Bus Converter

The Intermediate-Bus Converter (IBC) is the only isolated converter in the intermediate-bus architecture (IBA) of a typical telecom power supply, as depicted in Fig. 9. The IBC operates as a pre-scaling converter followed by point-of-load (POL) step-down converters. This architecture is popular in telecom and server applications, where DSP chips and microcontrollers which operate at very low voltages (1.2 V … 5 V) are powered locally by the POL converters, yielding a more efficient system [17].

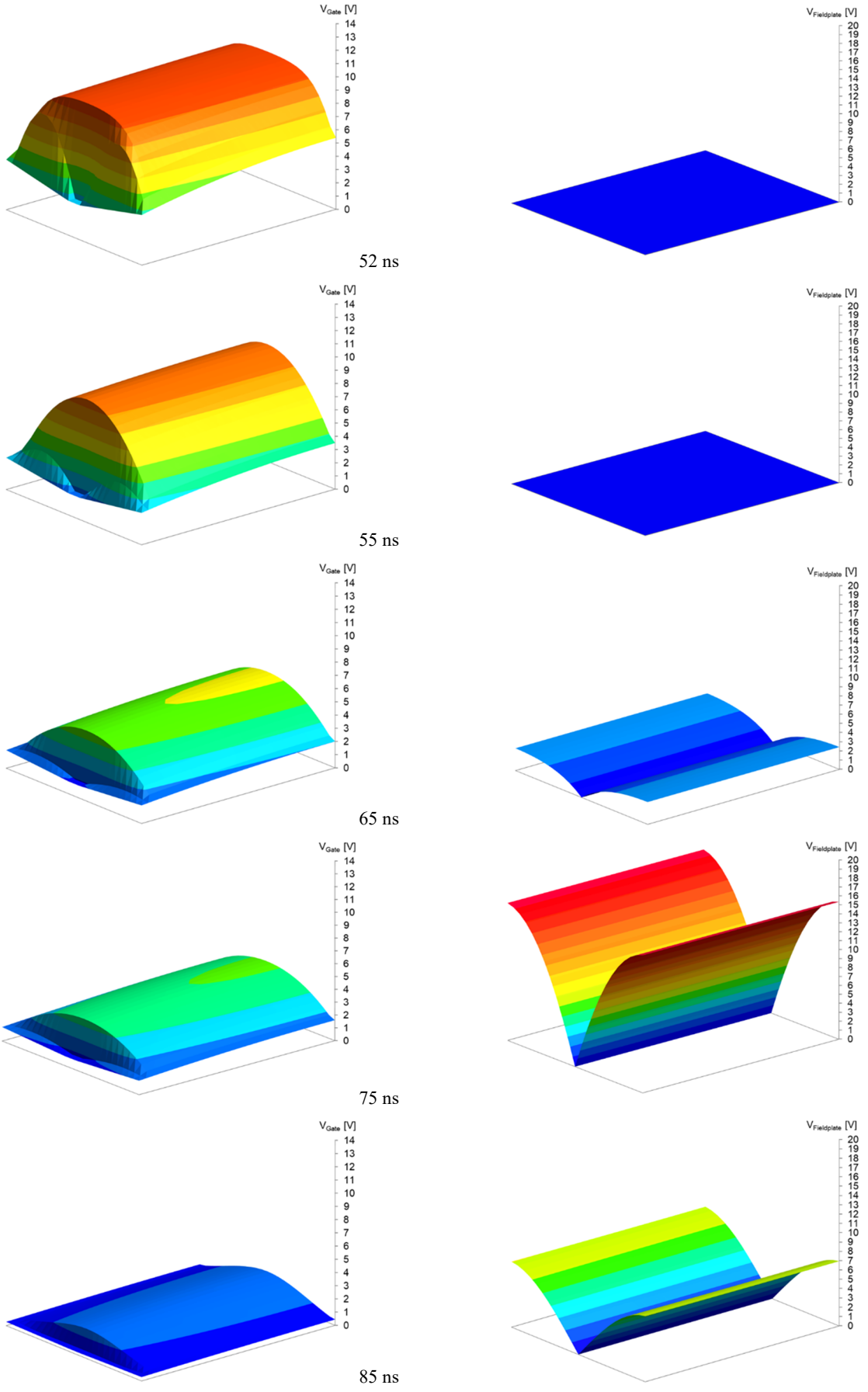

Fig. 7: Distribution of gate (left) and field-plate (right) potential at different points in time for the previous device technology with a stripe layout

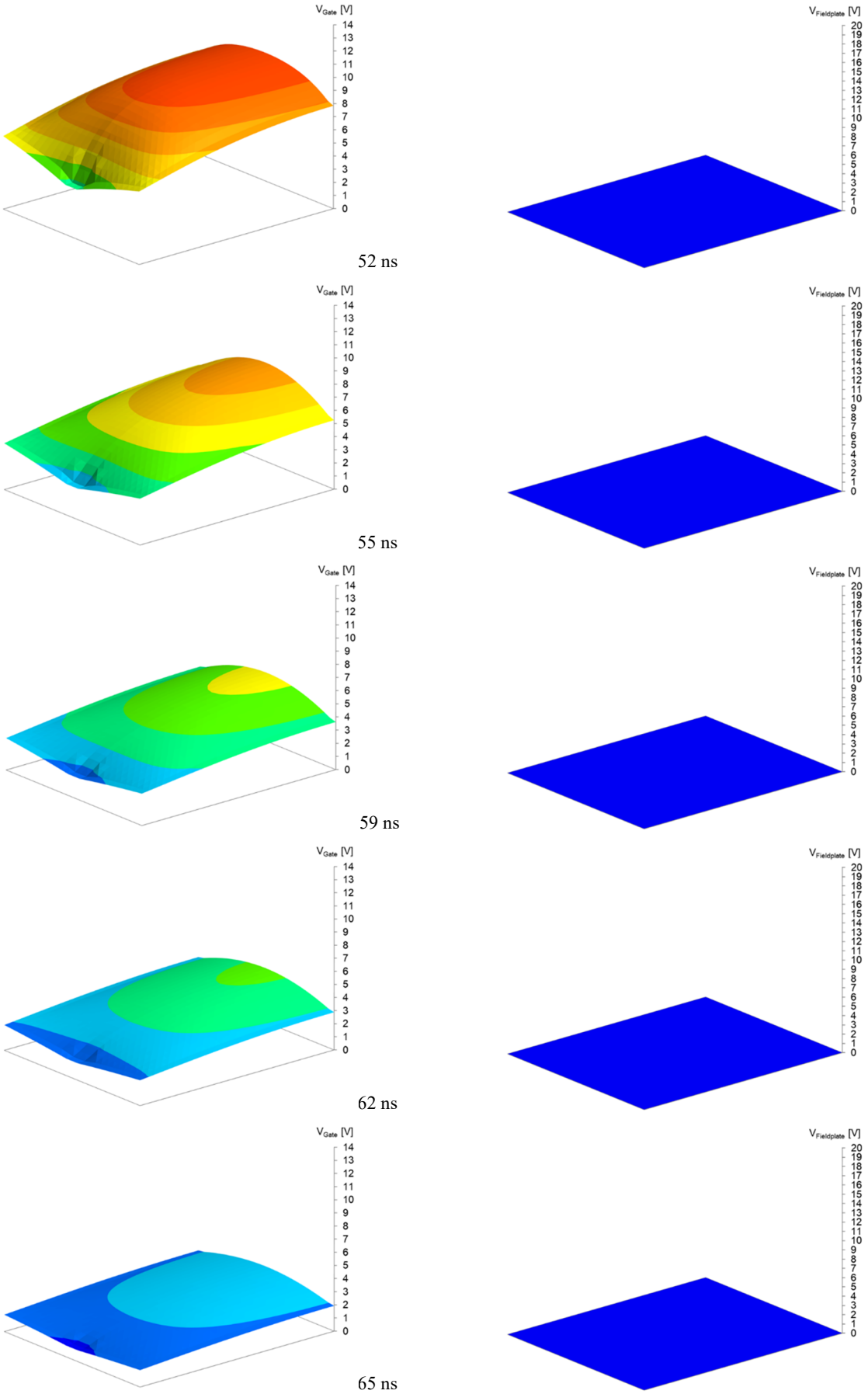

Fig. 8: Distribution of gate (left) and field-plate (right) potential at different points in time for the new device technology with a grid-like layout

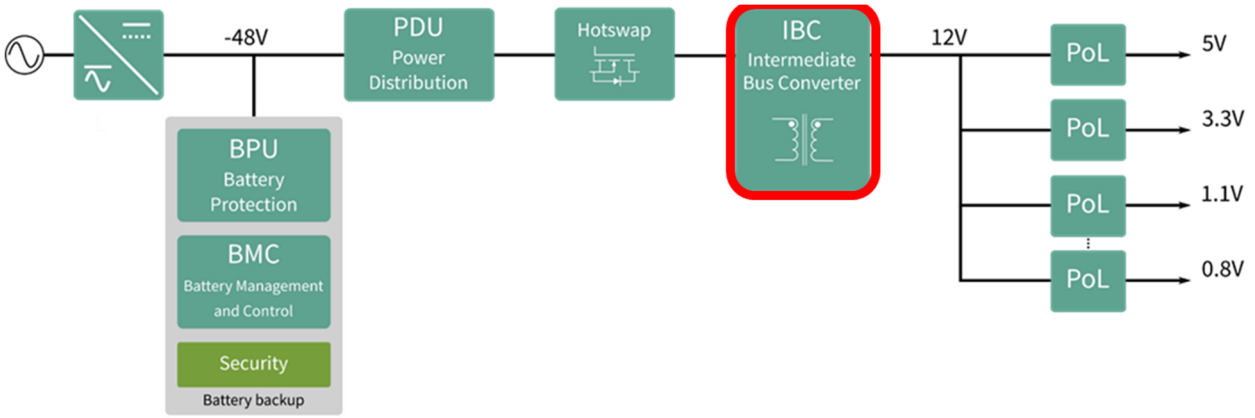

Fig. 9: Simplified schematic representation of a typical telecom power system based on the Intermediate Bus Architecture (IBA)

There are two cascaded converters between the front-end power supply and the IBA load: the IBC and the POL converters. The IBA system must operate with high efficiency, and this requires the IBC converter to have an extremely high efficiency. For common 48 V telecom and datacom systems, the front-end power-supply voltage ranges from -40.5 V to -57 V [18].
To realize the IBC, one can in principle choose from different topologies, which can be either hard switching or resonant.

600 W IBC board for telecom applications

In this work, the efficiency of the devices is studied in a DC/DC converter as typically used in telecom and datacom power systems. The converter uses a hard-switching full-bridge (FB) topology on the primary side, and a centre-tapped (CT) synchronous rectifier (SR) on the secondary side. Fig. 10 illustrates the basic converter schematic.
Thanks to the continuous improvement in MOSFET technologies leading to a stunning power density increase, the IBC in a standard quarter-brick form factor can deliver 600 W. The board operates with a switching frequency of 250 kHz, and the operating input voltage is allowed to vary between 36 V and 75 V. The turns ratio of the transformer is 3:1. Fig. 11 shows the top and bottom of the realized test board. The primary side devices on the board are marked by the red rectangle while the secondary side devices are indicated by the blue rectangle.
Now that the new devices in the 80 V voltage class are available, it is possible to study the efficiency using MOSFETs with an optimal voltage rating.
For this comparison, the primary side employs 100 V devices BSC035N10NS5 with 3.5 mΩ of the previous technology OptiMOS 5 ™, or ISC030N10NM6 3.0 mΩ in case of the new technology OptiMOS 6 ™. Both devices come in PQFN 5 x 6 mm² packages.
The secondary side is equipped with 80 V MOSFETs, either four paralleled devices BSC040N08NS5 with 4.0 mΩ of the established technology OptiMOS 5 ™, or four paralleled devices ISZ053N08NM6 with 5.3 mΩ of the new technology OptiMOS 6 ™. While the OptiMOS 5 ™ devices come in a PQFN 5 x 6 mm² package, the new technology enables the use of the smaller PQFN 3.3 x 3.3 mm² package.

Test results

Fig. 12 is a comparison of the measured efficiencies for both technology generations. The solution using the new generation of devices yields an impressive efficiency improvement of 0.35 % at full load, and an even more remarkable increase of 0.75 % at 20 % load in comparison with the previous generation.
The maximum temperature at the hotspot of the converter on the primary side reduces by 9°C (Fig. 13). On the

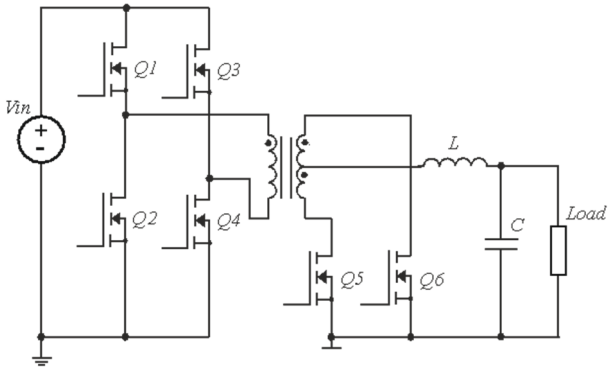

Fig. 10: Basic schematic of the 600 W isolated DC/DC IBC test board in FB-CT configuration

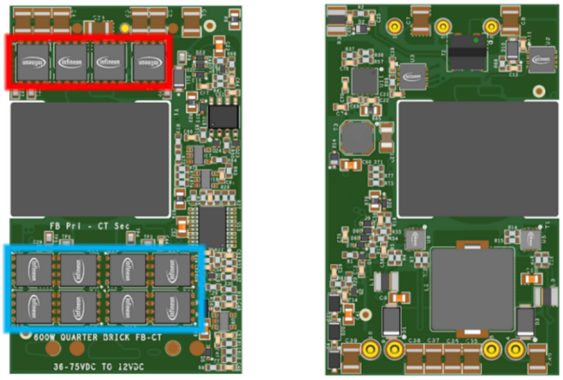

Fig. 11: Top and bottom view of the 600 W IBC test board, red: primary side MOSFET, blue: secondary side MOSFET

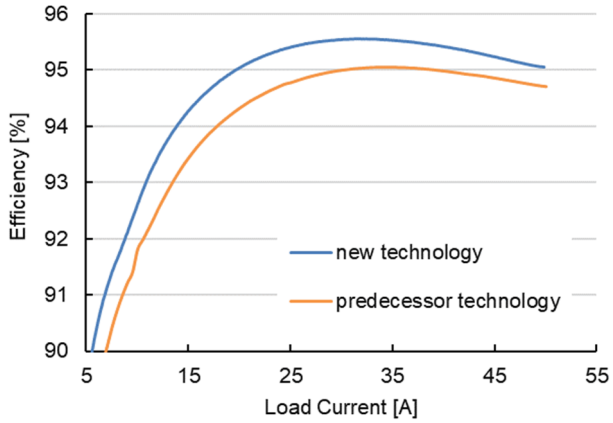

Fig. 12: Overall efficiency of the 600 W IBC comparing the previous and new technology generations

secondary side, despite the use of smaller devices with a clearly reduced footprint, the temperature still reduces by 2°C (Fig. 14).

This remarkable increase in the converter efficiency results from the lower gate charge Q_G and gate-drain charge Q_{GD} of the latest technology devices, and further benefits from a lowered reverse-recovery charge Q_{RR}.

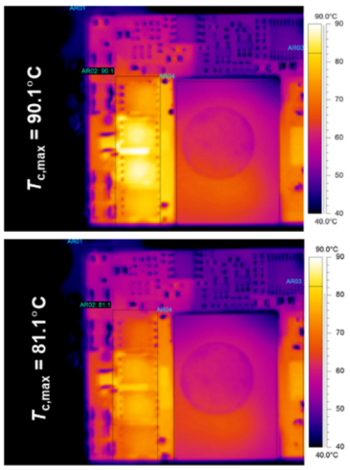

Fig. 13: Maximum temperature for using the predecessor (top) and new 100 V technology (bottom) on the primary side

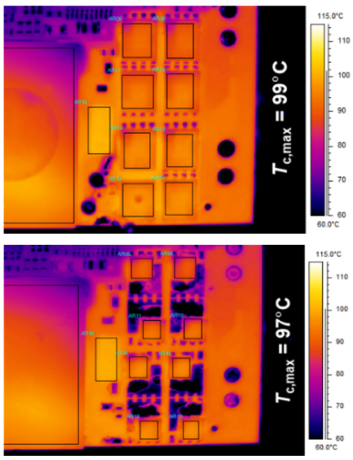

Fig. 14: Maximum temperature for using the predecessor (top) and new 80 V technology (bottom) on the secondary side

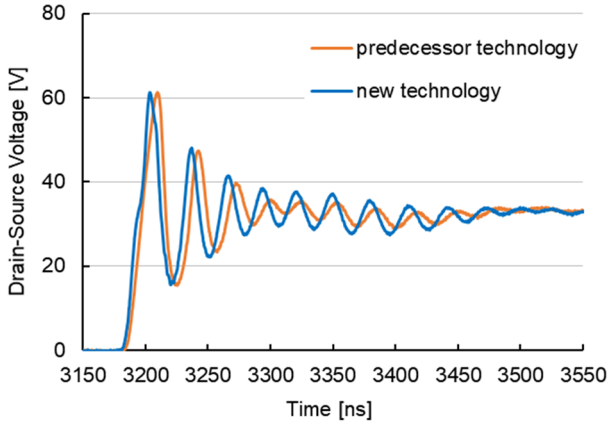

Fig. 15: Comparison of the drain-source-voltage waveforms of the secondary-side SR MOSFET (V_{IN} = 48 V, I_{LOAD} = 12.5 A)

Fig. 15 compares the waveforms of both technologies measured across the SR MOSFET on the secondary side at 20 % load.

CONCLUSION

This work introduces the 100 V and 80 V voltage classes of our latest power MOSFET technology family OptiMOS 6™. This new technology realizes improvements in all important device parameters and combines the benefits of low on-state resistance with superior switching performance. The new technology is specifically optimized for high switching frequency applications such as telecom and datacom SMPS.

The remarkable progress in the overall device performance is enabled by substantial improvements at the device technology level. This has culminated in a unique device structure, which is the first to employ three-dimensional charge compensation combined with the first ever use of a metal gate in a trench power MOSFET. As explained by means of circuit simulations reflecting the chip layout, the new design provides a so-far unmatched homogeneity of the dynamic potential distributions across the chip.

The reduction achieved in the on-resistance, the dramatically lowered gate and gate-drain charges, the low output charge and the improved switching homogeneity across the device area promises to enhance the system efficiency across all load conditions. The new device structure is also beneficial for the behaviour of the internal body diode of the MOSFET. Because the silicon area conducting the current is increased, the body diode current density is decreased which, for the same current level, translates into a decreased reverse recovery charge. Efficiency measurements in a 600 W intermediate bus converter board for telecom applications confirm the findings at the semiconductor device level. The efficiency improves by up to 0.75 %, depending on the load condition.

The much better device performance further enables the use of smaller footprints, without having a negative

impact on the temperature of the devices. Overall, these improvements offer significant efficiency gains in the demanding telecom power arena as well as in other application fields.

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REFERENCES

[1] Williams, R.K., Darwish, M.N., Blanchard, R.A., Siemieniec, R., Rutter, P., and Kawaguchi, Y.: The Trench Power MOSFET: Part I - History, Technology, and Prospects, IEEE Transactions on Electron Devices, 2017, Vol. 64, No. 3, pp. 674-691

[2] Ejury, J., Hirler, F., and Larik, J.: New P-Channel MOSFET Achieves Conventional N-Channel MOSFET Performance, in Proc. PCIM 2001, Nuremberg, 2001

[3] Schlögl, A., Hirler, F., Ropohl, J., Hiller, U., Rösch, M., Soufi-Amlashi, N. and Siemieniec, R.: "A new robust power MOSFET family in the voltage range 80 V-150 V with superior low RDSon, excellent switching properties and improved body diode", in Proc. EPE 2005, Dresden, 2005

[4] Pattanyak, D.: "Low Voltage Super Junction technology", in Proc. ISPS 2006, Prague, 2006

[5] Yedinak, J., Probst, D., Dolny, G., Challa, A. and Andrews, J.: "Optimizing Oxide Charge Balanced Devices for Unclamped Inductive Switching (UIS)", in Proc. ISPSD 2010, Hiroshima, 2010

[6] Roig, J., Lee, D., Bauwens, F., Burra, B., Rinaldi, A., McDonald, J. and Desoete, B.: "Suitable Operation Conditions for Different 100V Trench-Based Power MOSFETs in 48V-input Synchronous Buck Converters", in Proc. EPE 2011, Birmingham, 2011

[7] Hossain, Z., Burra, B., Sellers, J., Pratt, B., Venkatram, P., Loechelt, G. and Salih, A.: "Process & design impact on BVDSS stability of a shielded gate trench power MOSFET", in Proc. ISPSD 2014, Waikkoloa, 2014

[8] Kobayashi, K., Nishiguchi, T., Katoh, S., Kawano, T. and Kawaguchi, Y.: "100 V class multiple stepped oxide field plate trench MOSFET (MSO-FP-MOSFET) aimed to ultimate structure realization", in Proc. ISPSD 2015, Hong Kong, 2015

[9] Park, C., Havanur, S., Shibib, A. and Terrill, K.: "60 V rating split gate trench MOSFETs having best-in-class specific resistance and figure-of-merit", in Proc. ISPSD 2016, Prague, 2016

[10] Chang, H.R., Black, R.D., Temple, V.A.K., Tantraporn, W. and Baliga, B.J.: "Self-aligned UMOSFET's with a specific on-resistance of 1 mΩ cm^2", IEEE Transactions on Electron Devices, 1987, Vol. ED-34, No. 11, pp. 2329–2334

[11] Singh, P.: "Power MOSFET Failure Mechanisms", in Proc. INTELEC 2004, Chicago, 2004

[12] Siemieniec, R., Mößlacher, C., Blank, O., Rösch, M., Frank, M. and Hutzler, M.: "A new Power MOSFET Generation designed for Synchronous Rectification", in Proc. EPE 2011, Birmingham, 2011

[13] Ferrara, A., Siemieniec, R., Medic, U., Hutzler, M., Blank, O. and Henson, T.: "Evolution of reverse recovery in trench MOSFETs", in Proc. ISPSD 2020, Vienna, 2020

[14] Siemieniec, R., Hutzler, M., Braz, C., Naeve, T., Pree, E. Hofer, H., Neumann, I., Laforet, D.: A new power MOSFET technology achieves a further milestone in efficiency, in Proc. EPE 2022, Hannover, 2022

[15] Pawel I., Siemieniec R., and Rösch M.: Multi-Cell Effects during Unclamped Inductive Switching of Power MOSFETs, in Proc. MIEL 2008, Nis, 2008

[16] Pawel I., Siemieniec R., and Born M.: Theoretical Evaluation of Maximum Doping Concentration, Breakdown Voltage and On-state Resistance of Field-Plate Compensated Devices, in Proc. ISPS 2008, Prague, 2008

[17] Li, S.: Intermediate Bus Converters for High Efficiency Power Conversion: A Review, in Proc. TPEC 2020, College Station, 2020

[18] ETSI (2016.10): Power supply interface at the input to telecommunications and Datacom (IST) equipment; Part 2: Operated by -48V direct current (DC), EN 300 132-2

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