Press Pack IGBTs for MVDC-breaker Applications

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Abstract

With the rising demand for higher power densities and robust system control, the need for using press pack IGBT (PPI) devices in medium voltage (MV) applications is also increasing. So far PPI manufacturers have majorly focused on devices with paralleling of IGBTs/diodes inside a single housing, that drives thousands of Amperes and is used for high-power switching in various converter applications, like High Voltage Direct Current (HVDC), Flexible Alternating Current Transmission Systems (FACTS), and MV drives.

However, the absolute capabilities of a single chip are yet to be intensively explored for applications that do not require fast turn off, standard ±15 V gate voltage, and continuous switching, such as MV-DC-breaker.

The idea of this work is to investigate the boundaries and robustness of a single chip at higher gate voltage for all possible conditions and eventually realize an application out of it. The major focus of the work is on determining the maximum potential of the 4.5 kV trench IGBT chip at a gate voltage as high as 40 V. After performing several robustness and stability tests, it can be claimed that a single chip can turn off at least 12 times the nominal current after conducting about 10 milliseconds, a requirement which is very important for the DC hybrid circuit breaker.

Keywords: Press pack IGBT, Circuit breaker, MVDC, Surge current, High gate voltage applications

I. INTRODUCTION

As the demand for energy is rising around the world the way of transportation is also being reviewed. HVDC has been an alternative method of transmitting electric power from one location to another with some inherent advantages over AC transmission systems, such as lower losses and decoupling of networks for different frequencies or phase shift. The efficiency and rated power carrying capacity of direct current transmission lines depend highly on the converter used in transforming the current from one form to another (AC to DC and vice versa). This is the introduction of the voltage source converter to HVDC application and the demand for IGBTs has increased.

A. DC grids and DC breaker

Due to the trend of moving towards DC grids there is an increasing demand for DC circuit breakers, especially in mashed grids. Today's concepts for DC breakers for higher power ratings are mainly based on hybrid solutions, a combination of contactors and semiconductors which can be actively turned off. In Hybrid circuit breaker the load current is carried during normal ON operation by the vacuum interrupt switch (VIS). Only in case of switching, the current, I_{SS}, is taken by a semiconductor for up to 1 ms. Therefore, the function of the semiconductor is to conduct the current for up to 1 ms. and afterwards turn off the I_{SS} current. As semiconductors in a hybrid DC breaker today mainly use IGBTs as discrete devices or for higher power rating IGBT modules.

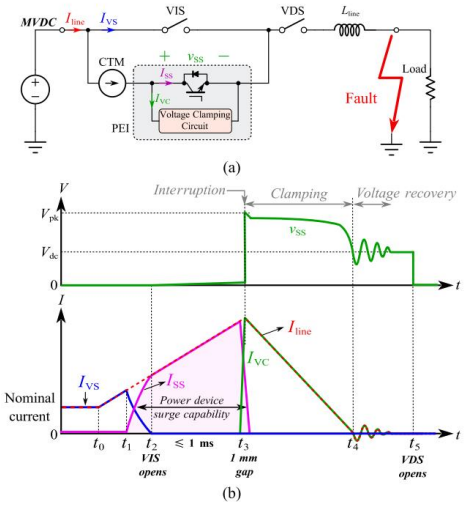


Fig. 1. (a) Hybrid circuit breaker unit with an IGBT-based system using a current transfer module (CTM) to enable current commutation from the VIS to the PEI branch. (b) Typical fault interruption waveforms of the hybrid circuit breaker. [8]

B. **Requirements for IGBTs in high current hybrid circuit breakers**

Today's state of the art IGBT modules are optimized for continuous operation in frequency converters. Therefore, the developments of the last decades are focussed on low losses, low thermal resistance, and high-power cycling capability. Now a new market of IGBTs for circuit breakers is emerging which has different requirements for the semiconductor. The main requirement is to conduct and switch off the highest current in the smallest area. A possible way to increase the maximum I_{SS} current of an IGBT is to increase the gate voltage during the on-state phase.

Due to the fact that the switching of a hybrid circuit breaker does not happen too often, the pulse for the IGBT can mainly be considered as a single pulse event. The power losses that occur during the pulse heat up the silicon and nearby components. For such low pulse operations, therefore, optimized cooling for continuous operation is not necessary. To increase the level of I_{SS} current, double-sided cooling for a short time is beneficial. To get a better understanding of the effect of double-sided cooling, Infineon's bipolar chip stack has been evaluated for the hybrid circuit breaker application.

II. New press pack IGBT

The first product of PPI is a 4.5 kV 3000 A device with 125 mm pole piece diameter. It contains 36 pieces of IGBT chip stacks. The innovative design of chip stack and housing technologies enables the creation of a perfect fitting portfolio with different current values and, in addition, with or without internal freewheeling diodes (FWD) to cover different applications and power ranges.

A. **IGBT chip technologies**

IGBT chip with a trench gate structure is designed to reduce conduction losses with negligible influence on the tail current and turn-off losses. It has been proven as an effective solution to minimize the saturation voltage of the IGBT chip. Another point, field stop technology is used to reduce the thickness of silicon for lower conduction resistance and higher blocking voltage, which also reduces the tail current and lowers the turn-off loss slightly. The IGBTs with trench gate and field stop technology have been in commercial production for many years already [5].

For this new press pack IGBT, the latest innovative 4.5 kV trench IGBT chip technology has been adopted. The same chip technology has been successfully used in the latest IGBT module generation for a long period of time. Only slight mechanical modifications needed to be performed to adapt the chip for use in press pack devices. One of the big improvements of the trench technology is of course the increase in maximum operating temperature from 125°C to 150°C of the IGBT chips. Besides this benefit, the conduction losses of the chips are decidedly reduced a lot compared to IGBT with planar technology. The typical on-state voltage is only 2.16 V under 25°C junction temperature and 2.70 V under 150°C junction temperature as shown in Fig. 2.

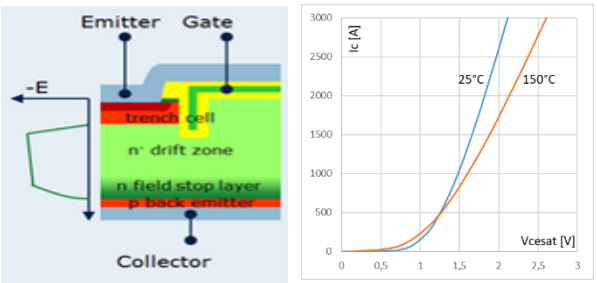


Fig. 2. The diagram of chip design (trench gate and field stop technology) and the typical output characteristic curve (Tj is 25°C and 150°C).

An IGBT, to be used in an Multi Modular Converter circuit, can be optimized for low switching frequency (50 ~ 150 Hz). Due to this and the technology curve of the silicon semiconductor, Vcesat can also be optimized for a low value. This reduces whole converter losses. In addition, reverse bias safe operating area (RBSOA) is enlarged by an optimized chip design that offers better IGBT robustness during turn-off in field applications [6].

B. **Chip stack by low temperature sintering (LTS)**

Due to its excellent conducting properties for heat and electric current, copper is the customary material for connecting high power semiconductors. However, there is a mismatch in thermal expansion between silicon and copper, which can lead to severe stress and ultimately to device failure if copper and silicon are attached directly. This is why, a layer of a better matching metal, usually molybdenum, is used to shield the silicon from the stress generated by the mismatch of thermal expansion. There are several options for joining silicon and molybdenum, such as free-floating, alloying, and sintering.

The free-floating (FF) assembly is the simplest configuration since the molybdenum is just put on both sides of the silicon and the contact is created by outside force. This is easiest to manufacture but increases thermal resistivity compared to other alternatives. Alloying offers better thermal performance but requires a process temperature of around 700°C. This leads to thermal stress inside the device and changes device behavior due to heavy modification on the alloyed surface. Besides this, the high process temperature results in changes inside the silicon, which is not acceptable. Therefore, for optimum device performance and reliability, silver sintering is recommended as the best solution. It is called low-temperature sintering (LTS). Here, a layer of silver is placed between silicon and molybdenum. Under high pressure and moderate temperatures (200 to 300°C) silver sintering creates links between the silicon, molybdenum, and each other, thereby creating a durable connection [7].

After the silicon is attached between two plates of molybdenum as a chip stack, the IGBT chip is well-protected from both thermal and mechanical stress. Due to the LTS process, the electrical data of this chip stack is stable under a wide range of pressures. This makes the semiconductor absolutely robust to check, at that level, static parameters as well as the electric dynamic robustness of the IGBT during turning on and off. The effort of conducting such tests at the chip level or free-floating arrangements is very high and can create a lot of scrap due to mechanical deviations. In addition, the tested electrical values can change a lot if the chip is connected again.

Within static and dynamic parameters, measurements of, for example, VGEth, VCEsat, Eon, Eoff, etc. made with similar parameters are recommended into one group for PPI assembly, which would ensure the static and dynamic current sharing among the IGBTs or diodes in one housing. Each chip stack is marked with an individual QR code on both surfaces to identify, thus a full traceability of chip-stacks is possible.

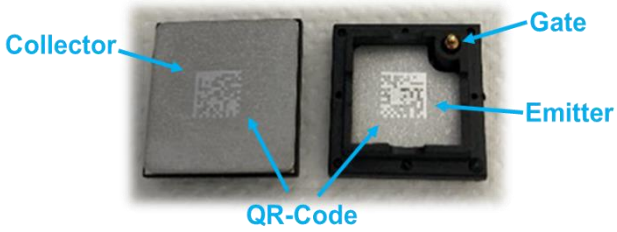


Fig. 3. Chip stack design including a QR code on both sides.

Besides this benefit, the mechanical robustness of the chip stack, comparing with a pure silicon chip, is also improved dramatically. By this, handling in production is gets much easier and many negative influences, e.g., particles, are reduced to zero. In addition, the production is highly automated to reduce variation in processing.

The LTS technology enables the reduction in the number of surface interfaces by 50% compared to free-floating, which decreases the thermal resistance of each chip. This allows a higher power density of the chips and increases the current capability of the PPI. In addition, the risk of surface problems is reduced because of fewer interfaces.

Alongside, the electrical robustness during switching is also increased by using the good connection to molybdenum as a sink for storing heat energy from the IGBT turning on or off.

III. IGBT chip capabilities

A. Surge current/static test

The first challenge for the 4.5 kV, trench IGBT chip having a total area of 246 mm^2 and an active area 144 mm^2, is to withstand a current several factors higher than the nominal current for at least 1 ms. The nominal and continuous current rating of the IGBT is 83 A at a maximum gate voltage of ±20 V. To meet the DC breaker requirements, the IGBT needs to be evaluated at high surge current and go beyond the existing forward bias safe operating area (FBSOA). Damage at surge current can be caused by extreme power dissipation, which is a function of current and the conduction time.

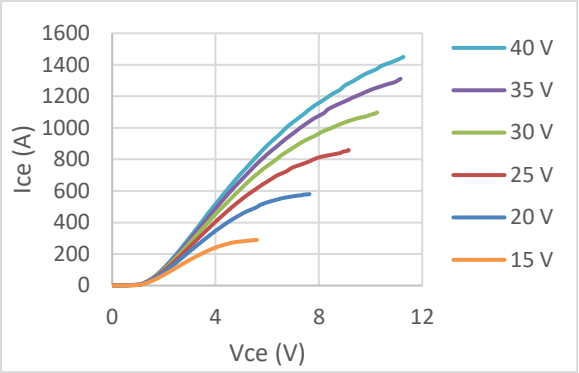


Fig. 4. Ice-Vce with different gate voltages till 40 V Vge

Fig. 4 gives an initial idea on what the chip is capable of at different gate voltages at 25°C without going into desaturation mode. To produce this result, ten samples were taken and tested at increasing gate voltages. Tests were also done at a maximum of 100°C to check the shift of the IGBT output characteristics. However, for the breaker application, 25°C is the standard operating temperature.

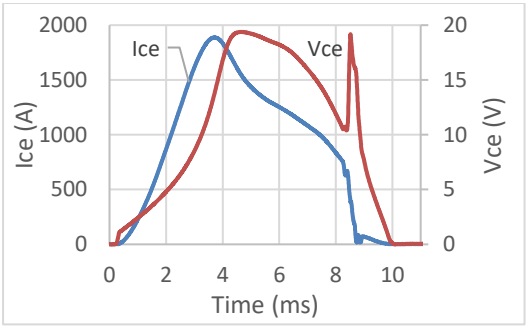
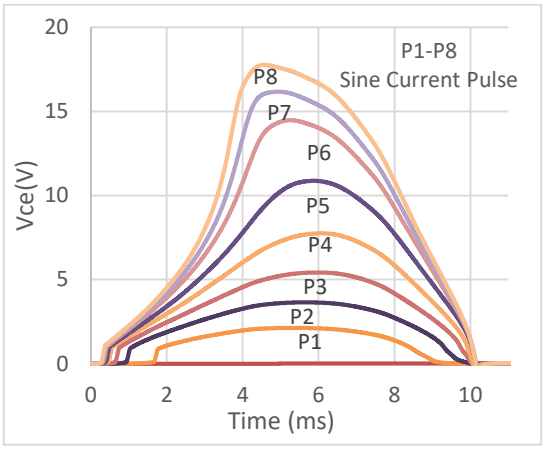


Fig. 5. Current and voltage curve for an IGBT damaged through surge current at 50 V Vge and Tvj = 25°C

The critical electric field for the Gate oxide of this IGBT is measured to be three times the nominal gate voltage, and there has been sufficient test data to statistically get an idea of the critical electric field at the corresponding gate voltage. However, these standard tests were done with a constant voltage in the gate for less than a millisecond and with an open collector emitter terminal. It was, therefore, important to investigate the high V_{ge} behavior when large collector current is flowing for a long period of time, the maximum being 10 ms for this work. For the first evaluation, the gate voltage was set close to the critical value and the first set of trials were done at 50 V with five devices, three of which got damaged, producing a data trend not supporting high currents over 1500 A. Fig. 5 is a current and voltage curve indicating when and where the IGBT got damaged at 50

V and at 25°C. Therefore, after careful consideration, the gate voltages were limited to 40 V, adding some buffer in case of overvoltage transients and to reach a gate voltage value where all samples would experience an electric field well below the absolute limit. For all FBSOA tests, a half sinusoidal wave was applied for 10 ms and the corresponding current and voltage of the chips were measured. It is important to note that for this work, IGBTs with V_{cesat} 2.7 V were measured at 83 A, 15 V Vge, and 150°C.



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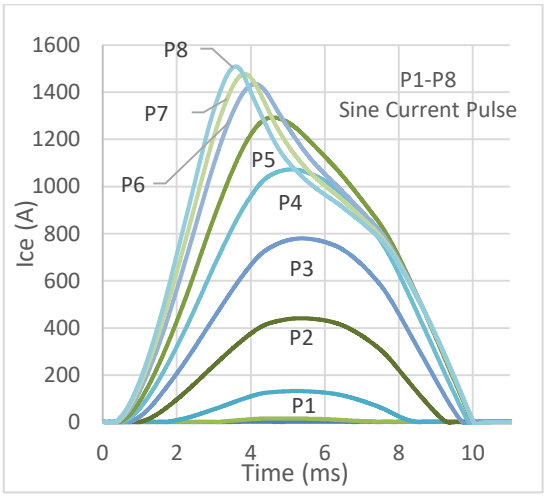
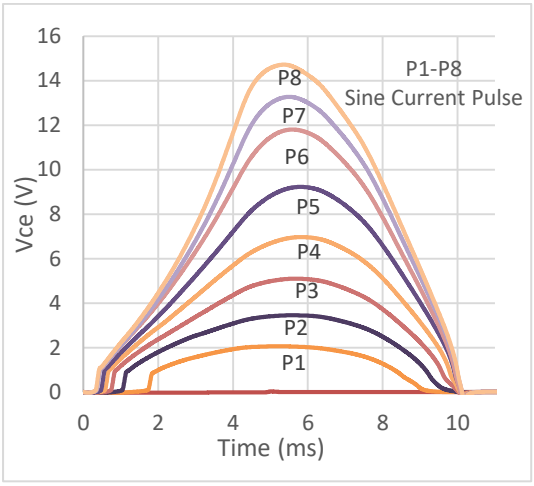


(b)

Fig. 6. Surge current pulse at 25°C, 10 ms and 40 V Vge; (a) Voltage (b) Current

Fig. 6 and 7 show measured surge currents and voltages at 25°C and 100°C respectively at V_{ge}= 40 V and 10 ms after a series of sinusoidal current pulses were applied to the IGBT. As can be seen in both the figures, as the IGBT approaches desaturation, the shape of the current sinusoid starts getting distorted, thereby adding to the power loss. Fig. 8 clearly shows the power dissipation distribution for the maximum current waveform for both temperatures. Because of the higher current capability at 25°C, the total energy reached as high as 94 kJ for a 10 ms pulse duration.



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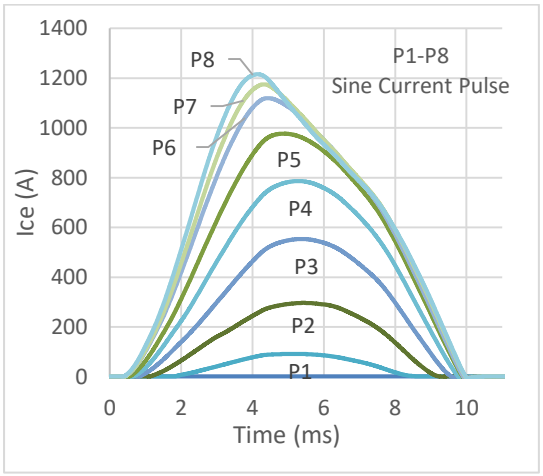


(b)

Fig. 7. Surge current pulse at 100°C, 10 ms, and 40 V Vge; (a) Voltage (b) Current

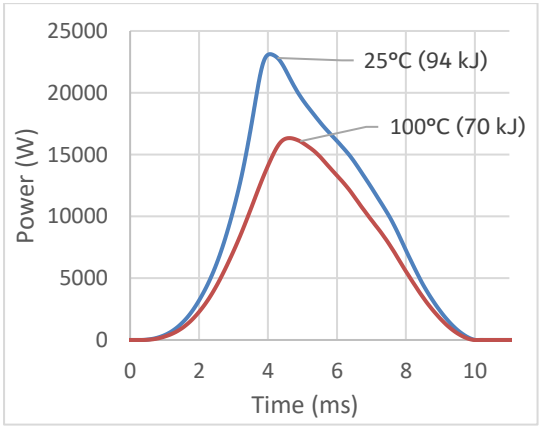


Fig. 8. Power at maximum current and 10 ms; total energy at 25°C = 94 kJ, and total energy at 100°C = 70 kJ

With the knowledge that a single chip can easily survive as high as 94 kJ, more samples were needed to statistically validate the trend. Fig. 9 is the measured data for 30 samples in the same settings with two temperatures. All devices safely reached more than 1300 A.

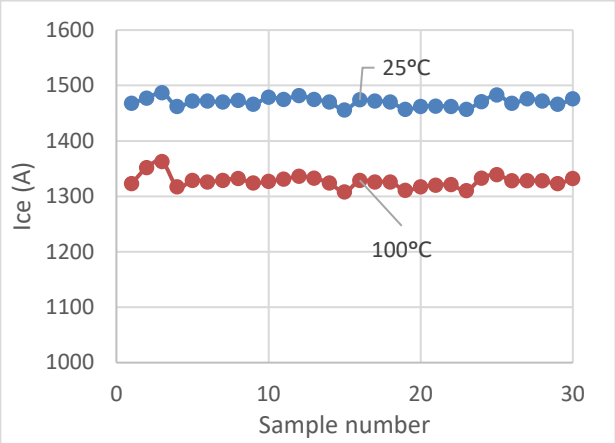


Fig. 9. IGBT surge current sample test with V_{ge} = 40 V

Thus, FBSOA can be claimed to be extended by at least 15 times the continuous rated current at higher gate voltages of up to 40 V.

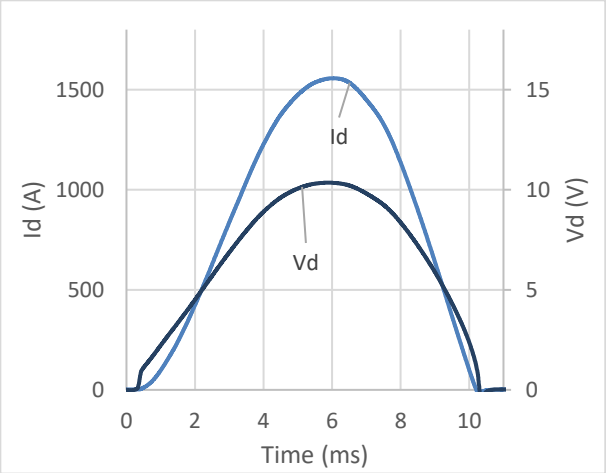


Fig. 10. FW diode surge current pulse for 10 ms at 100°C

Although the focus and scope of this work is limited to IGBTs, every IGBT needs a partner free-wheeling diode. To make the picture complete, the surge current capability of a 4.5 kV emitter-controlled diode is also shown in Fig.10. It shows that for a single chip reaching 1500 A is still under its destruction limit.

B. Long term stability

Like the extended FBSOA, it is also extremely important to test the long-term gate oxide stability for the IGBT at two temperatures. In this work, long term is defined by the number of cycles the chip will be experiencing in its entire lifetime. Generally speaking, for a circuit breaker application the IGBT needs to turn off currents a maximum of 100 to 500 times in its entire lifetime. However, since absolute limits of the device are being investigated, two modes of cycle tests were performed here.

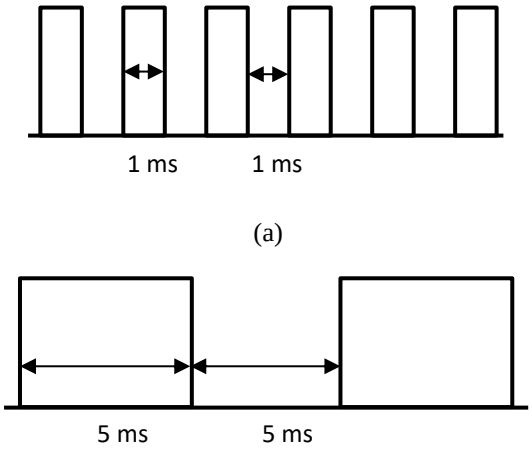


Fig. 11. Gate oxide stability test with 40/-8 V Vge (a) 10000 cycles (b) 25000 cycles

Fig. 11 illustrates the two modes of continuous pulse fed to the IGBT gate oxide. The 1 ms/1 ms pulse was for 25000 cycles and the 5 ms/5 ms was for 10000 cycles. Every time the Vge was changed between 40 V and – 8 V.

	25°C		100°C	
Parameters	**Before**	**After**	**Before**	**After**
V_{br} (V)	5148	5148	5148	5148
I_{ces} (mA)	0.0221	0.021	5.2	4.82
V_{geth} (mV)	6564	6567	5575	5588
V_{cesat}(mV)	2205	2179	2476	2450
t_{doff}(µs) (30 pcs)	10.30	10.16	10.36	10.34
t_{don}(ns) (30 pcs)	449	446	446	446
di/dt (A/µs) (30 pcs)	2843	2805	2765	2682

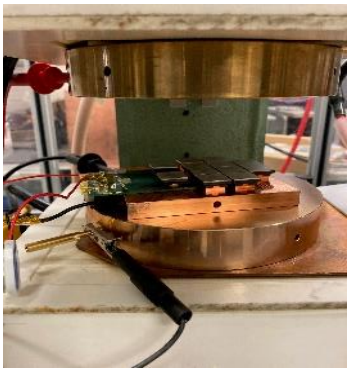
Table 1. Summary of the results before and after the cycle test

Once again, 30 samples were taken for the tests and every time before and after the cycle tests, both static and dynamic parameters were compared. The threshold voltage in the static parameters, has the most impact in case there is any change in the gate oxide. For the dynamic parameter, there can be a change in Miller plateau which is manifested by t_{doff}, t_{don}, and di/dt. However, as can be seen from Table 1, even with two temperatures, after the cycle test, there has been no significant changes in the parameters, thereby concluding that the single chip is able to withstand 40 V/-8 V without

a problem for at least 25000 cycles, both at warm and room temperatures.

C. **Dynamic tests**

This section addresses the most important criteria for establishing the usability and advantages of this IGBT chip for the circuit breaker application. In this part, the IGBT was switched off multiple times. The objective was to determine the maximum turn-off current with absolute safety, which stretches the RBSOA.



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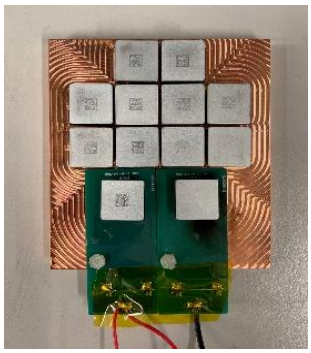
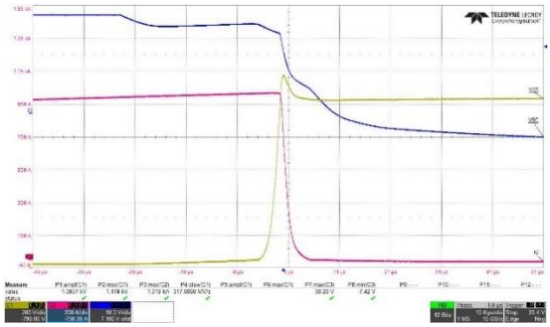


(b)

Fig. 12. Dynamic test setup (a) Press system (b) Chip stack system

For the dynamic tests, the chip stacks were pressed in a press system with copper pole pieces built specially for this project. The test circuit used here, was the classic double-pulse test setup with FWD connected anti-parallel to the load inductor.

The tests were conducted at two voltage levels, as can be there in the application as well – 1000 V and 2800 V. As 40 V is the maximum allowable gate voltage coming from the previous tests, additional safety margins were given to turn off with absolute robustness and hence all the tests were done at 30 V and switched off with -8V and a higher R_{goff}. The first trials were done to check with all 30 samples if 1000 A can be turned off at 1000 Vdc and 2800 Vdc at 25°C and 100°C. The following diagrams are the dynamic response of a single chip.



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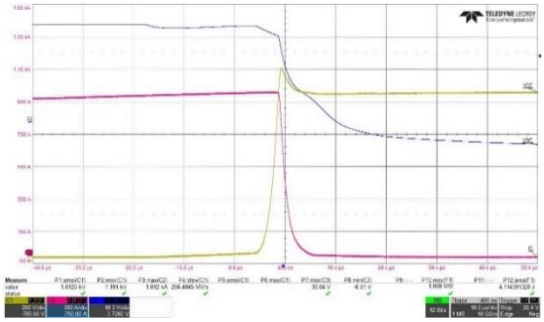

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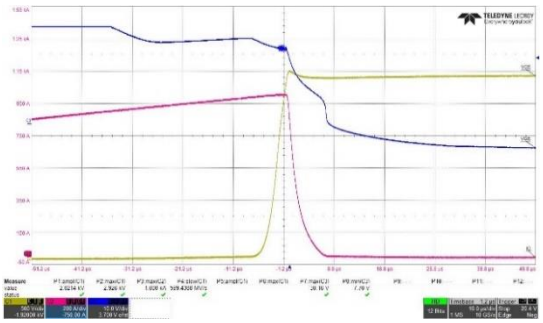
Fig. 13. Turn off 1000 A, 1000 Vdc (a) 25°C (b) 100°C



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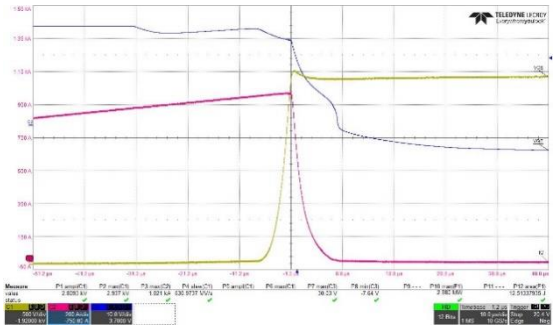

(b)

Fig. 14. Turn off 1000 A, 2800 Vdc (a) 25°C (b) 100°C

As the diagrams depict, turning off at 1000 A for voltages up to 2800 V does not show any robustness issues. In the pursuit of a higher current, keeping 30 V, V_{ge} as constant, it was found that some devices were damaged at about

1250 A (Fig. 15). Therefore, if the safety margin 30 V is fixed and if absolute robustness is required, 1000 A is the maximum current a single chip can be turned off at temperatures up to 100°C.

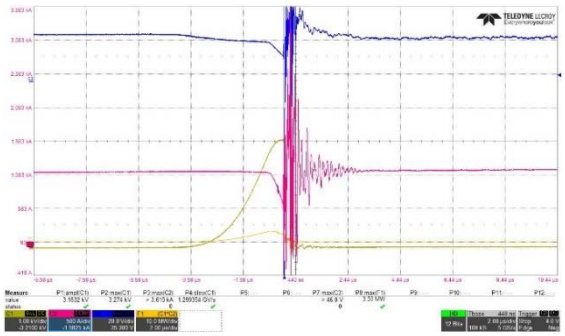

Fig. 15. Damaged IGBT at Turn off 1200 A, 2800 Vdc at 25°C

With this observation and supporting test results, the work concludes that a single 4.5 kV trench IGBT is able to turn off current in the range of 1000 A safely and can be realized for an application like hybrid DC breakers.

IV. Conclusion

The work started with the objective to explore the limits of the press pack 4.5 kV trench IGBT chip outside the standard ±15 V gate voltage range and investigate the surge current turn off capability, which was later exploited to find an application in the DC hybrid circuit breaker. The requirement for the breaker is that the chip needs to conduct a very high current for a maximum period of 1 ms and turn off slowly.

Since the work focused more on the chip level and not on the application, the first part started with exploring and eventually stretching the FBSOA. As can be seen from Fig. 16, the FBSOA was extended to 12 times the nominal current and up to 10 ms, instead of 1 ms, with 94 kJ being the typical energy loss at the conduction phase.

The next part addressed the turn-off of the chip at high currents, thereby stretching the limits of the existing RBSOA. As shown in Fig. 17, it was successfully tested that the chip can safely turn off 12 times the rated current at DC voltages up to 2800 V at 30 V gate voltage.

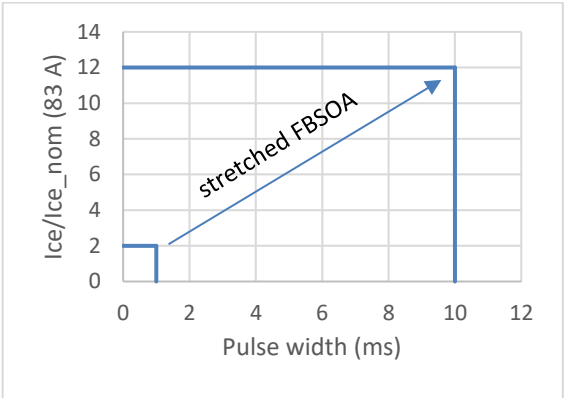

Fig. 16. Revised FBSOA for surge current operations such as hybrid circuit breakers

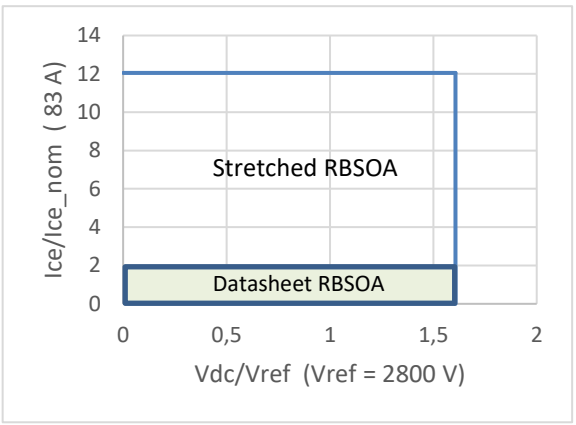

Fig. 17. Revised RBSOA for surge current operations

This work also investigated the long-term stability of the gate oxide by applying cycle tests till 25000 cycles and the oxide was able to retain its property before and after the tests.

The critical gate oxide having started with 50 V, the test parameter, i.e., the final gate voltage was brought down to 30 V in a stepwise manner, to provide a safety margin and better response to transient robustness. The press pack packaging also helps in better power cycling and increased mechanical stability. As of now, the objective has been met and the robustness boundaries have been explored. However, in future, investigations can be done at 40 V gate voltages. It should also be noted that turning off IGBT chips in parallel will add more current breaking capability, something that needs to be tested as an extended version of this work.

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