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Structure-Aware Compact Thermal Models of Power LEDs

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Abstract

This paper based on the example of white power LEDs illustrates the methodology for the generation of device compact thermal models, whose element values can be assigned physical meaning. The diode thermal behaviour was studied both with the forced water cooling and with the natural convection air cooling. Moreover, owing to the fact that the investigated devices had an electrically isolated thermal pad, the measurements were carried out with the thermal pad properly soldered and with the pad left unconnected, what facilitated the identification of particular sections in the heat flow path. All the measurements of device heating or cooling curves were taken according to the JEDEC standards. The determination of the optical power allowed the computation of the real heating power, which was used then as the input quantity for thermal computations and analyses presented in this paper. Based on the measurement results, thermal structure functions and time constant spectra were computed using the Network Identification by Deconvolution method. The compact thermal models of the investigated LEDs were derived based on the time constant spectra. Owing to the proposed methodology, it was possible to attribute physical meaning to model element values. The accuracy of generated compact models was validated by comparing the simulated heating curves with the measured ones. Although the compact models for the investigated cases consisted only of four RC stages, they provided excellent simulation accuracy with errors below 4% of the maximum temperature rise value.

Keywords: power LEDs, electrical, real heating power, Network Identification by Deconvolution, compact thermal models.

INTRODUCTION

Light Emitting Diodes (LEDs) become more and more important in our everyday lives. Compared to traditional light bulbs, LEDs are much more energy efficient, they last longer and, above all, they cost less [1]. However, their efficiency is still limited, so they produce not only the desired optical energy, but they dissipate significant amount of heat as well [2]. Therefore, Compact Thermal Models (CTMs) of LEDs and their cooling environment are always an indispensable part of larger multidomain system models [3].

Discrete thermal models are usually generated using the well-known electro-thermal analogy and typically they consist of a limited number of n thermal resistors R_{thi} and capacitors C_{thi}, whose product is called the thermal time constant τ_i. Different topologies of such thermal models were already proposed in the series of JEDEC JESD51 standards, including the canonical Foster RC networks. Then, device thermal responses in time $T(t)$ caused by the dissipated thermal heating power P_{th} can be found in such networks according to the following formula:

$$T(t) = P_{th} * \sum_{i=1}^{n} R_{thi} * \left[1 - e^{-\frac{t}{\tau_i}}\right] \qquad (1)$$

Foster RC networks can be derived using the Network Identification by Deconvolution (NID) analysis method, which is currently the base for the thermal measurement and modelling standards adopted for different electronic devices, not LEDs alone [4]. For real electronic systems the number of RC stages used in a model is theoretically infinite, but as it will be shown later on such models can be reduced to a compact form, preserving at the same time acceptable simulation accuracy.

According to the NID method, dynamic measurements of temperature responses have to be taken at instants equally spaced on the logarithmic time scale. Only then, all thermal time constants present in a response could be properly identified. Introducing a new time variable $z = \ln(t)$ and performing then numerical deconvolution, the continuous thermal time constant spectrum R_τ could be computed [5].

The concept of thermal resistance spectra extends the Foster RC ladder model, which can be related to each other as shown in Fig. 1. Namely, the Foster model can be obtained directly from the thermal resistance spectral density by dividing it into narrow segments having the width Δz. Then, each segment corresponds to a parallel RC connection, Thus, the RC equivalent Foster model results directly from the discretization of continuous time constant spectra.

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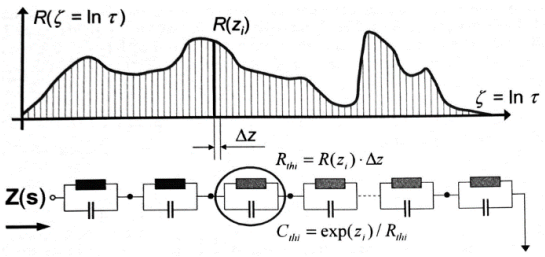

Fig. 1: The thermal time constant spectrum corresponding to the Foster RC network [4].

The thermal resistance spectra render possible also the construction of functions describing the entire heat flow path from the device junction to the ambient, which are known as cumulative thermal structure functions, shown in Fig. 2, relating the cumulative capacitance $C_{th\Sigma}$ and the cumulative resistance $R_{th\Sigma}$. These functions solve the main problem related to the Foster networks consisting in the fact that the node-to-node capacitances imply that thermal responses propagate instantaneously through the entire system and consequently thermal resistances and capacitances cannot be related to any physical part of a system.

Fortunately, the Foster RC networks can be transformed into mathematically equivalent Cauer networks, whose elements could be already assigned physical meaning. Such networks are formed by series thermal resistances and parallel capacitances, all connected to the thermal ground, however, the Cauer RC networks result from the discretization of the cumulative structure function performed in a similar way as described previously.

The main goal of this paper is to investigate the thermal properties of LEDs and to develop adequate methods for their thermal modelling. Based on measurement results, cumulative thermal structure functions of the diodes are calculated and their compact thermal models are derived from the time constant spectra using the NID method. The following section describes the experimental set-ups and presents obtained measurement results. Then, the results are analysed and the methodology to generate LED compact thermal models is introduced. Finally, the transient temperature simulation results obtained with these models are compared with the measurements.

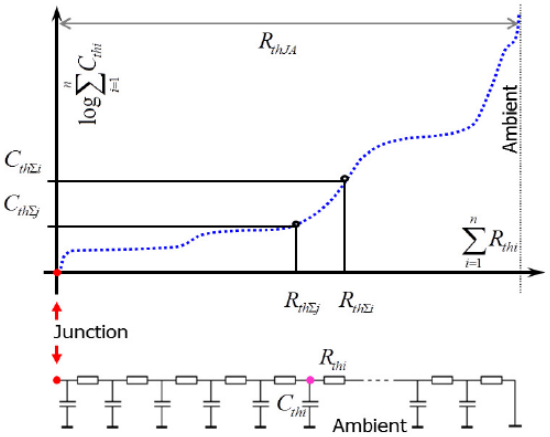

Fig. 2: The cumulative structure function corresponding to the Cauer RC network [6].

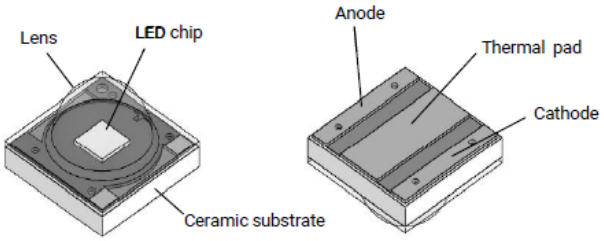

Fig. 3: Package of the investigated LED [7].

MEASUREMENT RESULTS

This section presents in detail the obtained measurement results. First, the investigated devices and their cooling conditions as well as the equipment used in experiments are described. Then, the diode temperature sensitivities are determined. Next, the device junction temperature transient measurement results for different mounting manners and cooling conditions are discussed. Finally, the optical measurements results are briefly covered.

Experimental Set-Ups

The particular device investigated here is the 3 A white power LED from the Cree XP-L family, whose package, shown in Fig. 3, has a thermal pad which is electrically isolated both from the cathode and the anode. This pad enhances the heat removal from the LED package to the board. For the experiments, the investigated diodes were mounted on metal core PCBs, whose dimensions were 2.50 cm x 2.50 cm x 0.16 cm. In order to investigate the influence of the thermal pad, two configurations were considered, once the thermal pad was properly soldered to the board and once it was left unconnected.

Additionally, two different types of cooling conditions, shown in Fig. 4, were applied. During the measurements with the free convection cooling the MCPCB with the Device Under Test (DUT) was suspended horizontally in thermally insulating clamps (see Fig. 4a), whereas with the forced water cooling the board was firmly pressed, again with the clamps, against a copper cold plate, as pictured in Fig. 4b. The thermal resistance between the board and the cold plate was reduced owing to the application of thermal grease. The cold plate temperature was maintained automatically at a desired value by a thermostat. During experiments both water and cold plate temperature values were measured.

a) free convection air cooling b) forced water cooling

Fig. 4: Cooling conditions applied during measurements.

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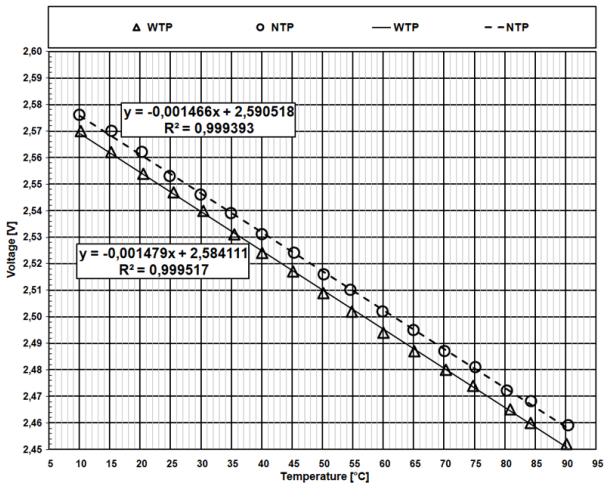

Fig. 5: Measured LED temperature sensitivity.

The measurements of diode heating or cooling curves were taken with the transient thermal tester T3Ster®, currently produced by Siemens. This equipment renders possible real time thermal impedance measurements compliant with the JEDEC standards by recording the device transient temperature responses to unitary power step excitations with the microsecond time resolution. The analysis of obtained experimetal results facilitates the evaluation software provided together with the tester and implementing the earlier described NID method.

Electrical Measurements

Before actual measurements the temperature sensitivity of the investigated LEDs had to be determined. For this purpose, the LEDs soldered to PCBs were placed on the cold plate. Then, the measurement current of 10 mA was forced through the devices and the diode voltage was recorded. The results of this calibration procedure are presented in Fig 5. As can be seen, both diodes show nearly perfectly linear characteristics of their junction voltage drop in function of temperature. The measured temperature sensitivity of the diode with the thermal pad connected (WTP) was equal to -1.479 mV/K whereas the sensitivity of the diode with the pad not connected (NTP) was -1.466 mV/K.

After the calibration, as mentioned previously, the diode cooling curves were recorded applying different kinds of cooling conditions. The measurements with the free convection cooling, denoted in the figures as FA, were performed for the diode currents of 350 mA, 700 mA and 1000 mA. In order to reach the thermal steady state the LEDs had to be heated for 1800 s and then cooled over the same period of time.

During the measurements with the forced water cooling, denoted further on as CP, the cold plate temperature was set to 20 ºC and the measurements were taken for the LED currents of 0.7 A, 1.0 A, 1.5 A and 2.0 A. Such high current values could not be attained with the free air convection cooling because of the excessive junction temperature. This time the diodes were heated only for 300 s until the thermal steady state was reached and then the cooling curve was recorded.

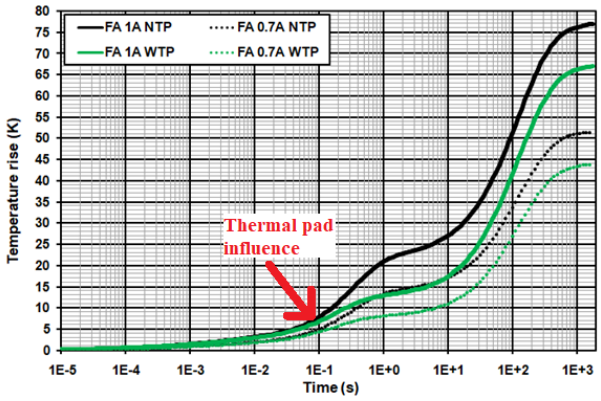

Fig. 6: Thermal pad influence in the case of the natural convection cooling.

The measurement results are shown in Figs.6-9. In order to facilitate the analyses, the figures represent the diode heating curves, which were obtained by subtracting the recorded cooling curves from the respective steady state temperature values. Analysing now the influence of the thermal pad, it can be seen that its presence affects the heating curves already after several tens of milliseconds. Independently of the applied cooling conditions, the pad noticeably enhances the dissipated heat removal. With the free convection cooling the device temperature rise is reduced owing to the use of the pad by one third and for the forced water cooling this reduction is even more significant.

Examining the influence of cooling conditions on the device heating curves, it can be observed that for the same current value the curves are initially identical and then they diverge drastically after a couple of seconds. When the thermal pad is not connected the junction temperature rise value is some two-third lower in the case of forced water cooling. This reduction is more important for the LEDs with the pad soldered, reaching even 80%.

Hence, it is evident that attaching the devices to a cold plate assures much better heat removal than in the case of free convection cooling. Furthermore, with the forced water cooling the thermal steady state is reached much faster, only after a few seconds, compared to the couple of minutes required in the case of natural convection cooling.

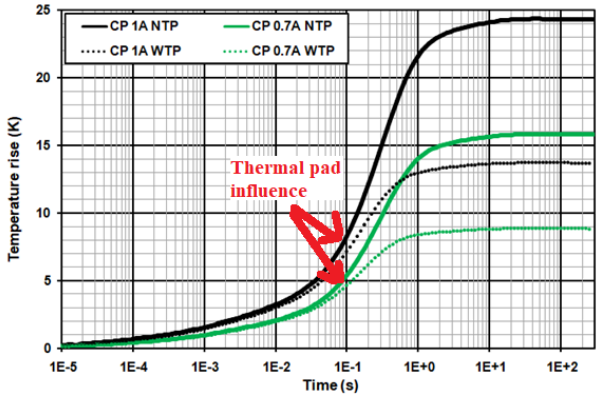

Fig. 7: Thermal pad influence in the case of the forced water cooling.

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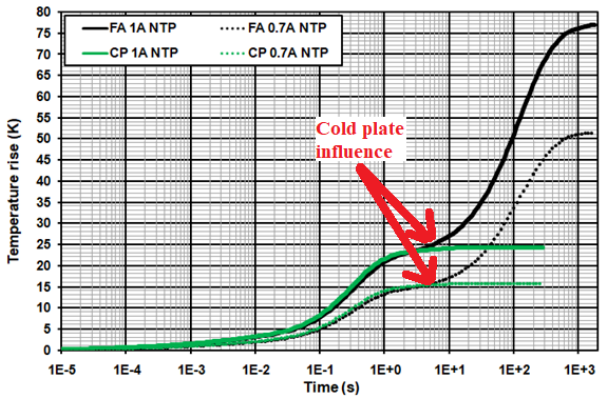

Fig. 8: Cooling condition influence for LED with the thermal pad not connected.

Optical Measurements

For most electronic systems the NID thermal analysis method could be applied directly using the electrical power value P_{el} as the input variable, since it is almost entirely dissipated in the form of heat. However, when a system contains devices in which the electrical energy is converted into some other form, e.g. the optical one P_{opt}, as it is in the case of LEDs, only the real heating power P_{th} has to be used for thermal analyses. This fact was stated in the JEDEC standard concerning LEDs [8]. The main function of LEDs is the generation of light. This occurs when the electric current flows through the junction of a diode. Unfortunately, these devices do not convert all delivered energy into light and a significant part of the input electrical power is dissipated as heat. Typically around a half of the energy is converted into heat, but the exact values depend on many factors, such the device current or operating temperature.
Here, the data concerning the optical power values were acquired from the earlier results published in [9]. There, the optical power was measured using the set-up shown in Fig. 10, where the diode was placed on a cold plate inside a light tight box. Then, the light intensity was measured directly over the diode and the total optical power was calculated based on the knowledge of the spatial distribution of the emitted light provided in the LED datasheet by device manufacturer.

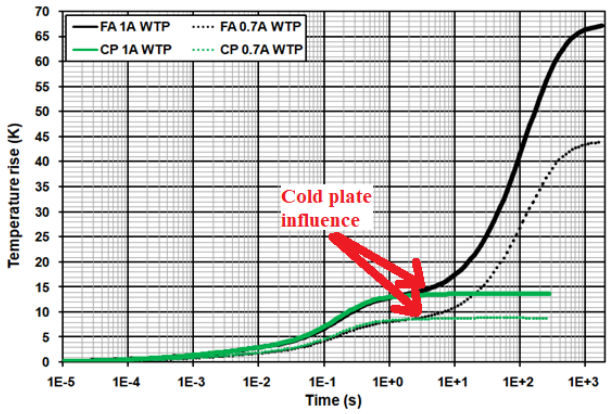

Fig. 9: Cooling condition influence for LED with the thermal pad soldered.

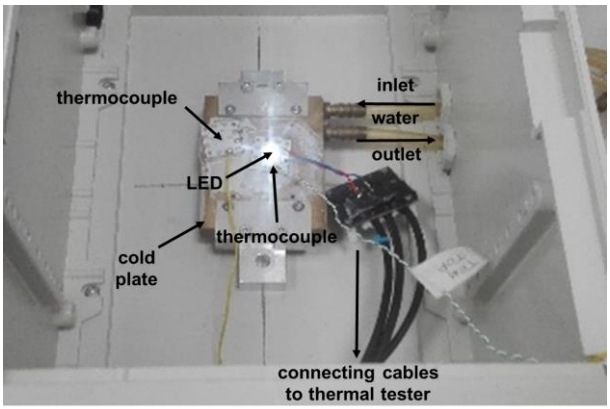

Fig. 10: Experimental set-up used for the measurements of optical power [9].

The results of these optical measurements, adapted from [9], are presented in Table 1. As can be seen, for the investigated diodes their optical efficiency η_{opt}, being the ration of the optical power to the electrical power, drops down when the device current increases. Then, correspondingly more supplied energy is transformed into heat. At the same time, the influence of temperature on the LED efficiency turned out not to be so important.

	I[A]	P_{el}[W]	P_{opt} [W]	η_{opt} [%]
Forced convection cooling 20°C with thermal pad	0.70	2.08	1.49	71.46
	1.00	3.06	2.07	67.46
	1.50	4.79	2.97	61.99
	2.00	6.60	3.78	57.24
Forced convection cooling 20°C with no thermal pad	0.70	2.06	1.44	69.88
	1.00	3.01	1.98	65.81
	1.50	4.64	2.79	60.08
	2.00	6.34	3.48	54.85
Natural convection cooling with thermal pad	0.35	0.98	0.68	69.53
	0.70	2.02	1.30	64.10
	1.00	2.95	1.74	58.98
Natural convection cooling with no thermal pad	0.35	0.98	0.71	72.69
	0.70	2.00	1.34	66.97
	1.00	2.90	1.79	61.65

Table 1: The optical measurement results.

THERMAL ANALYSES

This section provides detailed analyses of measurement results, which are obtained employing the NID analysis method. According to the discussion from the previous section, all the presented results are produced using the real heating power as the input quantity.

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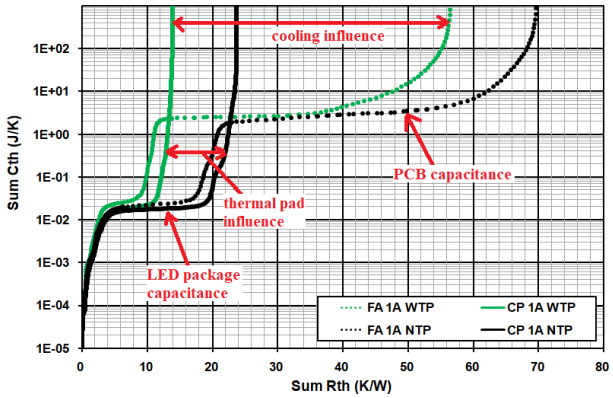

Fig. 11: Comparison of cumulative thermal structure functions for 1 A LED current.

First, the thermal structure functions are analysed and compared for different experimental set-ups. Then, the thermal time constant spectra for the considered cases are discussed. Next, the methodology used to generate CTMs is introduced together with the explanation of the physical meaning of particular model element values. Finally, the generated CTMs models are validated with measurement results.

Thermal Structure Functions

The cumulative thermal structure functions allow the identification of both thermal pad and cooling condition influence on thermal resistances. The analyses presented here begin with the examination of structure functions presented in Fig. 11. From the figure, it is clearly visible that the thermal pad reduces significantly the thermal resistance, what coincides with the earlier observations considering heating curves. The flat section around the thermal capacitance of 20 mJ/K can be attributed to the package capacitance and the one at around 2 J/K to the one of MCPCB.

The use of the cold plate visibly reduces the thermal resistance, around three times when the pad is soldered and almost four times when the pad is not connected. The thermal pad decreases the total thermal resistance by almost 10 K/W, but only in the section, where heat diffuses from the package to the board. On the other hand, the change of the cooling mechanism affects the entire structure function.

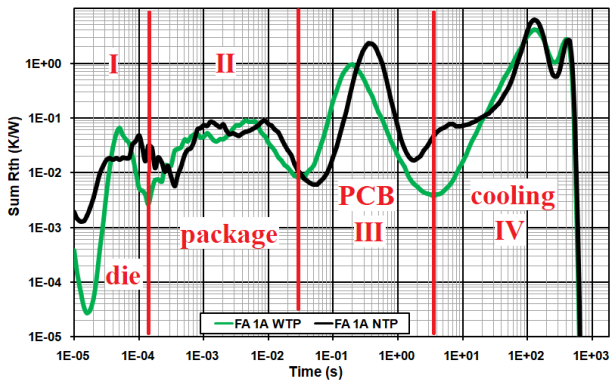

Fig. 12: Comparison of time constant spectra for the free convection cooling.

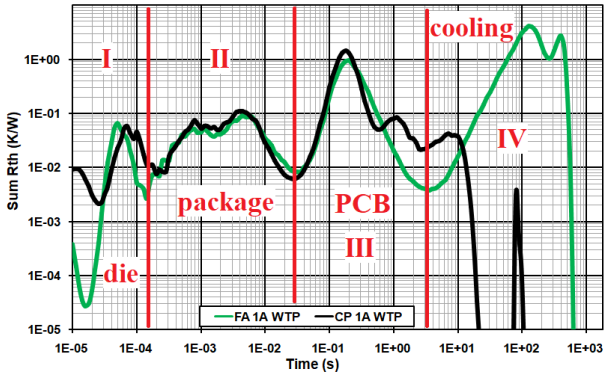

Fig. 13: Comparison of time constant spectra for the LED with the thermal pad soldered.

The natural convection cooling influences the thermal resistance already inside the package since heat spreads more laterally through its entire volume. Moreover, the structure function has an additional, long, flat section corresponding to the heat exchange with the air. The length of this part depends mainly on the value of the heat transfer coefficient. On the contrary, owing to the use of the cold plate, the thermal resistance is much lower and the structure function ends earlier. Then, the thermal capacitance of the MCPCB is no longer visible in the structure function because the heat spreads into the cold plat only through a very small part of substrate volume.

Time Constant Spectra

The time constant spectra demonstrating the influence of the thermal pad and applied cooling conditions are presented in Figs. 12-13 respectively. According to the NID method theory, the minima in the spectra indicate time instants when heat diffuses into another material. These spectra have three clear minima marked in the figures with thick vertical lines.

The first minimum between Sections I and II reflects the die attach thermal resistance. Furthermore, leaving the thermal pad unconnected shifts the peak in Section III to the right from 0.2 s to almost the double of this value and the spectral density of the resistance becomes much higher, what suggests that the shift is mainly due to the increase of the resistance. Finally, the change of cooling conditions affects only Section IV of the spectra.

Thus, Sections I and II reflect the heat flow inside the LED package from the semiconductor die to the solder point, whereas Sections III and IV the heat conduction into the PCB and the cooling. In this way the thermal time constant spectra can be divided into four sections corresponding to the physical parts of the structure.

Compact Thermal Models

Following the above presented discussion concerning the time constant spectra, the CTMs for the investigated circuits can be derived by dividing the spectra in the location of their minima. The main advantage of this solution is that it might preserve the physical meaning of model element values [8].

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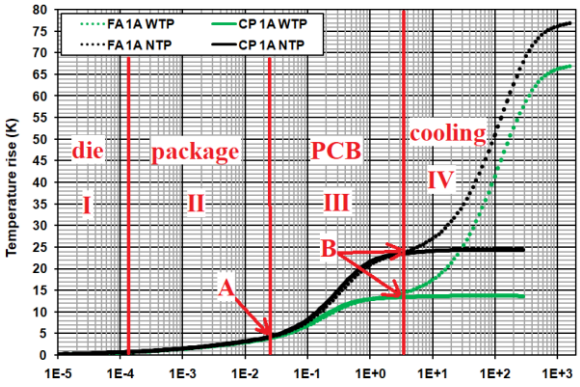

Fig. 14: Diode heating curves divided according to different heat flow path sections.

The four heat flow path sections identified in the spectra correspond to the respective locations in the heating curves indicated in Fig. 14. These curves diverge for the first time at Point A owing to the use of the thermal pad and then at Point B due to the change of cooling, what proves the correctness of the proposed approach.

For each of these sections, their thermal resistances can be computed by adding the components of the spectrum. The next step is to determine the thermal time constant values for each section. The best strategy is to assign initially for each time constant the value coinciding with the maxima in the spectra, what yields relatively small simulation errors, which could be further minimized. Then, the capacitance values could be computed simply by dividing the respective thermal time constant and resistance values. In this way a CTM in the form of RC Foster network is obtained.

Although it is easier to compute temperature responses using the Foster network, the physical meaning can have only the Cauer RC network element values. Therefore, the last step is the conversion from the Foster to Cauer network, such as the one shown in Fig. 15. The conversion can be performed employing the algorithm presented in [4]. The resulting values of the Cauer RC network element values for the curves shown in Fig. 14 are provided in Table 2.

The analysis of the values given in the table confirms the earlier observations. For the free convection cooling, the last component corresponding to the thermal time constant of some 140 s is the dominant one. Its thermal capacitance of 3 J/K is the capacitance of the MCPCB and its resistance of almost 50 K/W reflects the heat exchange with ambient. Knowing the surface area of the board, i.e. just over 13 cm^2, the value of the heat transfer coefficient h can be estimated around 17 ,W/(m^2 K), what corresponds well to values predicted theoretically for the natural convection.

With the forced convection cooling the last component is very small and then the third component becomes dominant. This RC stage describes the package to board interface, so the impact of the thermal pad is reflected in its element values. As already mentioned, the time constant of this stage increases noticeably when the pad is not connected. This is due to the change of thermal resistance, which for the natural convection cooling increases from 8.4 K/W to 17.2 K/W.

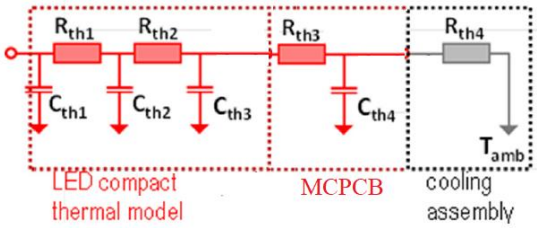

Fig. 15: The Cauer RC model for investigated structures [10].

The first and the second stage of the models correspond to the junction to solder point thermal resistance of the diode and its typical value provided in the datasheets is 2.2 K/W, whereas the measured ones fall in the range 2.5÷3.0 K/W. Therefore, these results are very realistic, taking into account that the exact boundary conditions applied during measurement were not specified by the manufacturer. Moreover, the CTMs in Sections I and II can be less accurate because, depending on the cooling conditions, they are relatively lower than the thermal resistances of Sections III or IV. Consequently, their estimates might bear more error because of relatively higher measurement noise.

Finally, the accuracy of generated RC ladder CTMs was verified by comparing the simulated heating curves with the measured ones. The results of this comparison are shown in Fig. 16, where the black lines denote the simulated curves. The dashed and double lines are used for the natural convection cooling with and without the thermal pad respectively. As can be seen, for all of the cases the simulated values closely follow the measured ones. In particular, for the free convection cooling with the thermal pad the maximum error is equal to 2.4 K, without the thermal pad it equals 2.2 K and finally for the forced convection with the thermal to only 0.4 K. Thus, this relatively simple 4 stage RC model provided excellent simulation accuracy with errors remaining always well below 4% of the maximum temperature rise value.

	sec	τ [s]	R [K/W]	C [J/K]
Natural convection cooling 1A with no thermal pad	I	3.83×10^{-5}	6.51×10^{-1}	5.89×10^{-5}
	II	3.40×10^{-3}	2.34×10^{0}	1.45×10^{-3}
	III	3.33×10^{-1}	1.72×10^{1}	1.94×10^{-2}
	IV	8.33×10^{1}	4.96×10^{1}	1.68×10^{0}
Natural convection cooling 1A with thermal pad	I	1.91×10^{-5}	4.59×10^{-1}	4.15×10^{-5}
	II	2.51×10^{-3}	1.99×10^{0}	1.26×10^{-3}
	III	1.96×10^{-1}	8.40×10^{0}	2.33×10^{-2}
	IV	1.44×10^{2}	4.57×10^{1}	3.15×10^{0}
Forced convection cooling 1A with thermal pad	I	3.71×10^{-5}	6.35×10^{-1}	5.84×10^{-5}
	II	2.40×10^{-3}	2.22×10^{0}	1.08×10^{-3}
	III	1.90×10^{-1}	1.06×10^{1}	1.79×10^{-2}
	IV	1.06×10^{1}	4.13×10^{-1}	2.55×10^{1}

Table 2: Cauer RC CTM values for different set-ups.

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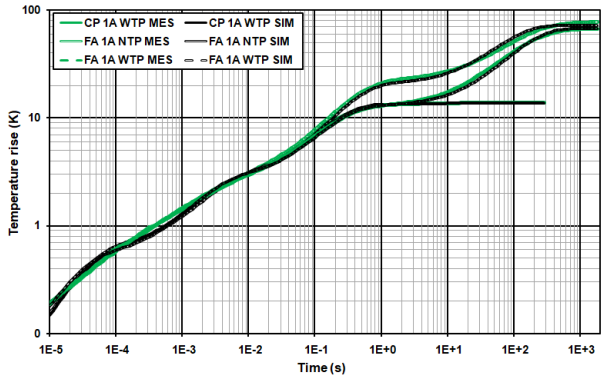

Fig. 16: Comparison of measured and simulated LED heating curves in different experimental set-ups.

CONCLUSIONS

This paper proposed a methodology to develop compact thermal models of power LEDs, which were generated in such a way that it was possible to relate particular model elements to selected regions of the structures, hence allowing physical interpretation of their values. As a result, the change of device mounting manner and cooling conditions affected only certain values of these CTMs.

Moreover, the paper demonstrated experimentally the influence of thermal pad and device cooling conditions on the value of junction to ambient thermal resistance. Specifically, it was shown that the use of thermal pad enhances significantly the heat conduction from the package to the board by lowering the thermal resistance. At the same time, the forced water cooling considerably improves the heat exchange between the board and the ambient.

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