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Degradation of 600V GaN HEMTs under Repetitive Short Circuit Conditions

J. Kozárik[1], J. Marek[1], M. Minárik[1], A. Chvála[1], T. Debnár[1], M. Donoval[1,2] and Ľ. Stuchlíková[1],
[1] Slovak University of Technology in Bratislava,
Ilkovičova 3, Bratislava, Slovakia
[2] NanoDesign, s.r.o, Drotárska 19a, 811 04 Bratislava, Slovakia

Abstract

This paper describes impact of repetitive short-circuit stress on commercially available 600V e-mode GaN HEMTs with p-GaN gate. The devices were subjected to up to 10^5 short circuit stress cycles at 100V and 300V drain voltage. Tests at voltages over 300V resulted in destruction of the devices. Electrical characteristics were measured prior to, and after each sequence of pulses to observe gradual effects of repetitive SC stress. The devices were also analysed by DLTS. A shift in all of the measured characteristics was observed. Amount of the shift does not correlate with the number of SC cycles, which suggests more parameters of the devices are affected. The shifts were also more pronounced at higher drain voltage. The trapping was also analysed using DLTS. Due to high complexity of the spectra, only the traps verified by simulation were investigated. At 100V stress voltage, the shift in DLTS spectra was small, at 200V it was significant. Full analysis of possible origin of the observed deep levels is still ongoing.

Keywords: GaN HEMT, repetitive short circuit, DLTS, degradation

INTRODUCTION

Gallium nitride high-electron mobility transistors (GaN HEMT) are one of the most promising technologies for future medium-power, high-efficiency semiconductor switches. However, to completely replace silicon power MOSFETs, they need to be able to withstand the harsh conditions that occur in real-world switching applications. One of the most commonly occurring extreme conditions is the type-I short circuit or hard-switching fault, a turn-on event of a switch that is experiencing a shorted complementary switch (Fig. 1a). In this condition the transistor is subjected to high drain-source voltage (V_{DS}) and current (I_D) simultaneously. Such stress can result in degradation or destruction of the transistor due to high amount of energy delivered to the device. Although GaN HEMTs exhibit good performance in standard operating conditions, their behaviour and reliability under extreme stress needs to be thoroughly analysed. Short-circuit (SC) behaviour of e-mode GaN HEMTs has been already adressed by researchers, mostly focused on destructive tests without analysis of impacts of repetitive non-destructive SC stress [1, 2]. Degradation after repetitive SC test was addressed e.g. by [3] who observed that repetitive SC stress results in channel and gate structure parameter changes, which lead to reduction of conductivity. Gate threshold voltage is also affected. The elevated temperature of the device during a SC event seems to be the trigger of the degradation. According to [4], in repetitive SC tests, local temperature fluctuates between room temperature and a high value, generating strong mechanical stress during the thermal expansion and contraction phases. Physical cracks are formed in the structure due to the high temperature spike and local temperature fluctuations in the GaN layer. However, there is not much research on how greater amounts (more than 10^4) non-destructive SC pulses at lower V_{DS} affect the transistor performance.

TEST EQUIPMENT

GaN HEMTs stand out among other power switching devices mainly due to exceptionally short switching time.

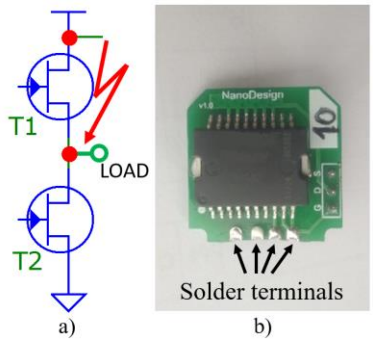

Fig. 1: a) Typical short circuit type I event. T2 turns on to shorted complementary transistor. b) Device under test soldered to a sample board.

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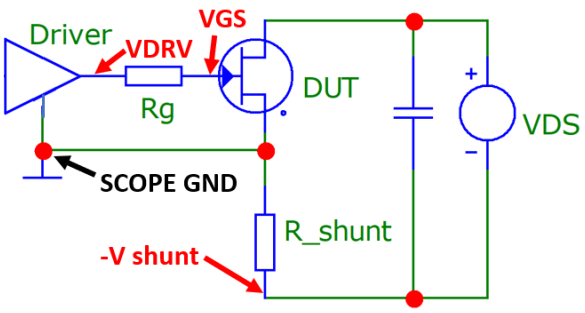

Fig. 2: Simplified schematic of the test setup.

To exploit this advantage effectively, circuit designers try to eliminate as much parasitic impedance as possible in gate-source loop and drain-source loop of the device [5]. To accurately simulate a real-world application, a custom tester device was designed and built. It consists of a main PCB fitted with high-voltage capacitor bank, gate driver, current-sense resistor and support circuits. A device under test (DUT) is soldered to another PCB, which is then soldered to the main board (Fig 1b). This soldered connection reduces the parasitic inductance and resistance to a greater extent than a connector, while the DUT can still be fitted and removed in a convenient manner. The PCB also features a Kelvin source contact to the gate driver. Figure 2 shows a simplified schematic of the tester. The main board is fitted with a gate driver IC optimized for driving GaN HEMTs. The gate voltage can be adjusted continuously from 4V to 12V between on-state and off-state levels. Negative off-state voltage is also supported. Input signal connector is optically isolated. Gate-source loop is only approx. 16mm^2 in area and can be fitted with a simple gate resistor or with a R-C network optimized for a rapid charge and discharge of a gate capacitance while preventing unnecessarily high steady-state current. This current is a consequence of the transistor gate diode structure. The drain-source capacitor bank is charged from an external DC power supply. It is rated up to 450V with a total capacitance 83µF and uses combination of ceramic and polypropylene capacitors capable of fast high-current discharge. This amount of capacitance is sufficient for GaN HEMTs with short-circuit saturation current up to 100A and 10µs pulse duration at higher V_{DS}. The decrease of capacitor voltage during the pulse is ~12V according to equation for constant current capacitor discharge:

$$v(t) = V_0 - \frac{i\,t}{C} \qquad (1)$$

The main board is fitted with a 10mΩ current-sense resistor in series between DUT source terminal and the capacitor bank negative terminal. In this configuration, current can be measured as a negative voltage drop across the resistor with an ordinary oscilloscope probe grounded at DUT source, a common ground terminal for all measured signals. In an event of a type-I short circuit in a well-designed real application circuit, turn-on drain current rise is steep, but turn-off V_{DS} overshot is relatively small due to reduced stray inductance.

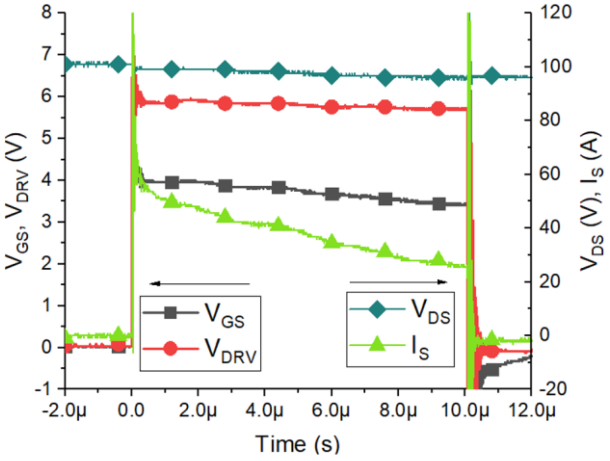

Fig. 3: Typical waveforms during short circuit. Gate voltage is limited by the transistor's gate diode to ~4V.

However, the overshot can still affect degradation of the DUT, particularly in repetitive tests. To eliminate this high-voltage stress affecting the test results, a typical high-speed gate-driving circuit has been substituted for a larger gate resistor that extends the turn-off time and reduces the voltage spike.

EXPERIMENTAL RESULTS

Sample transistors used for these experiments are commercially available enhancement-mode AlGaN/GaN HEMTs on Si substrate with p-GaN gate structure. Some of their key parameters are V_{DSmax} = 600V, on-resistance $R_{DS(on)max}$ = 70mΩ, max. pulsed current I_{Dmax} = 60A. At first, some samples were stressed at increasing voltages from 50V to 400V and pulse durations from 1µs to 10µs. Typical short circuit waveforms are shown in Fig. 3. Drain voltage over 300V often resulted in destruction of DUT (Fig. 4), in some cases even after the first SC pulse.

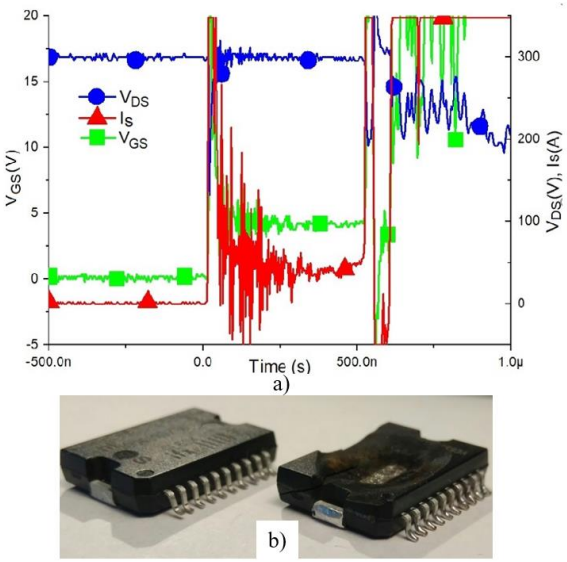

Fig. 4: a) Waveforms during device failure. b) Visible destruction of the transistor.

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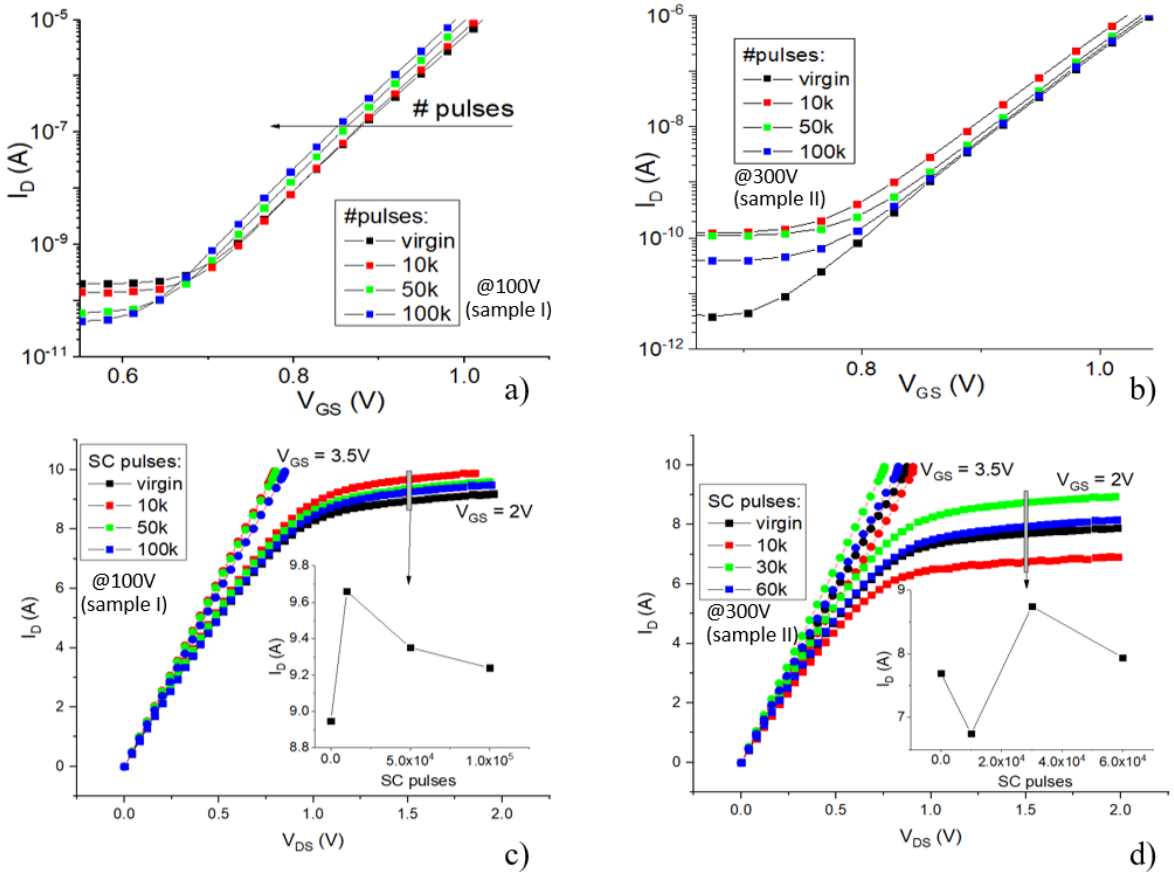

Fig. 5: Transfer and output characteristics measured after several sequences of SC pulses. a) Transfer at 100V. b) Transfer at 300V. c) Output at 100V. d) Output at 300V. Inset in c) and d) shows change of drain current at gate voltage VGS = 2V and VDS = 1.5V in relation to number of SC pulses While a) exhibits a decreasing trend in gate threshold voltage (V_{TH}), other data suggest that at least two device parameters are significantly affected by the test.

Therefore, the transistors were repetitively tested at V_{DS} up to 300V. Duration of the pulses was set to 2µs in all of the tests performed. The highest thermal stress occurs within this period [4]. To allow the structure to cool down between the repetitions, consecutive SC pulses were separated by 250ms period. The test was performed in several sequences of 10^3 to $5 \cdot 10^4$ pulses. Characteristics of the samples were measured on virgin samples and then after each sequence of pulses to observe gradual effects of repetitive SC stress. Although both were the same type devices, their initial characteristics varied observably, however this is common among current commercial GaN HEMTs. Repetitive SC stress had different effects depending on test voltage. Figure 5 a) and b) show a shift of transfer characteristics and gate threshold voltage (V_{TH}). Figure 5 c) and d) depict output characteristics with saturation current evidently affected. From measurements at different drain voltages it is clear that higher V_{DS} during stress is responsible for more significant shift of characteristics. However, uniform shift of characteristics was not observed. Based on previous studies, it is known that shift of characteristics is caused by trapping effects in AlGaN layer. Based on literature, three mechanisms apply during stress but not to the same extent. First charge trapping under gate electrode is responsible for threshold voltage shift [6]. Trapping in drain access region causes decrease of free charge in the 2DEG [7] and both trapping effects are decreasing mobility of carriers in the 2DEG [8] affecting on-resistance and saturation current. Drain leakage current ($I_{D(LEAK)}$) is strongly affected by the stress and in principal, is the main indicator of degradation and a critical parameter limiting the overall reliability of the element. At first, significant decrease of $I_{D(LEAK)}$ was observed, however after $4 \cdot 10^3$ stress pulses it increases again and after $4 \cdot 10^4$ pulses the leakage surpasses the virgin sample at V_{DS} from less than 100V (Fig. 6).

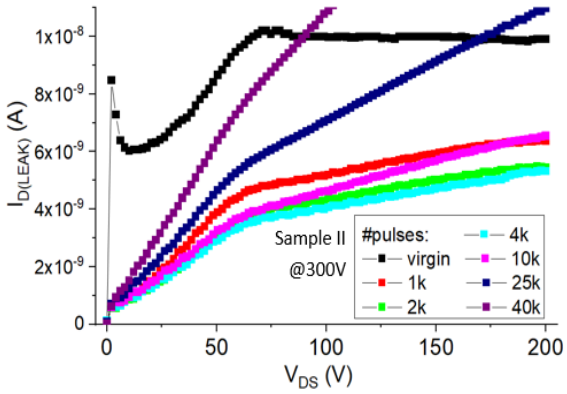

Fig. 6: Drain voltage dependence of drain leakage current $I_{D(LEAK)}$ at gate voltage V_{GS} = 0V. $I_{D(LEAK)}$ decreases up to 4000 pulses, then rapidly increases.

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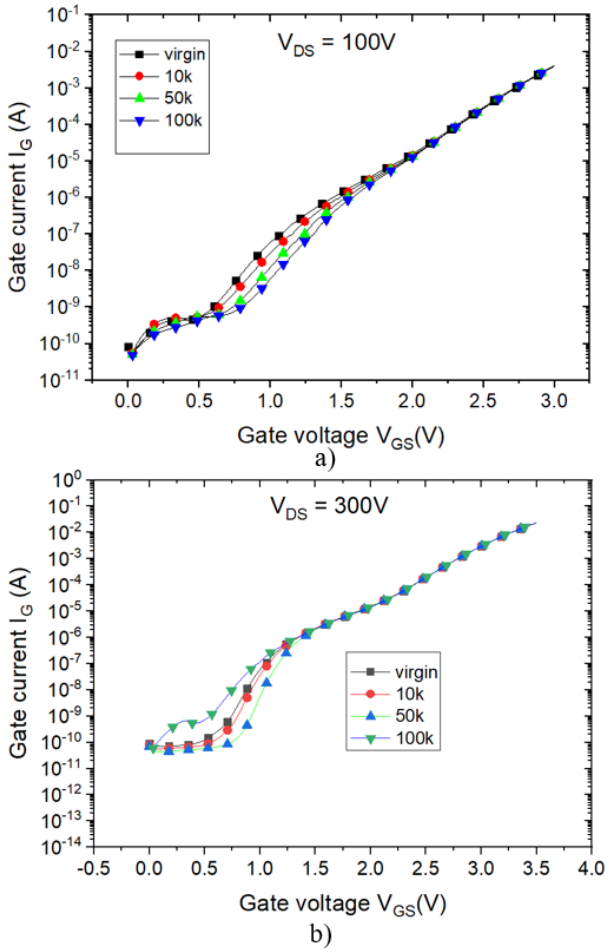

Fig. 7: Gate leakage current degradation. At 100V stress, there is an uniform trend, but more parameters are affected at 300V.

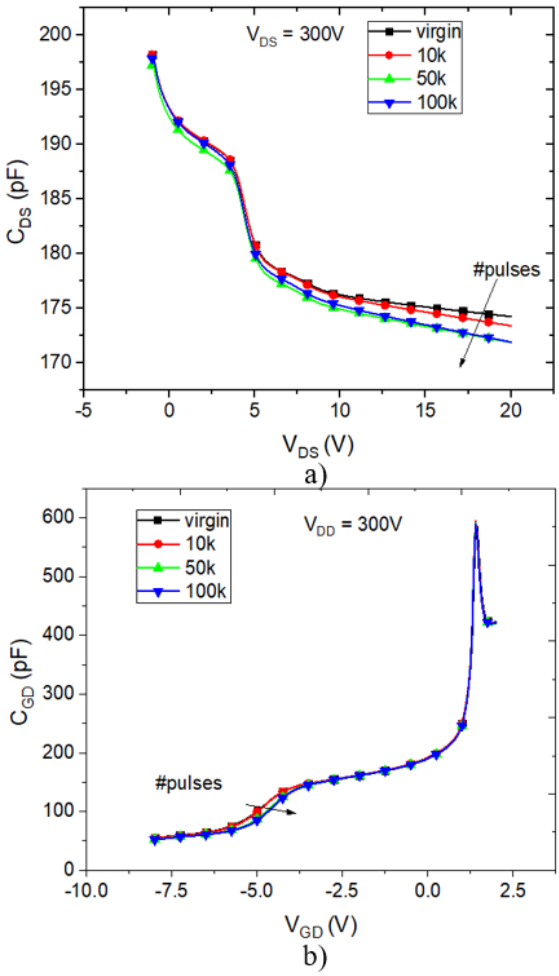

Fig. 8: Degradation of drain-to-source (C_{DS}) and gate-to-drain (C_{GD}) capacitances after 300V stress.

Gate leakage current $I_{G(LEAK)}$ degradation (Fig. 7) behaves in a similar manner as the transfer characteristics. At 100V stress voltage there is an decreasing trend of $I_{G(LEAK)}$ at gate voltages close to V_{TH}. However at V_{DS} = 300V there is no unequivocal trend, again suggesting different rate of degradation of at least two device parameters. Transistor capacitances were also ivestigated. The effect of 100V stress voltage on the capacitances was not significant. Degradation of drain-to-source (C_{DS}) and gate-to-drain (C_{GD}) capacitances after 300V stress are shown in Fig. 8. Both of them exhibit one-way shift, which is more pronounced in C_{DS} but only slightly visible in C_{GD}. Degradation of gate-to-source capacitance (V_{GS}) was negligible.

DLTS

To investigate possible generation of new traps, the DLTS spectra such as in Fig. 10 were measured on the virgin samples and compared to the spectra measured on the same samples after 10^5 SC stress cycles. First, several sets of measurements with various condition parameters were performed to map the distribution of the defects. The spectra were evaluated using the Fourier transform analysis by Direct auto Arrhenius Single and Multi-level evaluation and also by Tempscan maximum analysis [9].

Due to high complexity of obtained spectra it was difficult to evaluate parameters of all deep energy levels using the direct evaluation method. Therefore only traps that were verified by simulation and were present in most obtained spectra were evaluated. Positions of simulated DLTS peaks compared to measured spectra for both sets of measurement conditions are shown in Fig. 11. Parameters of 5 main evaluated traps are summarized in Table 1. Due to unknown active area of samples traps concentration was not evaluated. Analysis of possible origin of observed deep levels is still ongoing. Stated possible origins are first preliminary results. In Fig. 12 are shown DLTS spectra obtained on stressed samples for different stress conditions. First repetitive short circuit stress at 100 V was performed. Samples were exposed to 100k of stress pulses. Only small shift of DLTS spectra was observed, where small increase of signal for trap T1 dominated. Next gate stress was performed to analyse if shift of DLTS spectra is not induced by relatively high gate voltage present during stress pulses. From results it is clear that gate stress caused different shift of DLTS spectra. Signals of T1, T3 are decreased signalizing partial neutralization of this defects due to the stress.

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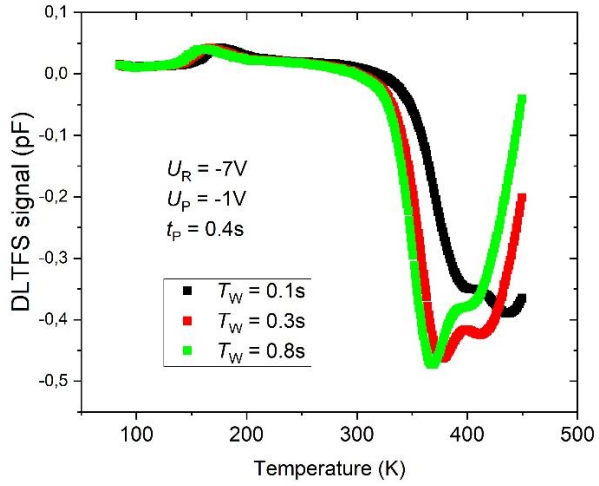

Fig. 10 Example of measured DLTS spectra of analysed sample of power HEMT before repetitive SC stress.

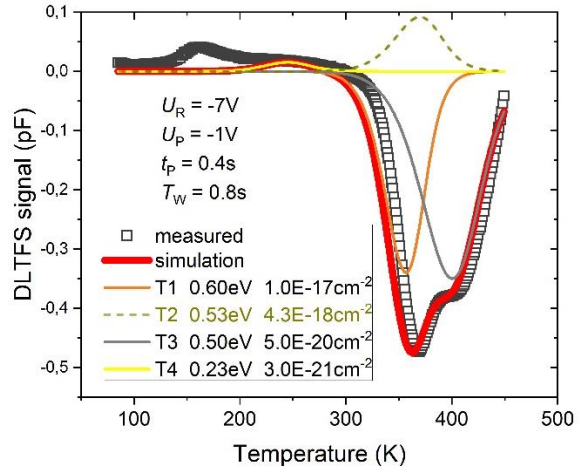

Fig. 11 Measured signals and simulated curves of DLTS defect states for selected measurement set.

Table 1: Parameters of observed deep levels

Trap	Activation energy ΔE_T (eV)	Capture cross section σ_T (cm^2)	Possible origin:
T1	0.6	1×10^{-17}	unknown
T2	Minority 0.53	4.3×10^{-18}	C_N deep acceptor states
T3	0.5	5×10^{-20}	Surface/interface states
T4	0.23	3×10^{-21}	Ga vacancy
T5	0.8	3.5×10^{-14}	GaN dislocations

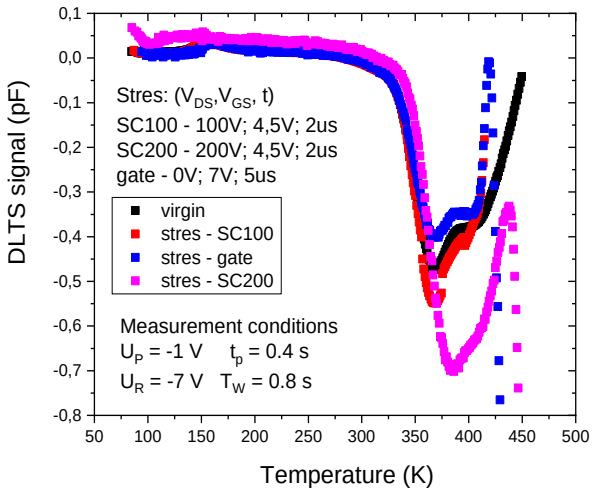

Fig. 12 Shift of DLTS spectra induced by different stress conditions

Finally, samples were exposed to repetitive SC stress at 200V. Significant shift of DLTS spectra was observed. Especially, signal of T1 and T2 traps was increased. Origin of trap T2 is believed to be C_N deep acceptor state (however, full analysis is still ongoing). These states are well known for their negative effects on dynamic on-resistance and current collapse phenomena [10]. Increase of T3, which origin may be in surface or interface states, may lead to decrease of carriers mobility in 2DEG and therefore has negative effect on device on-resistance and saturation current.

CONCLUSION

Gradual degradation of 600V GaN HEMT under repetitive SC stress was measured and analysed. Drain voltage above 300V (half of the nominal voltage) caused majority of tested devices to fail. At lower VDS measurable shift in device parameters and characteristics is observed. Higher stress voltage leads to higher degradation rate and more significant shifts of characteristics can be observed. However, particularly at higher stress voltage, shift of the characteristics does not have uniform character, pointing on at least three different mechanisms associated with generation of defects and trapping effects. The trapping was also analysed using DLTS. Due to high complexity of the spectra, only the traps verified by simulation were investigated. At 100V stress voltage, the shift in DLTS spectra was small, at 200V it was significant. The shift was verified not to originate from gate stress. Full analysis of possible origin of the observed deep levels is still ongoing.

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Addresses of the authors

Jozef Kozarik, FEI STU, Ilkovicova 3, 812 19 Bratislava, Slovakia, jozef.kozarik@stuba.sk
Juraj Marek, FEI STU, Ilkovicova 3, 812 19 Bratislava, Slovakia, juraj.marek@stuba.sk
Michal Minarik, FEI STU, Ilkovicova 3, 812 19 Bratislava, Slovakia, michal.minarik@stuba.sk
Ales Chvala, FEI STU, Ilkovicova 3, 812 19 Bratislava, Slovakia, ales.chvala@stuba.sk
Tomas Debnar, FEI STU, Ilkovicova 3, 812 19 Bratislava, Slovakia, tomas.debnar@stuba.sk
Martin Donoval, NanoDesign, s.r.o, Drotárska 19a, 811 04 Bratislava, Slovakia, martin.donoval@nanodesign.sk
Lubica Stuchlikova, FEI STU, Ilkovicova 3, 812 19 Bratislava, Slovakia, lubica.stuchlikova@stuba.sk