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CONTENTS

INVITED LECTURES

Key criteria for the short-circuit capability of IGBTs

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Abstract

Short-circuit behavior and capability are investigated and optimized during IGBT development. Thereby, knowledge about destruction and high-frequency short-circuit oscillation mechanisms is needed. For the thermal destruction mechanism, filaments are formed shortly before destruction during the thermal runaway itself, whereas for the electrical destruction mechanism strong current filaments are formed by an electrical mechanism, before the self-heating in the filaments leads to a thermal runaway. At low collector-emitter voltages, weak non-destructive filaments exist for a large current range. For both the filament formation and short-circuit oscillations (SCOs), an electric-field peak in the field-stop layer and a quasi-plasma layer beneath the MOS cells are mandatory. For SCOs, which are caused by a periodic storage and release of charge carriers inside the device, additionally, a weak electrical field at the beginning of the drift zone is necessary. Weak, non-destructive filaments and SCOs are likely to occur simultaneously. An increase of the bipolar current gain reduces the operating area with SCOs and increases the electrical short-circuit capability. A simultaneous reduction of the thermal short-circuit robustness can be avoided by advanced p-emitter concepts or (over-)compensated by an improved thermal setup.

Keywords: IGBT, short circuit, thermal short-circuit robustness, electrical short-circuit robustness, short-circuit destruction, high-frequency short-circuit oscillations, SOA

INTRODUCTION

For many industrial applications, IGBT chips and modules are required that have a certain short-circuit capability. During short-circuit operation, almost the entire DC-link voltage drops between collector and emitter, while the IGBT carries the driver and DC-link voltage-dependent saturation current, which is several times larger than the nominal current of the IGBT. IGBTs have to withstand a short-circuit incident for the time needed to detect the incident, and to turn-off the IGBT. The short-circuit robustness depends on parameters such as stray inductance during the short-circuit incident, emitter inductance, gate resistance, initial junction temperature and possible clamping circuits.

Short-circuit behavior and capability are investigated and optimized during IGBT development. Particular attention is paid on the thermal and electrical short-circuit robustness, and the occurrence of high-frequency short-circuit oscillations (SCOs). The optimization of the short-circuit capability can be challenging, because thermal short-circuit robustness, electrical short-circuit robustness and performance properties, such as conduction losses, switching losses and turn-off softness, are competing objectives. It can even be more challenging if undesired high-frequency SCOs need to be minimized in the application-relevant I_C-V_{CE} phase space.

For the short-circuit optimization of IGBTs, knowledge about destruction and high-frequency SCO mechanisms is necessary for identifying improvement measures. Therefore, this work gives an overview of the thermal and electrical short-circuit destruction mechanisms and the SCO mechanism. Improvement measures and interdependencies of these three criteria of the short-circuit capability of IGBTs are discussed.

SHORT-CIRCUIT TYPES

For the same DC-link voltage and collector current, the operating state of the IGBT at the moment of a short circuit can determine whether the IGBT is destroyed or not. Different short-circuit types can be distinguished (e.g. [1]). The two most important types for IGBTs are described subsequently.

Short-circuit type I

Characteristic for short-circuit type I (SC1) is the turn-on of the IGBT during an existing short circuit: the DC-link voltage is initially applied across the turned-off IGBT. When the gate voltage exceeds the threshold voltage, the collector current increases, causing a voltage drop across the stray inductance, and thus, a di/dt-dependent reduction of the collector-emitter voltage below the DC-link voltage. If a certain switching speed is exceeded, a collector-current overswing and a subsequent overvoltage occur during the transition to the short-circuit operating point. As long as the IGBT remains in the active region, both the collector-current overswing and

the overvoltage are significantly smaller for SC1 than for short-circuit type II.

Short-circuit type II

Characteristic for short-circuit type II (SC2) is the occurrence of the short circuit while the IGBT is turned on. During SC2, collector current and collector-emitter voltage increase initially according to the corresponding output characteristic. The displacement current through the voltage-dependent feedback capacitance causes a voltage drop across the gate resistances. Therefore, the gate-emitter voltage increases above the driving voltage, and with that, a relatively large collector current overshoot can be caused. The subsequent overvoltage during the negative d*i*/d*t* can be significantly above the DC-link voltage. Accordingly, the stress and the dissipated energy during the transition into the short-circuit operating point is usually larger for SC2 than for SC1.

THERMAL SHORT-CIRCUIT CAPABILITY

Characteristics of thermal short-circuit destructions

For long enough short-circuit pulses, a thermal destruction can occur within the pulse. Nevertheless, the thermal or energy short-circuit robustness is usually related to the destruction of an IGBT after its turn-off. The IGBT can withstand the short-circuit pulse and turn-off; however, some hundreds of microseconds up to milliseconds after the pulse, leakage currents increase and the IGBT is destroyed. For a given setup, the thermal destruction depends mainly on the dissipated energy during the short-circuit pulse [2]-[3], and is more critical for low-voltage IGBTs and relatively thin IGBTs.

Measurement of the critical short-circuit energy

By increasing the short-circuit pulse width in small increments (e.g. of 0.2 µs) until destruction, the critical short-circuit energy can be measured for defined test conditions. Usually, the device under test (DUT) is measured at a high initial device temperature, a high DC-link voltage, a typical driver voltage, and typical stray inductance and gate resistance.

Simulation setup and destruction mechanism

The thermal short-circuit capability of IGBT chips can be investigated by an electro-thermal device simulation which takes the electrical and thermal setup into account [4]. The thermal setup enables the simulation of the heat transport out of the silicon chip. It could e.g. consider the front-side metallization, the solder beneath the collector and the direct bonded copper (DBC) as insulator with their specific heat conductivities and heat capacitances. Effects due to an inhomogeneous current distribution are of minor importance, because once they have an impact on the critical short-circuit energy, the destruction occurs within and not after the short-circuit pulse [11]. Therewith, half-cell simulations are sufficient, since homogeneous self-heating can be assumed in the active area [5].

Such electro-thermal device simulations show that during the short-circuit pulse, the temperature increases mainly in the drift zone. After the pulse, the heat diffuses to the chip's front and back side. There, the rising temperature causes increasing leakage currents, which are amplified by the bipolar current gain of the collector-sided *p*-*n*-*p* transistor α_{pnp}. The leakage currents depend on the dissipated energy during the short-circuit pulse, the thermal setup and the IGBT chip. Up to a certain energy dissipation, the transient increase of the leakage current is followed by a decrease of the leakage current (Fig. 1). However, beyond a critical short-circuit energy, the leakage current keeps increasing. Excessive leakage currents lead to an almost homogenous self-heating of the chip. After the critical temperature is reached, a local thermal runaway due to latch-up occurs at a position with a slightly higher temperature. The corresponding current crowding destroys the chip.

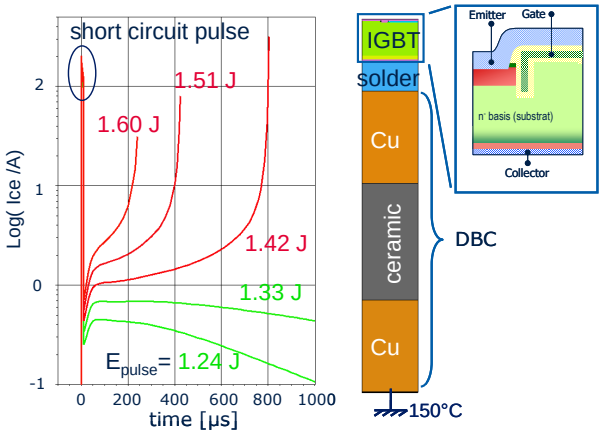

Fig. 1: Electro-thermal simulation. Left picture: the collector emitter current (log scale) initially increases after the short-circuit pulse, and leads to device destruction if a critical energy is exceeded. Right picture: IGBT cell and mounting setup. (picture from [4])

Measures for an improved thermal short-circuit robustness

The destruction mechanism indicates possible improvements of the thermal short-circuit capability:

- Lowering the bipolar current gain of the collector-side *p*-*n*-*p* transistor α_{pnp} would result in a reduced leakage-current amplification, and with that, an increased thermal short-circuit robustness.
- A better heat transport out of the chip would reduce leakage currents due to a reduction of the maximum temperature at the chip front and/or back. As shown in [4], the combination of large heat capacities at the chip front side and a die-attach concept with a high thermal conductivity at the back side is most efficient for reducing the maximum chip temperature at a given short-circuit energy, and enables a significant improvement of the thermal short-circuit capability.

The bipolar current gain of the collector-sided *p*-*n*-*p* transistor α_{pnp} can e.g. be reduced by a decrease of the *p*-emitter dose or an increase of the field-stop dose. For a conventional soft solder die attach with a thickness of e.g. fifty microns, the heat capacitance at the chip front side can be significantly increased if an aluminum front-side metallization with a thickness of a few microns is replaced by a copper metallization that is thicker by a factor of two or five. Since diffusion solder is almost one order of magnitude thinner than the conventional soft solder, the thermal conductivity at the chip's back side can e.g. be improved, if a conventional soft solder is replaced with a diffusion solder. An enormous increase of the critical short-circuit energy can only be achieved if cooling measures minimize leakage currents at both chip sides (Fig. 2). As soon as the front side is able to heat up, the corresponding leakage-current increase is amplified by the bipolar current gain. A temperature increase and the corresponding leakage-current increase at the back side cause an increasing temperature and leakage current at the emitter, which is again amplified by the bipolar current gain. Hence, improving the thermal setup only at one side yields in a limited improvement of the critical short-circuit energy.

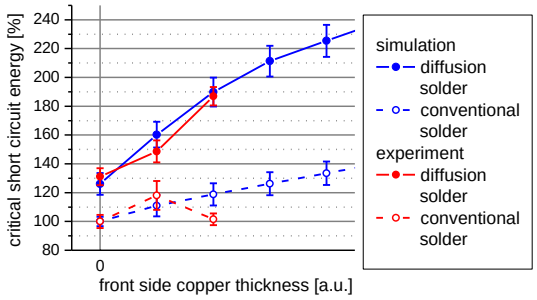

Fig. 2: Improvement potential of critical short-circuit energy on a relative scale. The aluminum front side is represented as 0 µm copper. Error bars for the simulation results are caused by the discretization of gate voltages. (picture from [4])

ELECTRICAL SHORT-CIRCUIT CAPABILITY

Measurement of the critical short-circuit current

The electrical or current short-circuit robustness is related to the destruction of IGBTs within a short-circuit pulse. The electrical short-circuit capability is usually investigated by a series of short-circuit pulses with low initial device temperature, a fixed DC-link voltage, a fixed pulse width and an incremental increase (e.g. in steps of 0.2 V) of the gate-emitter voltage until destruction. From the last non-destructive pulse, the critical short-circuit current can be extracted. For the measurement of a critical short-circuit current close to the chip's intrinsic critical short-circuit current, a low-inductive measurement setup and appropriate gate resistances must be used. The gate resistances should be high enough to damp current and voltage peaks, and low enough to limit self-heating during the transition into the short circuit.

The chip's current destruction limit, which is well above the save operating area (SOA), depends on the collector-emitter voltage (Fig. 3). For medium and high-voltage IGBTs, the current destruction limit has a minimum value at medium collector-emitter voltages [8]-[10].

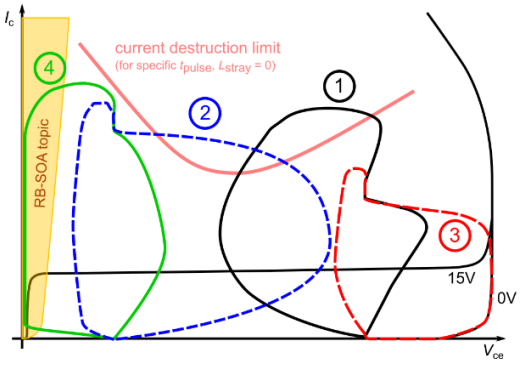

Fig. 3: Schematical view of the I_C-V_{CE} phase diagram with the 15 V- and 0 V-output characteristics, the current destruction limit and i_C-v_{CE} trajectories of the different non-destructive SC1 incidents close to the four failure modes (picture from [9])

Failure modes and electrical destruction mechanism

According to Fig. 3, four different failure modes can be distinguished [8]:

- pulse failure (failure mode 1),
- turn-off failure (failure mode 2),
- static clamping turn-off failure (failure mode 3) and
- turn-off in a transient low-voltage stage failure (failure mode 4).

However, only failure modes 1 and 2 are related to the current destruction limit. Failure mode 3 is linked to the blocking capability, and failure mode 4 to the reverse-biased safe operating area. Hence, failure modes 3 and 4 are not further discussed in this paper. Failure modes 1 and 2 correlate to current filaments, which are initiated at the drift-zone field-stop junction. If the IGBT stays too long in the area above the chip's current destruction limit, the current filaments become strong enough to provoke a local thermal runaway in the current filament(s) with the strongest self-heating [10]. Due to the dynamics of the thermal runaway, the destruction often occurs when the area with destructive filaments in the phase diagram is already passed. However, the time delay is significantly smaller than in the case of the energy destruction.

The i_C-v_{CE} trajectories, the duration in the area above the chip's current destruction limit and, thus, the critical short-circuit current depend strongly on the stray inductance, the turn-on and turn-off gate resistance, the pulse width [9] and the operating condition of the IGBT at the moment of the short circuit. For SC1, failure mode 1 is likely to occur for higher DC-link voltages, where the critical short-circuit current increases with the collector-emitter voltage, as the critical area is passed during the transition to the short-circuit operation. In contrast, failure mode 2 can be expected for lower DC-link voltages, where the current destruction limit decreases with the collector-emitter voltage, as the critical area is passed

during the IGBT's turn-off. At lower DC-link voltages, the IGBT can endure current filaments relatively long due to their limited energy dissipation. A high enough overvoltage during the IGBT's turn-off and the corresponding energy dissipation might also be sufficient for the destruction even though the critical area is not passed.

TCAD simulation of the filamentation border

TCAD simulations show that the relocation of the electric-field peak from the chip front side towards the field-stop layer [6]-[7], and the occurrence of a low-field/quasi-plasma region beneath the MOS cells [8], are necessary for the filament formation. The short-circuit current/gate-emitter voltage at which these two conditions are fulfilled increases with the collector-emitter voltage (Fig. 4).

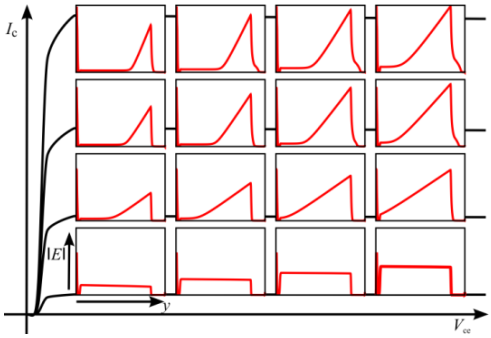

Fig. 4: Simulated electric-field distributions for different collector-emitter voltages and different gate voltages (left: emitter, right: collector). Schematic IGBT output characteristics are displayed in the background. (picture from [10])

In [10], the ratio of the gradients of the electric-field strength in front of the field-stop layer and below the cell field at the beginning of the drift zone,

$$c = \frac{(\mathrm{d}E/\mathrm{d}y)|_{\text{near field stop}}}{(\mathrm{d}E/\mathrm{d}y)|_{\text{near front side}}} \qquad (1)$$

was introduced for estimating the appearance of a quasi-plasma at the beginning of the drift zone (Fig. 5). For different collector-emitter voltages, the ratio is calculated during the simulation of the transfer characteristic. For ratios significantly above 1, a quasi-plasma layer builds up and filaments may occur. This simple and phenomenological criterion can be adjusted to the increasing branch of the measured destruction limit (Fig. 6). A large collector-current range between the measured destruction limit and the estimated filamentation border exists at lower collector-emitter voltages. In this area, at a certain current significantly below the current destruction limit, the measured critical energy starts to decline, and the failure mode changes from a thermal to an electrical destruction [11]. The change in the failure mode at this transition current can be explained by weak current filaments that remain non-destructive due to their relatively low energy dissipation. The existence of non-destructive current filaments in the area between the filamentation border and the destruction limit could also be confirmed by images of thermal-reflectance measurements, which show a regular pattern above the estimated filamentation border, for different points in the I_C-V_{CE} phase space above the safe operating area (SOA) [12].

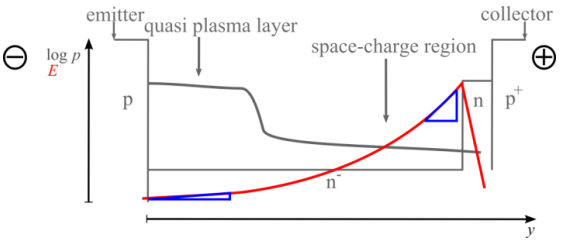

Fig. 5: Schematic view of the hole density (gray) and the electric-field strength (red) in an IGBT during a short circuit with a high current (picture taken from [5])

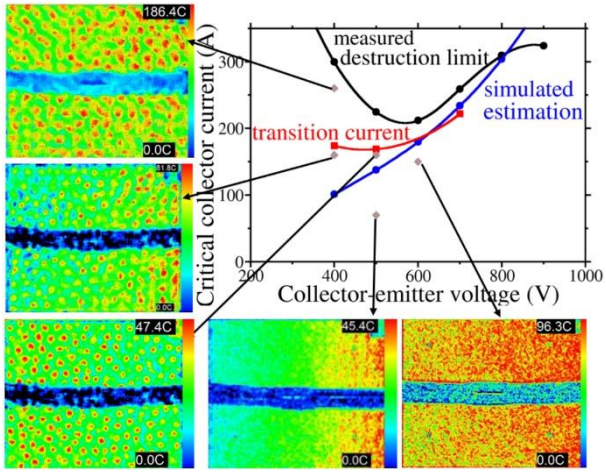

Fig. 6: I_C-V_{CE} phase diagram with critical SC current (of last non-destructive pulse) of a 1200 V IGBT (black line), the borderline for the appearance of a front-side plasma layer estimated by TCAD simulations with c = 30 (blue) [10] and transition current between energy and electrical destruction (red) together with thermal reflectance measurements for certain points [12] (picture taken from [11])

Measures to improve the electrical short-circuit robustness

By increasing the value of α_{pnp}, the relocation of the electric-field peak, the occurrence of a quasi-plasma layer, and thus, the electrical short-circuit destruction can be shifted to higher I_C values. However, it should be kept in mind that for very high α_{pnp} values, dynamic avalanche is triggered [7]. Advanced concepts, such as the injection enhanced floating emitter, enable the improvement of the electrical short-circuit capability without reducing the thermal short-circuit capability as the hole injection is only enhanced during short-circuit conditions [13].

HIGH-FREQUENCY SHORT-CIRCUIT OSCILLATIONS

During short-circuit operation high-frequency short-circuit oscillations (SCOs) may be present. Their occurrence depends on both the chip and the circuit design. Typically, SCOs occur at low junction temperatures in a DC-link voltage interval well below the nominal voltage.

Measurement of SCOs

A sample measurement with SCOs is shown in Fig. 7. SCOs do not only depend on the DC-link voltage $V_{DC\text{-}link}$, they also depend strongly on the driver voltage V_{Dr}. For a test-vehicle chip, which was intentionally designed with a large operating area with SCOs and strong oscillation amplitudes, this is shown in Fig. 8. For determining of the V_{Dr}-$V_{DC\text{-}link}$ phase space with SCOs, the minimum and maximum DC-link voltage and the minimum driver voltage with SCOs were determined by means of test measurements. Afterwards, a measurement matrix was specified. Within this matrix, the DC-link voltage was varied in 25 V steps and the driver voltage in 100 mV steps. The measured short-circuit conditions were then assigned to one of the following categories, whereby, the second half of the short-circuit pulse was considered as quasi-stationary (Fig. 7).

- The red category is characterized by SCOs during the quasi-stationary short circuit.
- The green category is characterized by no SCOs during the quasi-stationary short circuit.

With their corresponding color code, the operating points were drawn into the V_{Dr}-$V_{DC\text{-}link}$ phase space (Fig. 8, top). Additionally, the maximum gate voltage variation (Fig. 8, middle) and the dominant oscillation frequency (Fig. 8, bottom) were evaluted. Although the device under test was intentionally designed with a large operating area with SCOs and strong oscillation amplitudes, it was not destroyed during the measurements.

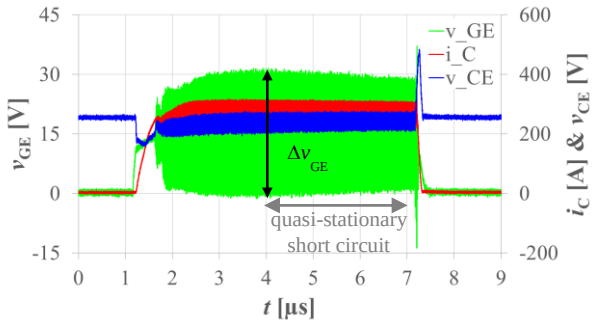

Fig. 7: Measured transients $v_{GE}(t)$, $i_C(t)$, and $v_{CE}(t)$ for a short-circuit pulse with V_{Dr} = 15 V, $V_{DC\text{-}link}$ = 250 V and T_J = 300 K of a 1200 V IGBT test-vehicle chip

Simulation setup and intrinsic SCO mechanism

TCAD simulations of a circuit with just one IGBT cell, a driver and a DC-link voltage source demonstrate that IGBTs can already have a built-in ability to SCOs for some operating points [15]. For the TCAD simulation of intrinsic SCOs, a two-step simulation procedure was proposed [15]. First, the operating point was simulated in a quasi-stationary manner by simulating a transfer characteristic or output characteristic up to the operating point. The result of the quasi-stationary simulation was then used as initial condition for the second step: the transient isothermal simulation of the operating point.

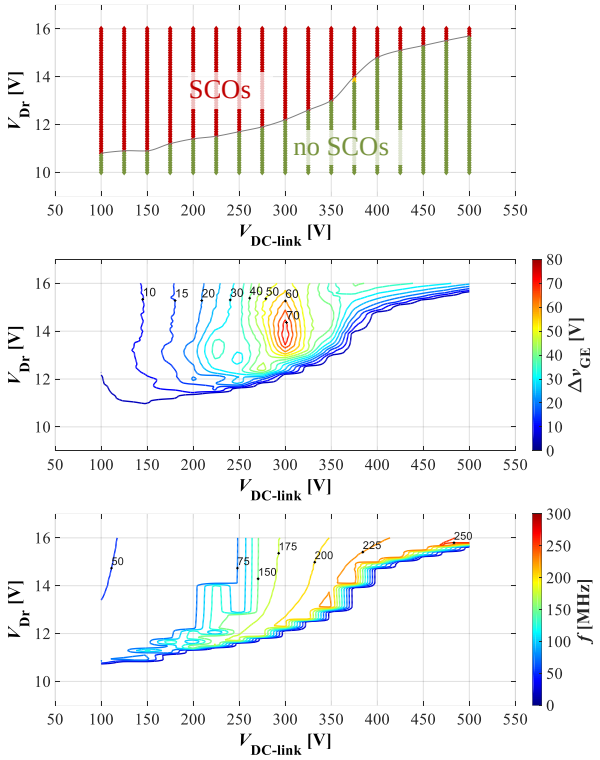

Fig. 8: Measured V_{Dr}-$V_{DC\text{-}link}$ phase space with SCOs at room temperature (top), the corresponding contour plots of the maximum gate-voltage variation Δv_{GE} (middle), and the dominant oscillation frequency f (bottom) during the quasi-stationary short-circuit of a 1200 V 100 A IGBT test-vehicle chip (picture from [15])

The collector and emitter currents of a transient simulation of an operating point with SCOs are depicted in Fig. 9. After a transition time with increasing oscillation amplitudes, permanent oscillations with an almost constant oscillation amplitude occur. At the front side, the electron current is almost constant due to the fixed gate-emitter voltage. However, at the back side the electron current has a significant oscillation amplitude. The hole current has a smaller oscillation amplitude at the collector than at the emitter. The different electron- and hole-current amplitudes at the emitter and the collector indicate a periodic storage and release of charge carriers in the IGBT cell during the intrinsic oscillation.

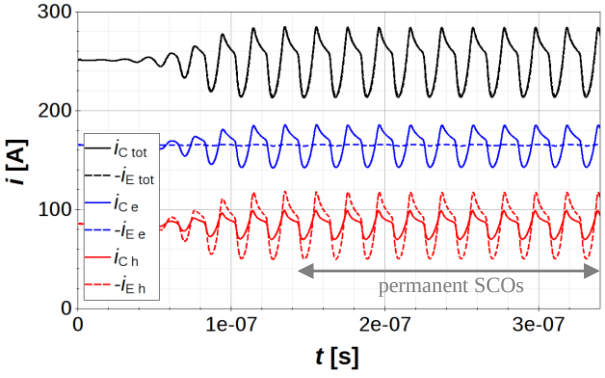

Fig. 9: Simulated total, electron and hole current at collector and emitter of an operating point with high-frequency SCOs (V_{Dr} = $v_{GE}(t)$ = 13.5 V, $V_{DC\text{-}link}$ = $v_{CE}(t)$ = 200 V, T_J = 300 K)

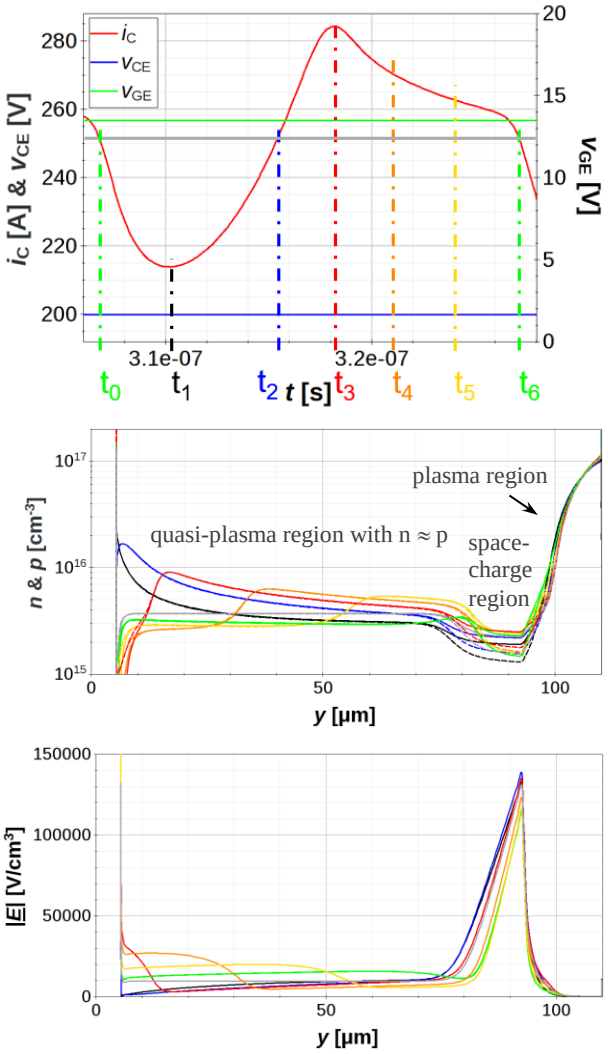

Fig. 10: Vertical distributions of electrons (solid lines) and holes (dashed lines) (middle), and of the electric-field strength (bottom) at the indicated points of one oscillation period (top). The gray characteristics show the result of the corresponding quasi-stationary simulation.

The distributions of carrier densities and the electric-field strength at selected points in time of one oscillation period during permanent SCOs are shown in Fig. 10. At t_0, the transient collector current equals the collector current of the corresponding quasi-stationary simulation of the operating point. However, compared to the corresponding quasi-stationary simulation, fewer carriers are present in the drift-zone at t_0. Between t_0 and t_2, the collector current is smaller than in the quasi-stationary simulation, as a significant number of charge carriers is stored in the drift zone. Since electrons are stored in the drift zone, the electron current at the collector is smaller than at the emitter. The storage of holes in the drift zone results in a reduced hole current at the emitter (Fig. 9). At t_2, the collector current of the quasi-stationary simulation is again reached. However, many more carriers are present in the drift zone at t_2. After t_2, the transient collector current is larger than the quasi-stationary current. Between t_2 and t_3, a carrier front develops and propagates towards the collector. At the front, electrons and holes are released. The electrons flow to the back side and increase the electron current at the collector. The holes flow to the front side and increase the hole current at the emitter. Since most of the carriers are stored at the beginning of the drift zone, fewer carriers are released at the front. The carrier confinement in the drift zone causes the characteristic current shape between t_2 and t_6. At t_6, the collector current of the quasi-stationary simulation is reached again, and the charge-carrier storage and release start again. Although most of the carriers are stored at the beginning of the drift zone, and thus, close to the gate trench, MOS capacitances are not necessary for the intrinsic SCO mechanism [15].

An electric-field peak in the field-stop layer and a quasi-plasma layer beneath the MOS cells are mandatory for the occurrence of high-frequency SCOs. Additionally, a weak electrical field beneath the MOS cells is necessary [14], [15]. Since the electric field builds up in the quasi-plasma layer with increasing V_{CE} and I_C values, SCOs usually disappear in well-designed IGBTs until approximately one-third of the nominal voltage, and well before the electrical destruction current. Accordingly, we have not seen a destruction due to SCOs in our extensive SCO measurements of IGBT chips of different generations and voltage classes.

The electric-field peak in the field-stop layer and a quasi-plasma layer beneath the MOS cells are also necessary for the filament formation. Under conditions where the electric-field strength in the quasi-plasma layer at the beginning of the drift zone is not too large, SCOs and non-destructive filaments are therefore likely to occur simultaneously near the filamentation border (Fig. 11).

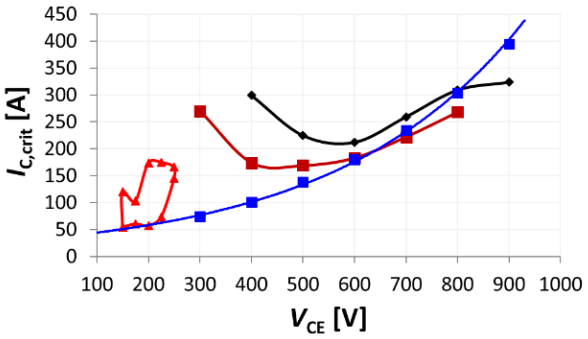

Fig. 11: Critical SC current (of last non-destructive pulse) depending on V_{CE} of a 1200 V IGBT for L_{stray} = 70 nH and 25°C (black line), borderline for the appearance of a front-side plasma layer estimated by TCAD simulations with c = 30 (blue), transition current between electrical and energy destruction (brown) as well as measured operating area with SCOs (red)

The oscillation frequency depends strongly on the shape of the electric field and the corresponding carrier velocities. The oscillation frequency increases with the DC-link voltage, as the space-charge region (with relatively high electric-field strengths) extends, and decreases slightly with the driver voltage, as the quasi-plasma layer (with relatively low electric-field strengths) widens (cp. Fig. 8 (bottom) with Fig. 4).

Measures to reduce high-frequency SCOs

An increased α_{pnp} strengthens the electric field beneath the MOS cells, and thus, reduces SCOs. Accordingly, both the area with SCOs and the oscillation amplitudes decrease for a decreasing field-stop dose (Fig. 12, top) and an increasing p-emitter dose (Fig. 12, bottom). The reduction of the operating area with SCOs goes along with an increased electrical short-circuit robustness. However, unless advanced concepts, such as the injection enhanced floating *p*-emitter, are used, an increase of the bipolar current gain results in increased leakage currents and a reduced thermal short-circuit capability. An improved thermal setup could (over-)compensate an increased bipolar current gain.

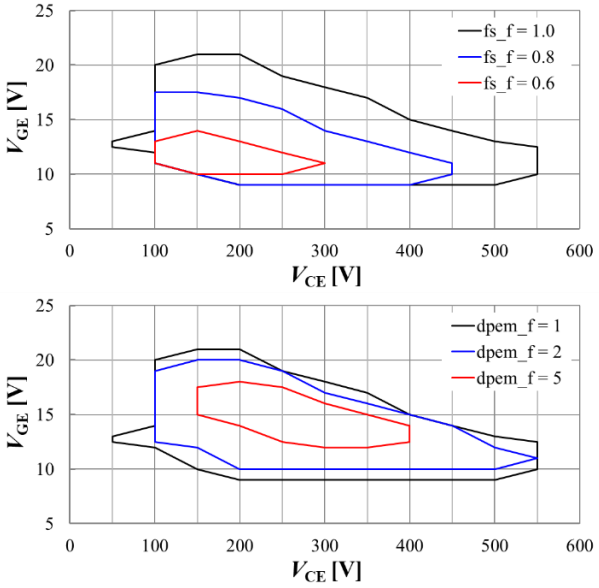

Fig. 12. Comparison of the simulated SCO OA border of the 1200 V IGBT structure for a variation of the initial field-stop dose by the factor *dfs_f* (top) and for a variation of the initial *p-emitter* dose by the factor *dpem_f* (bottom) (picture from [15])

The occurrence of SCOs does not only depend on the chip design, the circuit design has also an impact as e.g. shown in [16].

CONCLUSIONS

Current filaments and local thermal runaway are characteristic of both the thermal and the electrical short-circuit destruction mechanism. Accordingly, in both cases, the failure picture shows a local melting of metallization and silicon in the active area [11]. However, for the thermal destruction mechanism, filaments are formed shortly before destruction during the thermal runaway itself, whereas for the electrical destruction mechanism strong filaments are first formed above the SOA by an electrical mechanism before the self-heating in the destructive current filament leads to a thermal runaway.

At low collector-emitter voltages, weak, non-destructive current filaments may exist for a large collector current range. For the filament formation and the occurrence of SCOs, both an electric-field peak in the field-stop layer and a quasi-plasma layer beneath the MOS cells are mandatory. Accordingly, weak, non-destructive current filaments and SCOs are likely to occur simultaneously. However, for SCOs, which are caused by a periodic storage and release of charge carriers in the device, additionally, a weak electrical field beneath the MOS cells is necessary.

An increase of the bipolar current gain reduces the operating area with SCOs and increases the electrical short-circuit capability. The simultaneous reduction of the thermal short-circuit robustness and the impact on performance properties, such as conduction and switching losses and turn-off softness, can be avoided by advanced concepts, such as the injection enhanced floating *p*-emitter, or compensated by an improved thermal setup. The thermal short-circuit capability can be improved significantly by improved double-sided cooling without affecting the electrical short-circuit capability and performance properties.

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New Packaging Concepts: Bridging Devices and Applications

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Abstract

The performance of power modules has continued to improve with Si IGBTs (Insulated Gate Bipolar Transistors), and current capacities ranging from several A to several thousand A and rated voltages ranging from several hundred V to several thousand V have been realized. However, with the expansion of power electronics applications and the demand for even higher efficiency, the specifications required for power modules are becoming more diverse, with lower loss, smaller size and weight, higher density, environmental resistance, longer life and so on. In addition, WBGs (Wide Band-gap semiconductors) such as SiC and GaN have been commercialized, and innovative approaches to bring out the performance of these devices are expected.
In this paper, we will discuss the latest trends and future prospects of packaging technology for power modules in the domain of die bonding, wiring, encapsulation, insulation, and functional integration.

Keywords: power module, packaging,

1. Introduction

The power modules are at the forefront of the latest energy innovations that seek to solve global environmental issues while creating a more affluent and comfortable society for all. Some of these innovations are photovoltaic (PV) and wind power generation from renewable energy sources, smart grids realizing efficient supply of power, electric vehicles (xEV) that take the next step in reducing carbon emission and fuel consumption, and home appliance that achieve ground-breaking energy savings. Whether in appliances, railcars, xEV or industrial systems, the power modules are key elements in changing the way energy is used.

As the application of power modules expands, the performance requirements and operating environments for power modules are becoming more and more diverse. In order to achieve these requirements, it is important not only to improve the characteristics of power semiconductor devices, but also to maximize their performance and to protect them from external factors through the use of packaging technology [1].

2. Power module

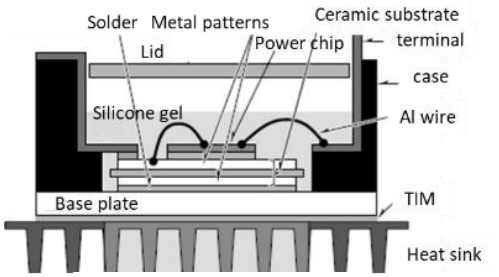
Since power semiconductors cannot be directly installed in equipment, power modules are those that are packaged so that they can be built into equipment. The role of the package is to provide electrical and mechanical interface with systems and protection from external stress.

Figure 1 shows the package structure of a conventional power modules. One is a case-type package, which is mainly used for high-voltage industrial equipment. It consists of insulating substrates and semiconductor chips stacked on a metal base plate via solder, and put into a plastic case. Inside the case, aluminum wires are used to connect the chips to each other, to the substrate and to external terminals. And the inside of the case is filled with silicone gel. They are fixed to the heat sink via a TIM (Thermal Interface Material) such as silicone grease, and the heat generated by the power semiconductor is dispersed through the solder, insulating substrate, base plate, and TIM to the outside by the heat sink. As the semiconductor type, combination, and layout can be changed according to the required specifications, the advantage of them is that it offers a design flexibility.

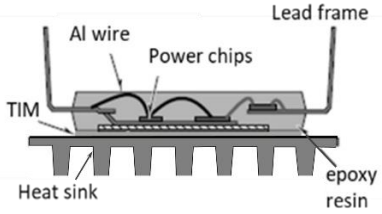
The other is a transfer molded package, which is used for applications with relatively small power, like home appliances. The structure consists of a semiconductor chip soldered onto a copper lead frame, wired with aluminum wires, and encapsulated with epoxy resin. Then, as with the case-type module, it is fixed to the cooling fins via TIM. Transfer molding technique leads to high productivity.

In either structure, the functions required for a power module are ; bonding the semiconductor chips to an insulating substrate or lead frame, electrically connecting internal and with the external terminals, encapsulating with insulating material, and making a path to release the heat generated by the power semiconductor to the

outside. In other words, die bonding, wiring, encapsulation, and insulating substrate technologies are the essential packaging technologies for power modules.



(a) Case-type module



(b) Transfer molded module

Fig.1 Package structure of power modules

3. Packaging technologies

3.1 Die bonding

In accordance with the RoHS Directive, which restricts the use of lead, tin-based solders are now being mainly used [2]. To achieve the high Tj operation expected for SiC devices, sintering technologies using fine metal particles, such as nano-silver, is being adopted [3] [4]. In general, sintering requires high pressure under high temperature, which causes stress on the semiconductor chip (die). Processes to reduce the stress and materials that can be sintered with low pressure are being developed[5].

3.2 Wiring

Currently, aluminum or its alloy wire is used for internal connecting between semiconductor chips, to patterns on substrate, and terminals. In order to achieve high current density and high Tj operation, the use of copper wire has been proposed. However, since the copper wire bonding process requires a large power, it is necessary to form a hard metal layer such as copper or nickel on the semiconductor chip surface as a buffer layer to protect the device structures and chip itself. There are two methods being considered for applying the buffer layer directly by plating, or by attaching a metal plate via sintered materials onto the chip surface[6] [7] [3].

Lead-frame interconnect technology has also been adopted to address high current density. Bonding materials and buffer structures are being considered to protect the device structure on the chip surface from thermal stress[8] [9].

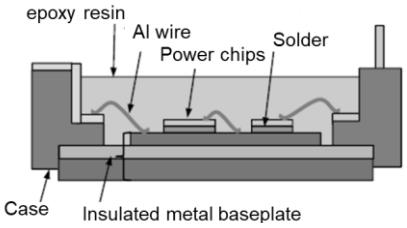
3.3 Substrate

Dielectric strength and thermal conductivity as a heat dissipation path are required for the substrate. In general, the substrates are made of ceramics with metal laminated on both sides. Ceramic materials with high strength and high thermal conductivity and methods of applying thick metal patterns are being investigated to overcome the high Tj operation and thermal stress caused by it [10].

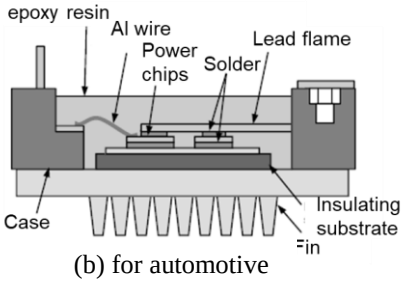
Such ceramic substrates have the problem of warpage in assembly and operation due to the large difference in CTE (Coefficient of expansion) between ceramic and metal patterns. To compensate for this problem, organic/inorganic composite insulating materials with tuned CTE have been commercialized [11].

As another important function, heat dissipation, a structure in which the insulating substrate and cooling fins are integrated has been proposed. This structure eliminates the solder layer and TIM under the substrate, which lowers the thermal resistance and also has the advantage of extending the life of the module [12] [13].

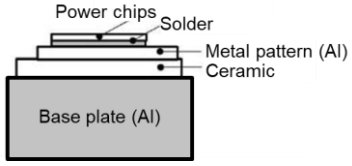
Some examples of new insulating substrate structure concepts are shown in Figure 2. Depending on the application, different properties are considered important. Various approaches have been presented to achieve a balance between performance and cost.



(a) for industry



(b) for automotive



(c) for HV

Fig. 2 New insulating substrate structures

3.4 Encapsulation

The function of the encapsulation is to protect the semiconductor chip and interconnection from electrical and environmental influences. Silicone gels are commonly used in case-type module, but their low molecular compositions make their performance unstable at high temperatures, also has a crystallization point around -60 °C, which limits its use at high and low temperatures. Their permeability to gas and water limits their use in harsh environments. Epoxy-based resin encapsulation is expected to break through these limitations. Epoxy resins are widely used in transfer molded modules, but their design flexibility is limited as they use a molding die for pressurization. In order to combine the ease-of-process of silicone gel with the robustness of transfer molded resin, thermosetting epoxy resins that can be poured in liquid have been developed [14].

4. Functional integration

Integration of functions is required for modules with WBGs and new applications, in addition to the conventional functions of easy of connection and protection from external stresses.

One approach is to “embed” components into the module, such as ICs for driving, various sensors for condition monitoring, and passives for protection and noise reduction. Smaller and more heat-resistant components, and methods of thermal isolation within the module are being considered [15] [16].

Another approach is to “build” the functionality into the module. The integration of sensors and drivers on semiconductor chips has been used. Also, methods of forming passive circuits by applying multilayer circuit technology of PCB and LTCC are being studied [17] [18].

5. Prospects for the future

The power electronics systems are expected to have higher functionality, higher efficiency, and wider applications in order to utilize electric energy with less loss. WBGs such as SiC and GaN are being promoted as a key to next-generation power electronics. In order to bring out the advantages of these WBGs, not only semiconductor technology but also innovative module technology is required. Therefore, expectations for packaging technology will become more and more important in the future.

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ORAL PRESENTATIONS

Aluminium modification as indicator for current filaments under repetitive short-circuit in 650 V IGBTs

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Abstract

In this work, an investigation of the top-side aluminium (Al) metallization modification, under repetitive short-circuit (SC) type I measurements, was carried out for 650 V IGBTs. These measurements were performed far beyond the safe operating area (SOA). The presence of current density filaments at the collector side during SC leads to a local temperature increase that reconstructs the emitter metallization and thus leads to a modification of the top Al surface. Here, the optical microscope was used to observe the change in emitter surface metallization. For 650 V IGBTs, a uniform Al modification pattern was observed irrespective of DC-link voltage and SC pulse width, which is in contrast to the results of 1200 V and 1700 V IGBTs. The computer-aided TCAD simulations were performed using a simplified front-side IGBT structure to understand the uniform Al modification on all the measured DC-link voltages.

Keywords: IGBT, short-circuit, current filaments, aluminium modification.

INTRODUCTION

IGBTs are one of the frequently used power semiconductor devices in the field of power electronics. One of the important properties of the IGBT is SC robustness. Even though the IGBT has many advantageous features, it requires a detailed investigation regarding its physical limit during SC operation beyond the safe operating area (SOA).

The short-circuit safe operating area (SC-SOA) for different voltage classes ranging from 1200 V to 6500 V has been investigated in [1-6]. The results shown in [6], explain that IGBT SC destruction can be due to the formation of current filaments occurring at the collector side. These current destructions occur far beyond the SOA [7]. Further experimental investigations, carried out in [8], showed that it is possible to observe the current filaments in the IGBTs using Thermo-Reflectance Microscopy (TRM) under repetitive SC operation. A wide range of non-destructive current filaments was observed for IGBTs and these current filaments occur in a regular pattern [8]. The current filaments generate a similar pattern imprint visible as local Al modification under repetitive SC conditions. Hence, the optical microscope was used to study the local Al modification as an indicator of current filaments in 1200 V and 1700 V IGBTs [9-11]. Generally, for lower DC-link voltages, non-destructive current filaments can be observed under repetitive SC measurement. As the applied DC-link was increased, the filament pattern became finer, and transformed into a substantially homogeneous current distribution [11].

In the present work, repetitive SC measurements were performed on 50 A - 650 V class IGBTs with trench technology using an open, encapsulated chip soldered on a direct copper bonded (DCB) substrate. The repetitive SC measurements show a uniform Al modification of the emitter metallization irrespective of the DC-link voltages and collector current. Even though the SC pulse width was reduced, the Al modification remains uniform for all the measured SC conditions. These results were contrary to 1200 V and 1700 V IGBTs. Hence, TCAD simulations were carried out for 650 V IGBTs to study the reason for the homogenous Al modification at different DC-link voltages.

ALUMINIUM MODIFICATION THEORY

The study about Al surface modification on silicon due to thermal cycling was recorded in [12]. During power cycling, the change in the Al metallization was observed due to periodic stress [13]. This modification of the Al metallization due to compressive and tensile stress during heating and cooling phases leads to the protrusion or cavitation of single Al grains. Thereby, the roughness and electrical resistance of the Al metallization increases [13, 14, 15].

SETUP FOR REPETITIVE SHORT-CIRCUIT (SC) MEASUREMENT

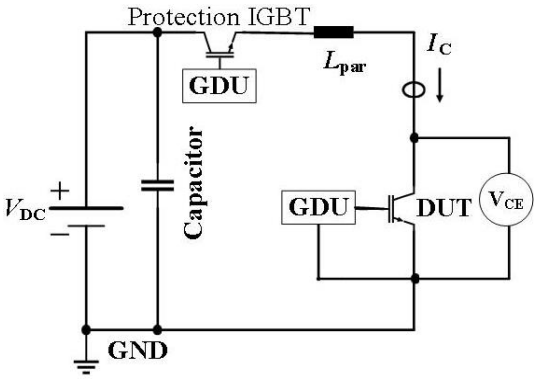


Fig. 1: Schematic of a SC type-1 measurement setup.

A schematic measurement setup used to measure the short-circuit of an IGBT is shown in Fig. 1. The protection IGBT and the device under test (DUT) were connected in series close to the DC-link capacitors to reduce the parasitic inductance of the SC path. A parasitic inductance L_{par} of the whole SC was 30 nH. The protection IGBT was used to limit the failure current in case of a DUT failure at the level of the SC current of the protection IGBT. Two gate drive units (GDU) were used to control the gate voltages V_{GE} of the DUT and the protection IGBT.

MEASUREMENT OF THE DESTRUCTIVE BOUNDARY LINE FOR 650 V IGBT

Before explicating the repetitive SC measurements, the destruction boundary limit of the 50 A - 650 V IGBTs was measured for two different temperatures (Fig. 2). For fixed V_{CE} = V_{DC}, the destruction current limit was measured by increasing the V_{GE} in steps of 0.25 V.
The critical collector current I_C as a function of V_{CE} of the last non-destructive SC type-1 pulse is plotted at

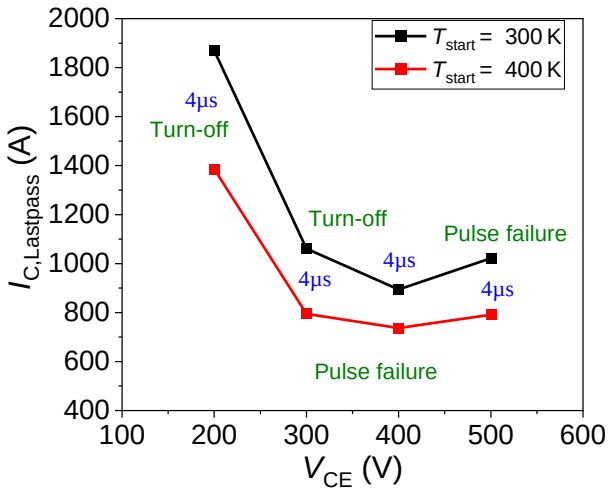


Fig. 2: Measured destruction limit of 650 V IGBTs far above the datasheet SC-SOA with measurement conditions L_{par} = 30 nH, $R_{G,ON}$ = 150 Ω, $R_{G,OFF}$ = 270 Ω.

300 K and 400 K in Fig. 2. An SC pulse width of 4 µs was set for all the last passed collector current measurements. For both temperatures, the minima of the destructive line occur at 400 V. In Fig. 2, the decrease in SC robustness far above the SC-SOA from 200 V to 400 V is due to the higher energy dissipation. Above 400 V, the SC capability increases due to the homogenous current distribution in the IGBT as the space-charge region covers the whole drift region with higher applied voltage and higher collector current [7]. For DC-link voltages of 200 V and 300 V, the destruction of the IGBT occurred during the SC turn-off, and for 400 V and 500 V during the SC pulse. A similar failure type occurs at higher temperatures. However, there is a significant reduction in the SC robustness of the IGBT device.

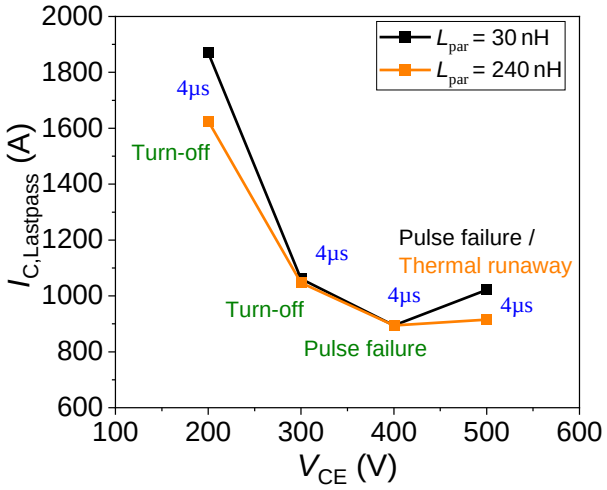


Fig. 3: Measured destruction limit of 650 V IGBTs for different parasitic inductances with measurement conditions $R_{G,ON}$ = 150 Ω, $R_{G,OFF}$ = 270 Ω, T_{start} = 300 K.

The parasitic inductance (L_{par}) is one of the important parameters under SC stress. The SC behavior of the IGBT can vary depending on $L_{par.}$ For two different parasitic inductances, the critical SC collector current of the IGBT is plotted in Fig. 3. For higher L_{par} measurements, the failure types are similar to lower parasitic inductance, except at 500 V. The reduced collector current at 200 V can be explained due to an increased SC turn-off voltage peak, which is shown and compared in Fig. 4(a) and (b). For a DC-link voltage 200 V and higher L_{par}, the maximum voltage during SC turn-off increases to 418 V compared to 234 V for lower L_{par}. Apparently, the turn-off peak voltage induced by the parasitic inductance L_{par} worsens the situation, so that the IGBT mostly fails during turn-off for lower DC-link voltages. For the non-destructive, last passed pulse, the critical energy will be higher for 240 nH in comparison to 30 nH. At higher L_{par}, the critical energy decreases with critical SC current showing that the turn-off overvoltage is an accelerating parameter [7]. Also, for higher parasitic inductance and at 500 V, the last passed collector current reduces due to a higher SC turn-off voltage peak. As this voltage peak is close to the rated

voltage of the device, thermal runaway of the device can occur.

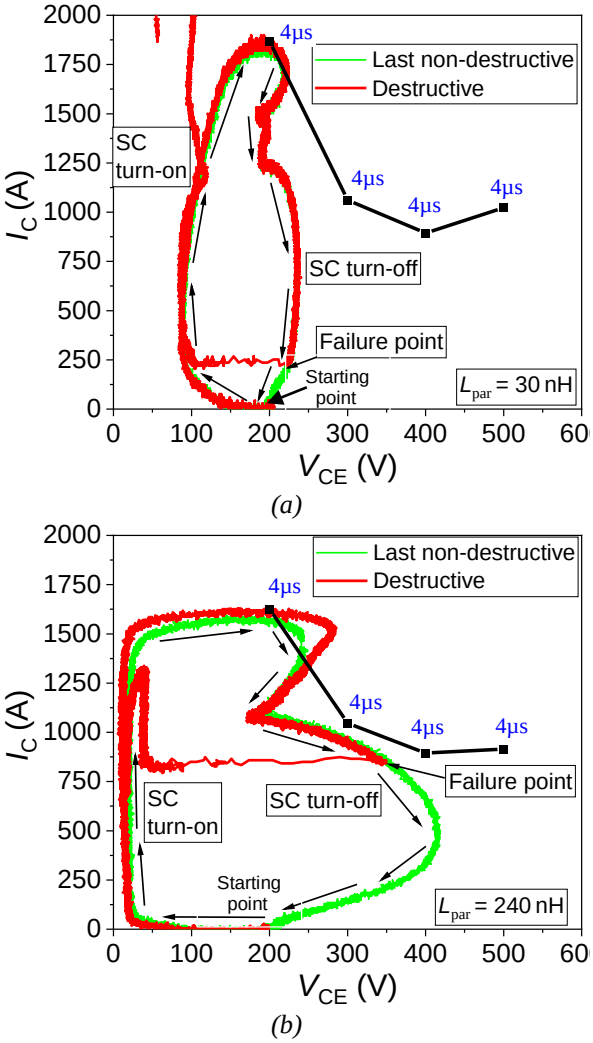


Fig. 4. SC in I_C-V_{CE} phase space diagram for last passed and destructive pulse at V_{DC} = 200 V, $R_{G,ON}$ = 150 Ω, $R_{G,OFF}$ = 270 Ω, T_{start} = 300 K. (a) L_{par} = 30 nH (b) L_{par} = 240 nH.

RESULTS OF REPETITIVE SHORT-CIRCUIT MEASUREMENTS

Fig. 5 displays an overview of the repetitive SC measurements carried out within the I_C-V_{CE} phase space. The black squares show the critical collector current as a function of V_{CE} of the last non-destructive SC pulse for the case that only single SC pulses were applied and the gate-emitter voltage was gradually increased until destruction occurred.

The scattered points in Fig. 5 indicate the operating conditions of the investigated IGBTs under repetitive SC events. The IGBT chips measured close to the destruction boundary line were able to survive few tens to hundreds of repetitive SC pulses. The devices which were destroyed during the repetitive SC pulses are marked with red squares along with the number of SC pulses survived. The blue stars represent the working samples after several hundreds or thousands of SC pulses away from the destructive boundary line.

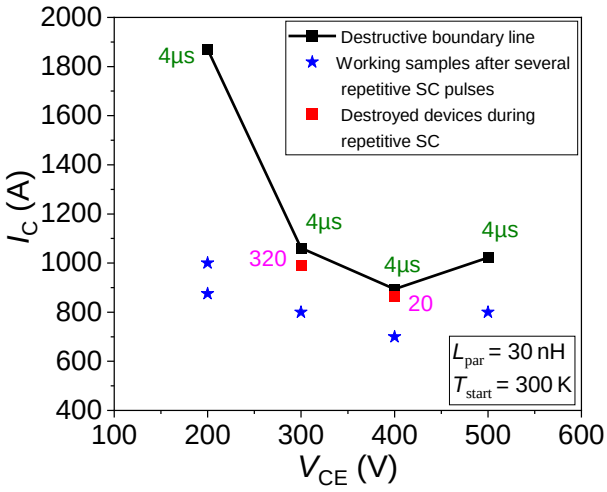


Fig. 5: Critical SC current of the last non-destructive pulse of a 650 V IGBT (black line), and test points for repetitive SC measurement in I_C-V_{CE} phase space (scattered points).

In order to observe the aluminium modification on the emitter metallization for defined conditions, the repetitive SC measurements were interrupted after a certain number of pulses. The optical microscope is used to observe the change in emitter-surface metallization. This technique can be used without additional effort on the measurement setup, and gives information about the Al modification. However, this method does not give any information about the temperature on the top-side metallization. This approach provides indirect information about the current distribution during SC. An initial picture of the top side of the unstressed IGBT was taken using an optical microscope before starting the repetitive SC events. For the defined measurement condition at a constant gate-emitter voltage (V_{GE}) and collector-emitter voltage (V_{CE}), the repetitive SC event was interrupted after a certain number of SC pulses, for example, 500 pulses, to take another picture of the top-side Al metallization. Afterwards, the next set of SC pulses was applied, and the measurements were repeated for several thousand SC pulses.

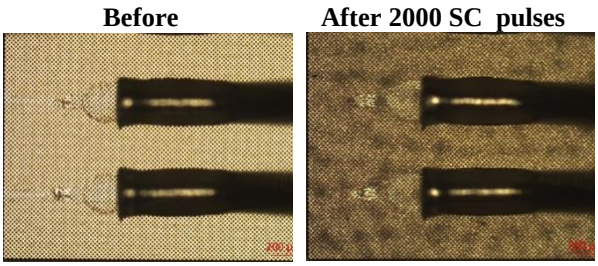
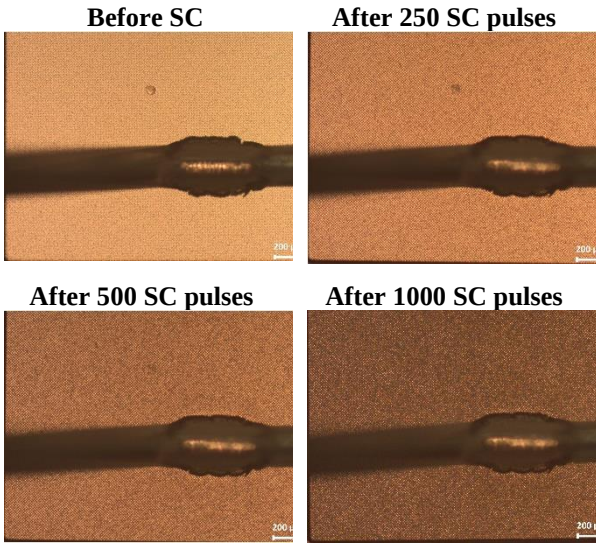


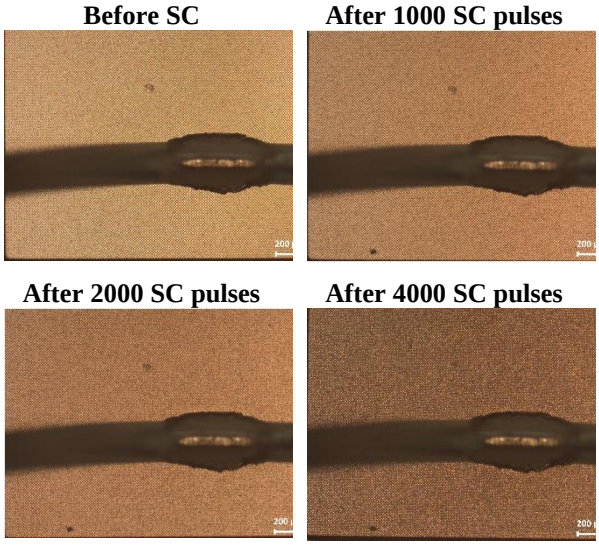
Fig. 6: Aluminium emitter surface analysis using optical microscope for a 1200 V IGBT at V_{DC} = 300 V, V_{GE} = 40 V, I_C = 300 A, t_{SC} = 4 µs, t_{gap} = 1 s, R_G = 220 Ω, $R_{G,OFF}$ = 270 Ω, and L_{par} = 45 nH [10].

The Al modification occurs during repetitive SC events due to a certain temperature swing [14]. When the device is subjected to the repetitive SC event, and if sufficient

temperature swing is generated due to the dissipated energy, the grain structures of the Al metallization modify. However, this process needs a certain amount of repetitive cycles as e.g. shown in Fig. 6. The 1200 V IGBT shows a clearly inhomogeneous aluminium modification as an indicator of current filaments as shown in Fig. 6 at DC-link voltage of 300 V [10].



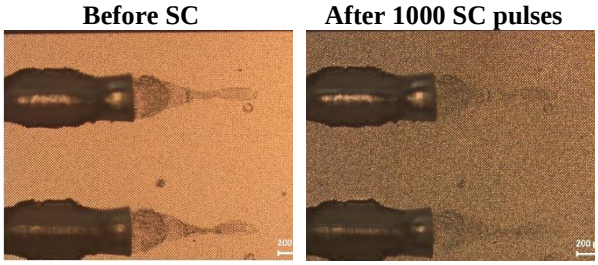
(a) V_{DC} = 200 V, V_{GE} = 25 V, I_C = 1000 A, t_{SC} = 4 µs, t_{gap} = 1 s, $R_{G,ON}$ = 150 Ω, $R_{G,OFF}$ = 270 Ω, and L_{par} = 30 nH



(b) V_{DC} = 200 V, V_{GE} = 25 V, I_C = 1000 A, t_{SC} = 2 µs, t_{gap} = 1 s, $R_{G,ON}$ = 150 Ω, $R_{G,OFF}$ = 270 Ω, and L_{par} = 30 nH

Fig. 7: Aluminium surface of a 650 V IGBT before and after series of SC pulses using optical microscope for different SC pulse width for given SC conditions (a) t_{SC} = 4 µs (b) t_{SC} = 2 µs.

The results in Fig. 7 show the Al modification compared for two different SC pulse widths for the same SC conditions. For t_{SC} = 4 µs, the 650 V IGBT shows a homogenous Al modification after 500 repetitive SC pulses. The change in temperature during the SC (ΔT_{SC}) will be higher for the 650 V IGBTs, compared to HV IGBTs, due to the smaller drift region [16]. Hence, the SC pulse width was halved to reduce the overall energy deposition during the SC and to make possible current filaments more visible in the metal imprint. Even though the SC pulse width was reduced to 2 µs during repetitive SC events in order to reduce the overall temperature influence on the emitter surface, no distinct metal-color change was visible. However, for t_{SC} = 2 µs, a higher number of repetitive SC events was required to modify the Al uniformly compared to the 4 µs pulse width. Furthermore, the collector current was reduced from 1000 A to 875 A for a SC pulse length of 4 µs in Fig. 8. The emitter metallization shows still a homogenous modification of Al after 1000 SC pulses.



V_{DC} = 200 V, V_{GE} = 22.8 V, I_C = 875 A, t_{SC} = 4 µs, t_{gap} = 1 s, $R_{G,ON}$ = 150 Ω, $R_{G,OFF}$ = 270 Ω, and L_{par} = 30 nH

Fig. 8: Aluminium surface of a 650 V IGBT before and after series of SC pulses using an optical microscope with reduced collector current at V_{DC} = 200 V.

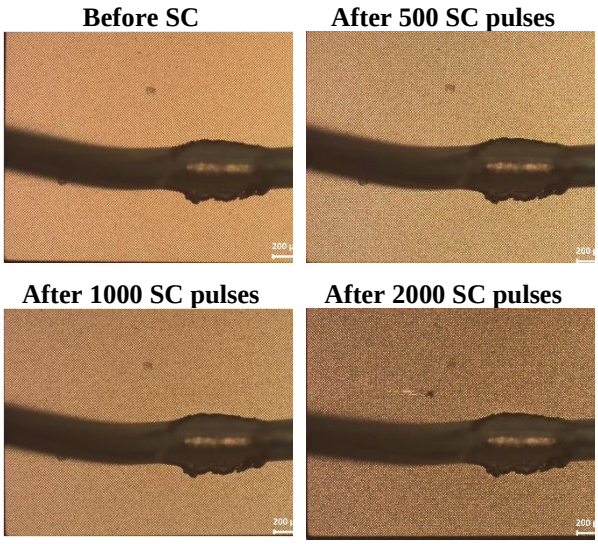
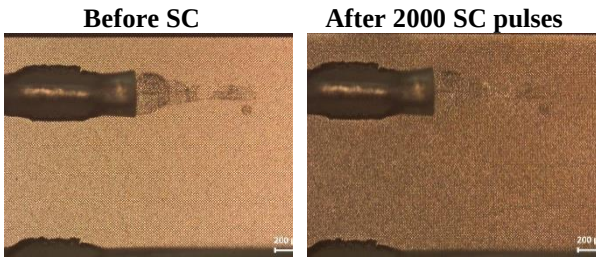


Fig. 9. Aluminium surface analysis of a 650 V IGBT using an optical microscope before and after series of SC pulses at V_{DC} = 300 V, V_{GE} = 20.8 V, I_C = 800 A, t_{SC} = 2 µs, t_{gap} = 1 s, $R_{G,ON}$ = 150 Ω, $R_{G,OFF}$ = 270 Ω, and L_{par} = 30 nH.

Fig. 9 exhibits the Al modification at 300 V and a collector current of 800 A. Here, a similar pattern to the repetitive measurements carried out at DC-link voltage of 200 V can be observed. The whole emitter metallization changes into a darker color with an increased number of SC pulses.

For both DC-link voltages at 200 V and 300 V, no clear local or inhomogeneous Al modifications for 650 V IGBTs were observable in contrast to the high-voltage class IGBTs (e.g., Fig. 6 in [9-11]). As 650 V IGBTs have a smaller base width, the high temperature from the back-side can reach the emitter

surface during a SC event with higher values. The temperature is more homogenous and higher throughout the emitter surface. These reasons can lead to a homogenous Al modification on the emitter side in 650 V IGBTs.



V_{DC} = 400 V, V_{GE} = 19.5 V, I_C = 700 A, t_{SC} = 2 µs, t_{gap} = 1 s, $R_{G,ON}$ = 150 Ω, $R_{G,OFF}$ = 270 Ω, L_{par} = 30 nH

Fig. 10: Aluminium surface of a 650 V IGBT chip at V_{DC} = 400 V and V_{GE} = 19.5 V.

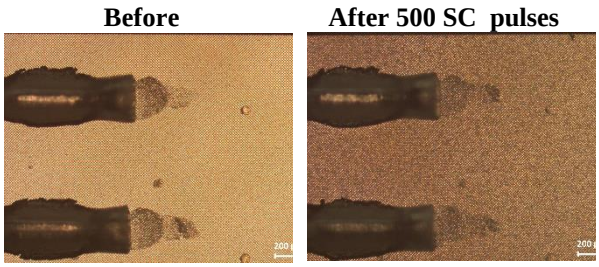


Fig. 11: Aluminium surface of a 650 V IGBT chip after a few hundred SC pulses at V_{DC} = 500 V and V_{GE} = 21 V.

Fig. 10 shows the Al modification development at V_{DC} = 400 V and V_{GE} = 19.5 V during 2000 SC pulses. The Al modification became stronger, and is distributed evenly after 2000 SC pulses. The SC duration was set to 2 µs for each pulse. Fig. 11 exhibits a similar Al modification after several hundred repetitive SC pulses at V_{DC} = 500 V and V_{GE} = 21 V. In both cases, a uniform Al surface modification appeared. The homogenous Al modification at 400 V and 500 V is in accordance with high-voltage class IGBTs under repetitive SC measurements [9-11].

ELECTRO-THERMAL SHORT-CIRCUIT SIMULATION RESULTS

In this section, electro-thermal SC simulations are shown for 650 V and 1200 V IGBTs using Sentaurus TCAD. This simulation result helps to understand the reason for homogenous Al modification irrespective of DC-link voltages for 650 V IGBTs. The device simulation was carried out to study the current filament formation and to estimate the surface temperature during a SC pulse with current filaments in the chip. A simplified front-side IGBT structure was used to investigate the current filament behavior under different V_{DC} and I_C conditions [6]. This IGBT structure is 200 µm wide. A simple time-dependent SC current pulse was simulated with a 300 K starting temperature (T_{start}), L_{par} =30 nH and with a constant DC-link voltage. For the SC simulation, the Phillip's unified mobility model, University of Bologna avalanche model, Shockley-Read-Hall (SRH) and Auger recombination models and Slotboom model for effective intrinsic density were utilized. For the SC simulation, self-heating was considered with a thermal boundary condition at the drain contact and a thermal resistance of 3.22 K/W. For simulation at 1200 V IGBT structure in [9], the SC pulse width was set to 4 µs, which was also used for this paper. However, the pulse width was reduced to 2.5 µs for 650 V IGBT during SC simulation in order to reduce the deposited energy during the SC.

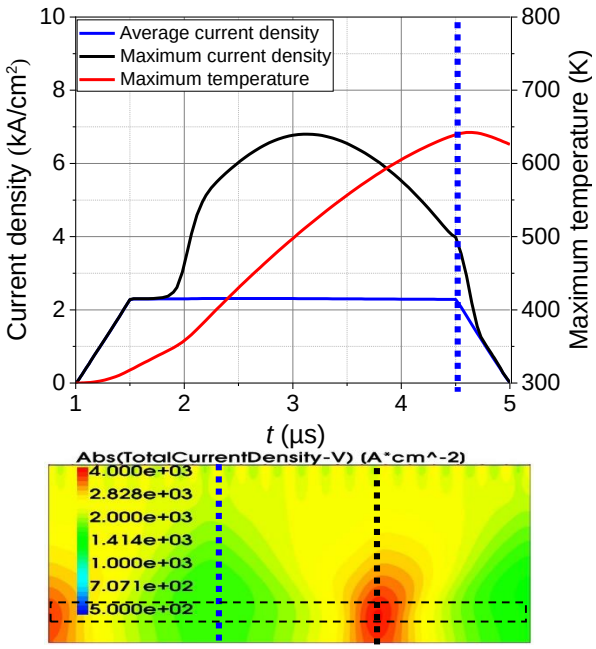


Fig. 12: (Top) Transients of the maximum and the average current density and the transient of the maximum temperature from electro-thermal short-circuit simulation at V_{DC} = 400 V, I_C = 235 A, T_{start} = 300 K (Bottom) current density distribution at 4.5 µs for 1200 V IGBT.

For 1200 V IGBTs, a clear local Al modification under repetitive SC stress using microscopy has been observed as shown in Fig. 6, and explained through simulation in [9,10]. The SC simulation was performed for 1200 V IGBT class at V_{DC} = 400 V, I_C = 235 A, T_{start} = 300 K and SC pulse length (t_{SC}) of 4 µs. In Fig. 12, the top picture shows the transients of the average and maximum current densities and the transient of the maximum temperature during the SC event for the above mentioned SC condition. The rise time and fall time was set to 0.5 µs. The bottom picture in Fig. 12 shows the absolute total current density in the IGBT at 4.5 µs. The average and maximum current densities were extracted from a window near the *n*-base/*n*-field-stop junction. The maximum temperature was extracted from the whole silicon region. At 1.8 µs, the average and maximum current densities start to split. The current flow becomes inhomogeneous. The slope of the maximum temperature transient increases slightly after 2 µs. For the simulated structure of 200 µm, there are one and a half current filaments at 4.5 µs during SC as shown in bottom Fig. 12. The edge-to-edge lateral distance between the current filaments is 110 µm.

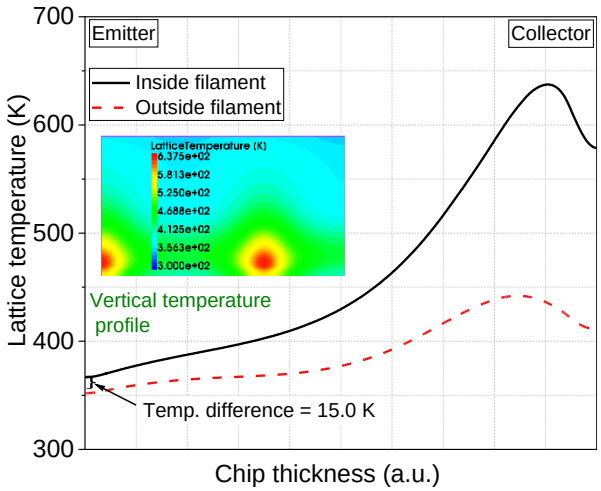


Fig. 13: Lattice temperature distribution in a 1200 V IGBT during SC simulation at V_{DC} = 400 V, I_C = 235 A, T_{start} = 300 K at 4.5 µs, for cuts ref. to Fig. 12 (bottom). Inset: IGBT lattice temperature distribution at 4.5µs.

The lattice temperature distribution of the 1200 V IGBT during SC simulation at 4.5 µs is shown in Fig. 13. The positions of the vertical cross sections are inside and outside the current filament and marked in Fig. 12 (bottom). The temperature reaches a maximum value of 630 K inside the current filament, and a value of 490 K outside the current filament at the collector side. The temperature at the emitter-side reduces as the temperature propagates from back-side to front-side. The temperature at the emitter surface above the filament area shows a value of 366 K, which is 15 K higher than the emitter surface above the non-filament area as shown in Fig. 13.

The short-circuit simulations were carried out for 650 V IGBTs with t_{SC} of 2.5 µs. In Fig. 14 (top) the picture shows the transients of the average current density, maximum current density and maximum temperature during the SC event at V_{DC} = 200 V, I_C = 1500 A, and T_{start} = 300 K. The average and maximum current densities were extracted from the window shown in the current density distribution bottom picture in Fig. 14. As soon as the average and the maximum current density start to split at 2.75 µs, the current flow becomes inhomogeneous. The current distribution at time point 3.1 µs is depicted in the bottom picture in Fig. 14. There are four and a half current filaments for the 200 µm simulated structure. These filaments have an edge-to-edge lateral distance of 30 µm ± 6 µm. Hence, there are more current filaments for 650 V IGBTs in comparison to 1200 V IGBT (see Fig. 12) for the given area. Furthermore, the increase in simulated SC pulse width leads to higher homogenous distribution at the emitter side.

Fig. 15 shows a vertical cross section of the absolute value of the electric-field strength, electron density and hole density in the IGBT structure at time point 3.1 µs.

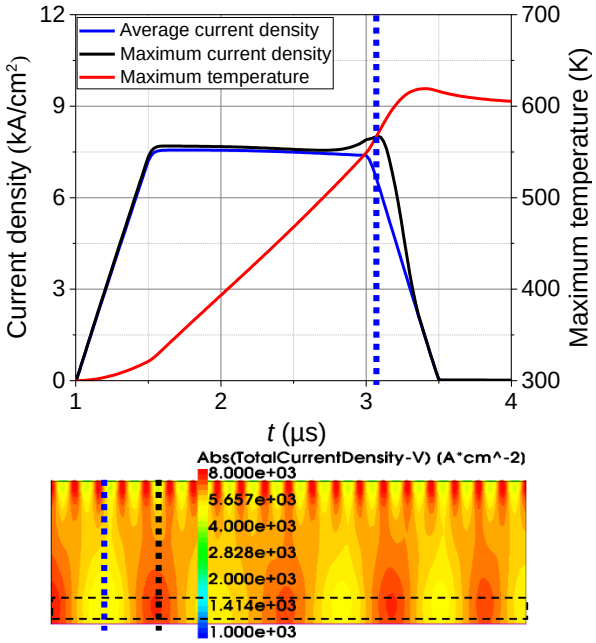


Fig. 14: (Top) Transients of the maximum and the average current density and the transient of the maximum temperature from electro-thermal short-circuit simulation at V_{DC} = 200 V, I_C = 1500 A and T_{start} = 300 K (Bottom) current density distribution at 3.10 µs for 650 V IGBT.

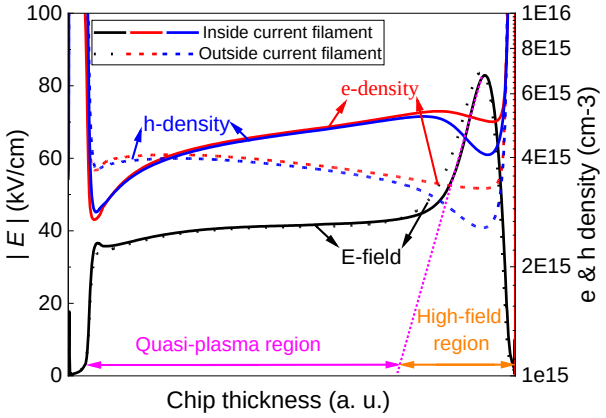


Fig. 15: Absolute value of the electric-field strength, electron and hole density distribution in IGBTs during SC simulation at V_{DC} = 200 V, I_C = 1500 A, T_{start} = 300 K at 3.1 µs, vertical cuts marked in Fig. 14 (bottom).

The positions of the vertical cross sections are marked inside and outside the current filament in Fig. 14 (bottom). For 650 V IGBTs, the electric field strength remains approximately the same inside and outside the current filament. However, the electron and hole density varies in the filament and non-filament area. As the current constricts in the current filament, the electron and hole densities are two times higher in comparison to the outside filament cut. From the simulation, there is a correlation between the lateral distance between the filaments and the width of the quasi-plasma region. The width of the high-field region defines the diameter of the current filament [11], see Fig. 14 (bottom). For 650 V IGBTs, the drift region is smaller, hence a smaller high-field region leads to a higher number of current filaments.

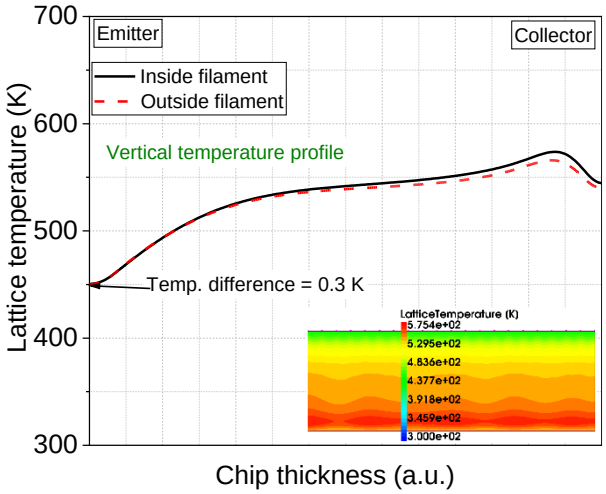


Fig. 16: Lattice temperature distribution in a 650 V IGBT during SC simulation at V_{DC} = 200 V, I_C = 1500 A, T_{start} = 300 K at 3.1 µs, for cuts ref. to Fig. 14 (bottom). Inset: IGBT lattice temperature distribution at 3.1µs.

For 650 V IGBT, the lattice temperature distribution inside and outside the filament area is plotted in Fig. 16 at 3.1 µs during the given SC conditions. At the collector side, the temperature difference between inside and outside filament is 10 K. The temperature at the emitter surface above the filament area is 450 K. The emitter surface temperature above the non-filament area is similar to the temperature found in the emitter region above the filament area. The temperature difference between these two emitter areas is 0.3 K. For 650 V IGBTs, the emitter surface temperature is very high and the difference in the emitter surface temperature between inside and outside filament position is approximately the same. This may be the reason for homogenous Al modification at 200 V DC-link.

In Fig. 17 (top) the picture shows the transients of the average current density, maximum current density and maximum temperature at V_{DC} = 300 V, I_C = 855 A during SC. Under these conditions, even weaker filaments are seen with slightly increased lateral spacing between two neighbouring filaments as shown in Fig. 17 (bottom). The average and maximum current densities were extracted from the window shown in the current density distribution bottom picture in Fig. 17. The maximum temperature during the SC is 565 K at 3.4 µs. For DC-link voltage of 300 V, the number of filaments has reduced to four in comparison to 200 V. The edge-to-edge lateral distance between current filaments is 35 µm ± 5 µm.

The vertical cross section of the absolute value of the electric-field strength, electron density and hole density in the IGBT structure at time point 3.0 µs for given SC conditions is shown in Fig. 18. The positions of the vertical cross sections are marked inside and outside the current filament in Fig. 17 (bottom). The electric field strength remains approximately the same inside and outside the current filament as shown in Fig. 18. The electron and hole density varies in the filament and non-filament areas.

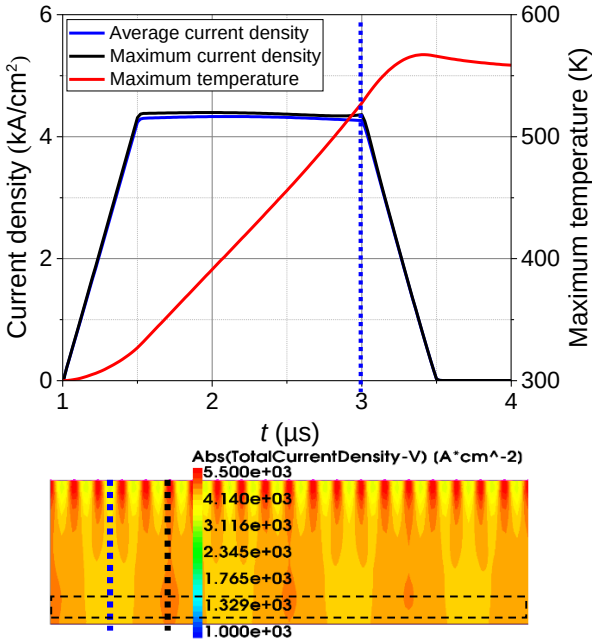


Fig. 17: (Top) Transients of the maximum and the average current density and the transient of the maximum temperature from electro-thermal short-circuit simulation at V_{DC} = 300 V, I_C = 855 A and T_{start} = 300 K (Bottom) current density distribution at 3.00 µs for a 650 V IGBT.

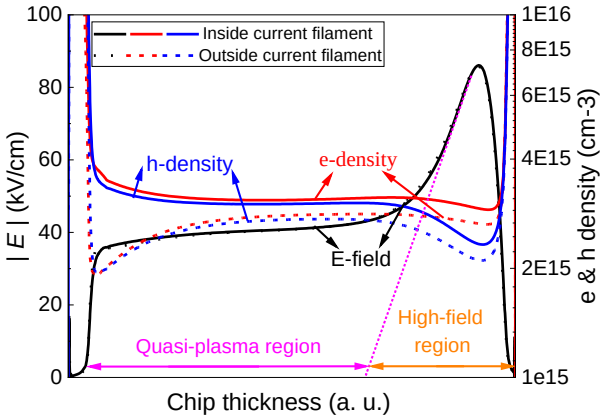


Fig. 18: Absolute value of the electric-field strength, electron and hole density distribution in a 650 V IGBT during SC simulation at V_{DC} = 300 V, I_C = 855 A, T_{start} = 300 K at 3.0 µs, vertical cuts marked in Fig. 17 (Bottom).

The temperature distribution inside and outside the filament region is approximately the same as shown in Fig. 19 for 650 V IGBT at 300 V DC-link voltage. A slightly lower temperature of 434 K is seen on the emitter surface in comparison to 200 V SC conditions.

The current distribution became homogeneous above 400 V. The SC simulation results at 500 V is exemplified in Fig. 20. The split in average and maximum current density was very small. The current flow is uniform throughout the device.

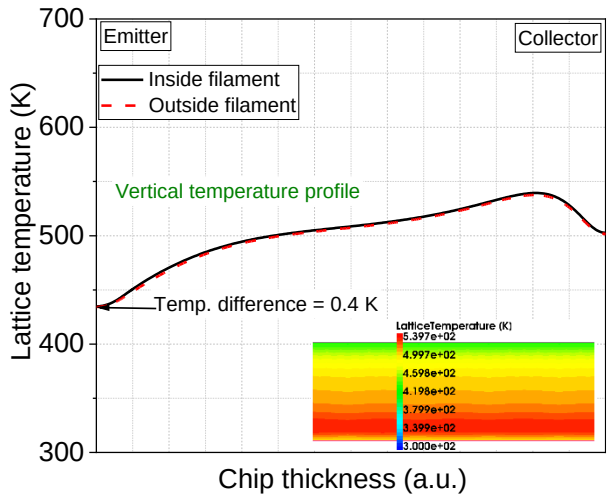


Fig. 19: Lattice temperature distribution in a 650 V IGBT during SC simulation at V_{DC} = 300 V, I_C = 855 A, T_{start} = 300 K at 3.0 µs, for cuts ref. to Fig. 17 (bottom). Inset: IGBT lattice temperature distribution at 3.0µs.

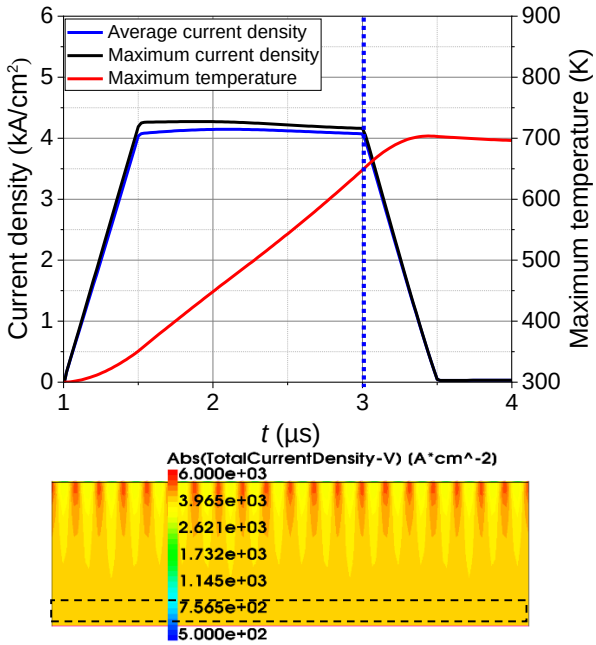


Fig. 20: (Top) Transients of the maximum and the average current density and the transient of the maximum temperature from electro-thermal short-circuit simulation at V_{DC} = 500 V, I_C = 820 A and T_{start} = 300 K (Bottom) current density distribution at 3.00 µs for a 650 V IGBT.

CONCLUSION

In 650 V IGBT short-circuit measurements, the dependence of the critical collector current as a function of DC-link voltage is similar to that of the high voltage IGBT class. As the DC-link voltage increases, the collector current decreases and increases after reaching a minimum. In repetitive SC measurements, homogenous Al modifications were observed at 200 V and 300 V DC-link voltage. Generally, the appearance of current filaments is expected at these DC-link voltages, which is supported by the performed electro-thermal SC simulations. Furthermore, the 650 V IGBT shows a higher amount of these current filaments during SC for the simulated structure width of 200 µm in comparison to the 1200 V IGBT structure due to the smaller quasi-plasma region. Even though the SC pulse width was reduced to 2.5 µs during the SC event, the 650 V IGBTs show a much higher emitter surface temperature in comparison to the 1200 V simulated IGBT due to the smaller base width. However, whereas the temperature difference at the emitter surface between the filament and non-filament region is 15 K for 1200 V IGBT, it is significantly smaller for a 650 V IGBT structure. This explains why the homogenous Al modification on the emitter metallization of 650 V IGBTs occurs although current filaments are present at the collector side.

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Study of 6.5 kV injection enhanced floating emitter (IEFE) IGBT switching behavior and its improved short-circuit robustness

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Abstract

In this work the improved short-circuit robustness of a new IGBT along with its switching behavior is investigated. The application of the recently proposed injection enhanced floating emitter (IEFE) concept to a 6.5 kV IGBT results in a higher hole current injection from the buried floating p-islands in front of the p-collector under short-circuit conditions. Hence, this concept provides a significantly improved short-circuit robustness compared to IGBT without p-islands and for the same design. The simulated results of the IEFE IGBTs depict the suppression of electrical current crowding at the collector-side without affecting the static and dynamic losses of the device.

Keywords: IGBT, short-circuit, current filaments, switching behavior, TCAD simulation.

INTRODUCTION

IGBTs are frequently used power semiconductor switches in the field of power electronics in a wide range of applications. One of the superior features of IGBTs is the ability to withstand both a high voltage and high current under short-circuit (SC) conditions for a certain time interval. The short-circuit safe operating area (SC-SOA) limit was investigated by many authors for IGBTs of different voltage classes from 1200 V to 6500 V [1-6]. The results in ref. [1,2,6] explain that the IGBT short-circuit destruction can be caused by the formation of current filaments at the collector side. In the experimental investigations, non-destructive current filaments in IGBTs operating under SC conditions were observed by using thermo-reflectance microscopy (TRM) [7]. In the experimental investigations, these current destructions occur far beyond the safe operating area (SOA) of the IGBT.

A new IEFE IGBT structure, which suppresses the formation of current filamentation at the collector side and offers improved SC robustness has been demonstrated for the 1200 V class with simplified IGBT structure by TCAD simulation [8].

The critical SC current for a conventional IGBT can be increased by increasing the *p*-emitter doping. But the increase in the *p*-emitter doping leads to an increase in the leakage current during static blocking and reduces the thermal robustness of the IGBT. Hence, the new IEFE IGBT with *p*-islands has been investigated for an improved SC robustness without compromising the thermal robustness of the IGBT and the dynamic losses of the device. In this work, a realistic front-side trench-gate 6.5 kV IGBT structure has been designed, and device simulations were carried out with Sentaurus TCAD. The static characteristics of the IEFE IGBT have been compared with a reference IGBT model along with the switching behavior to study the E_{off}-$V_{CE,sat}$ trade-off relationship. The switching behavior of the new IGBT structure has been investigated in detail at different parasitic inductances and for different nominal currents. Also, SC simulations have been performed on 6.5 kV IEFE IGBTs to demonstrate the improved SC capability in comparison to the reference IGBT structure.

IGBT STRUCTURES

Fig. 1(a) shows a reference trench-gate 6.5 kV IGBT structure with uniform field stop (FS) at the collector side. In the IEFE IGBT structure, the floating *p*-islands are implemented inside the field-stop area and in front of the *p*-emitter at the anode-side to amplify the hole injection from the backside as shown in Fig. 1(b). The reference IGBT and the IEFE IGBT structures have a similar front-side design, base doping, and field-stop profile.

The design and placement of the floating *p*-islands are optimized in such a way that the static and dynamic behavior of the IEFE IGBT is comparable to the reference IGBT. The floating *p*-amplification stage design and placement is kept constant throughout this paper and the simulation results are compared with reference IGBTs. For the IEFE structure, the doping of

the *p*-amplification stage is 1e18 cm^{-3} and the *p*-emitter is doped with 1e17 cm^{-3} as mentioned in [8]. These *p*-islands cover a certain lateral area at the collector-side and are separated from the *p*-emitter by an *n*-barrier layer. The *n*-barrier layer resistivity is selected in such a way that the electric field should not influence the breakdown voltage during static forward blocking of the IGBT.

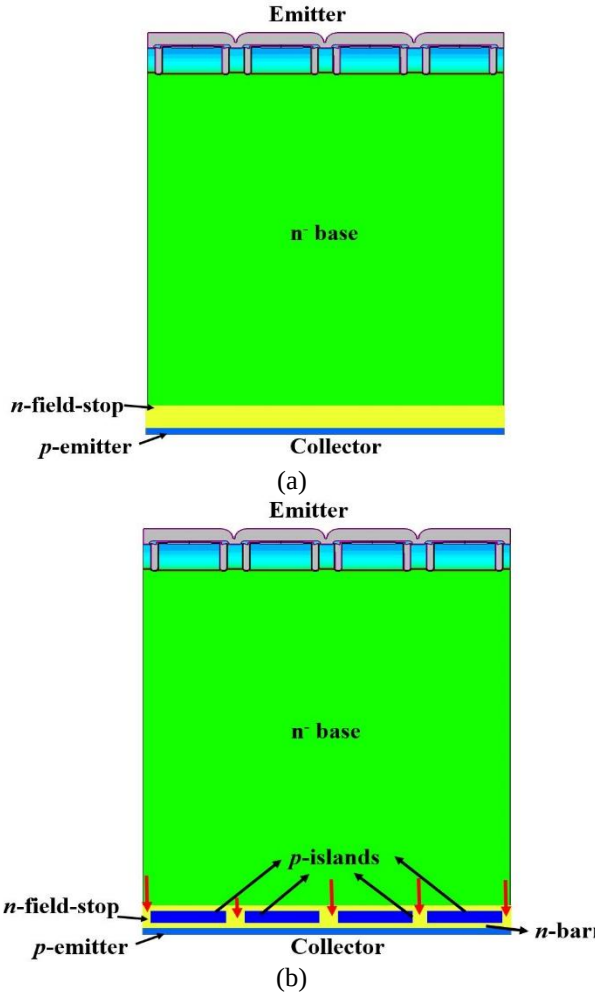


Fig. 1: Real front-side trench-gate 6.5 kV IGBT (a) reference structure without *p*-islands in front of the *p*-emitter, (b) IEFE IGBT structure with *p*-islands in front of the *p*-emitter.

The IEFE IGBT physics can be explained by means of the bipolar current gain (α_{pnp}) of the *pnp*-transistor in the IGBT. The α_{pnp} is a product of emitter injection efficiency (γ) and the transport factor (α_T). The control of α_{pnp} is strongly dependent on the emitter efficiency of the IGBT [9]. The ratio of the hole current density (j_p) to the total current density (j) at the collector side is defined as the emitter efficiency.

Hence, an enhanced hole density at the collector side due to the *p*-islands will lead to higher bipolar current gain for the IEFE structure in comparison to the reference IGBT. Thus, the critical field bending at the collector-side of the IGBT is more efficiently suppressed. Additionally, the IEFE IGBT shows two different emitter efficiencies at the collector-side. A more detailed IEFE IGBT physics explanation can be found in [8].

STATIC-CHARACTERISTICS - DEVICE SIMULATION

In this section, for the designed 6.5 kV IGBT structures, initially static characteristic simulations are described. The simulated IGBT structures have a rated current of 30 A. For these simulations, the Phillip's unified mobility model, University of Bologna avalanche model, Shockley-Read-Hall (SRH) and Auger recombination models and the Slotboom model for effective intrinsic density were utilized. The static characteristic simulations were isothermal. For the electro-thermal switching and SC simulations, self-heating was considered with a thermal boundary condition at the collector contact and a thermal resistance of 0.57 K/W.

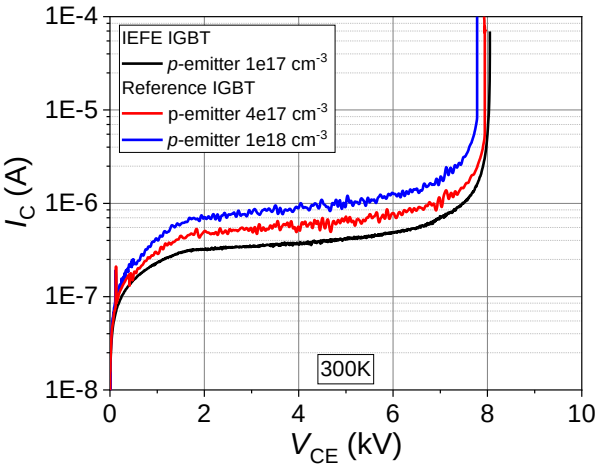


Fig. 2: Leakage current behavior for two different *p*-emitter doping concentrations in the reference IGBT structure (red and blue lines) and the IEFE IGBT (black) at 300 K.

The leakage current behavior during static blocking at 300 K is compared for the reference IGBT and the IEFE IGBT in Fig. 2. The increased leakage current and the decreased blocking voltage are clearly seen in the reference IGBT as the *p*-emitter doping is increased. However, the IEFE structure shows a slightly reduced leakage current and similar blocking voltage compared to the reference IGBT with *p*-emitter doping of 4e17 cm^{-3}.

During the blocking state, the IEFE IGBT shows a smaller leakage current even though the *p*-islands have a doping concentration of 1e18 cm^{-3}. The electric field is much lower across the *p*-islands in comparison to the emitter-side during blocking mode and the *p*-islands are embedded in the field-stop region. During the forward blocking state, the leakage current flows through the gap between the *p*-islands marked by red arrows in Fig. 1(b). Thus, the influence of the *p*-islands during the static blocking can be neglected.

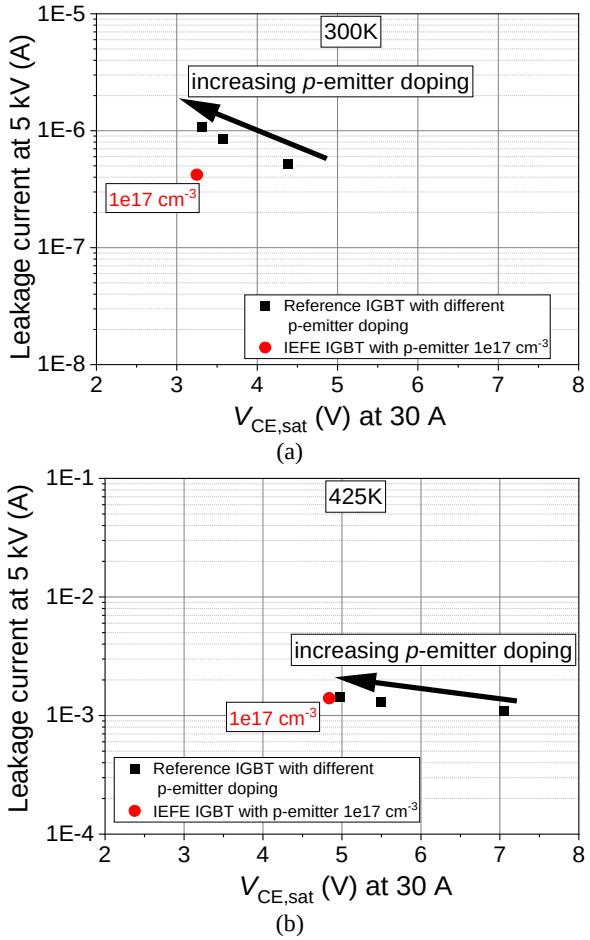


Fig. 3: Comparison of the leakage current at 5 kV as a function of $V_{CE,sat}$ between the reference IGBT with different *p*-emitter doping and the IEFE IGBT with *p*-emitter doping 1e17 cm^{-2} (a) 300 K (b) 425 K.

In Fig. 3, the leakage current has been plotted as a function of $V_{CE,sat}$ for the reference IGBTs with different *p*-emitter doping and the IEFE IGBT at 300 K and 425 K. For the reference IGBT structure, as the *p*-emitter doping increases, the increase in leakage current is more prominent at 300 K in comparison to 425 K. For the total leakage current at 425 K, the diffusion leakage current contribution is much higher than the space-charge region leakage current.

The $V_{CE,sat}$ of the reference IGBT strongly reduces with an increase in the *p*-emitter doping as the hole injection increases strongly from the collector-side and therefore the bipolar current gain of the IGBT increases accordingly. Even though the *p*-emitter doping of the IEFE structure is 1e17 cm^{-3}, the $V_{CE,sat}$ of the IEFE structure is comparable to that of reference IGBT with the highest *p*-emitter doping at 300 K and 425 K.

The IEFE structure with highly doped *p*-islands – located in the field-stop layer in front of the *p*-collector doping and separated by an *n*-barrier layer – offers an opportunity to reduce the collector-side *p*-emitter doping. Therefore, it is possible to attain a slightly lower leakage current [8].

DYNAMIC SWITCHING BEHAVIOR

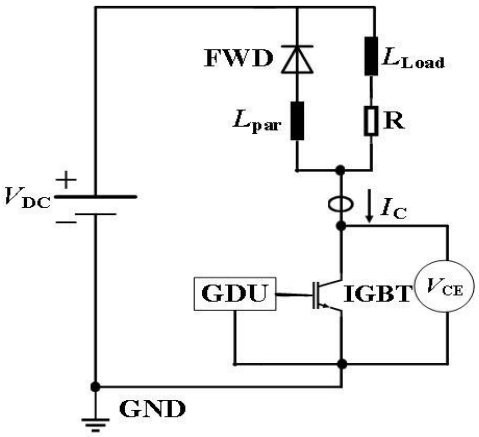


Fig. 4: Circuit for turn-off simulations.

A double-pulse setup with inductive load is used for the dynamic switching simulation (Fig. 4). The simulated IGBT can be controlled by the gate driver unit (GDU). The circuit consists of a parasitic inductance (L_{par}), a load inductance (L_{Load}), and a freewheeling diode (FWD).

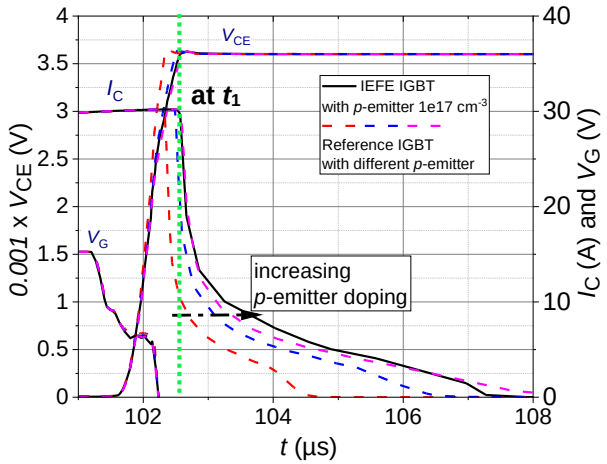


Fig. 5: Comparison of the turn-off behavior between the reference IGBT with different *p*-emitter doping concentrations and the IEFE IGBT. Simulation conditions: V_{DC} = 3600 V, I_C = 30 A, L_{Load} = 12 mH, V_{GE} = -15 V/+15 V, L_{Load} = 12 mH, L_{par} = 250 nH, $R_{G,ON}$ = 2 Ω, $R_{G,OFF}$ = 10 Ω, t_{pulse}= 100µs, T_{start} = 425 K.

The simulated turn-off behavior of the reference IGBT with different *p*-emitter doping and the IEFE IGBT are compared at 425 K in Fig. 5. The turn-off simulations are carried out using a circuit as shown in Fig. 4. For turn-off simulations, the collector current is turned off at a rated current of the IGBT by switching the V_{GE} from +15 V to -15 V. As the IGBT is turned off, the voltage increases to the applied DC-link voltage V_{DC} of 3600 V across the IGBT with a turn-off peak slightly higher than V_{DC} due to L_{par} in the circuit. The considered parasitic inductance of 250 nH is very small for a single chip, and hence a very small overvoltage is seen in Fig. 5. As the *p*-emitter doping increases for the reference IGBTs, the tail current in the IGBTs increases and dV_{CE}/dt decreases slightly.

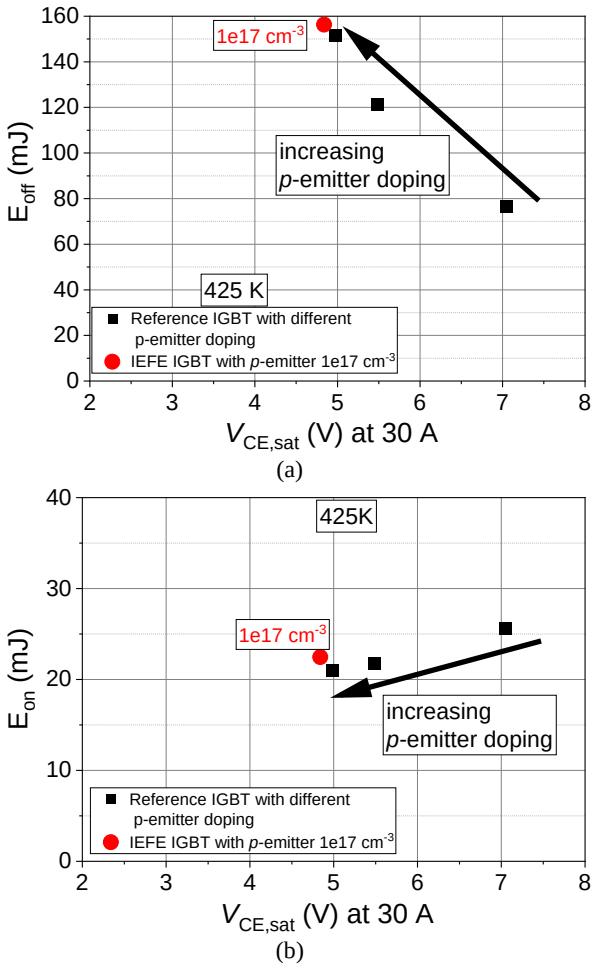


Fig. 6: Comparison of (a) turn-off losses (b) turn-on losses as a function of $V_{CE,sat}$ between the reference IGBT with different *p*-emitter doping concentrations and the IEFE IGBT using the same FWD. Simulation conditions: V_{DC} = 3600 V, V_{GE} = -15/+15 V, I_C = 30 A, L_{Load} = 12 mH, L_{par} = 250 nH, $R_{G,ON}$ = 2 Ω, $R_{G,OFF}$ = 10 Ω, t_{pulse}= 100µs, T_{start} = 425 K.

The turn-off behavior of the IEFE IGBT is comparable with the reference IGBT with the highest *p*-emitter doping as shown in Fig. 5.

For the simulated switching behavior at 425 K, the turn-off and turn-on losses are plotted as a function of $V_{CE,sat}$ for the IEFE IGBT and the reference IGBTs in Fig. 6. The IEFE IGBT shows slightly lower $V_{CE,sat}$ and moderately higher E_{off} losses compared to the reference IGBT with the highest *p*-emitter doping. However, the IEFE IGBT is on the same E_{off} - $V_{CE,sat}$ trade-off curve as the reference IGBT. The E_{on} losses of the IEFE IGBT are slightly higher in comparison to the reference IGBT with different *p*-emitter doping.

The electric field and charge carrier densities of the IEFE IGBT and the reference IGBT with the highest *p*-emitter doping are compared in Fig. 7 at time point t_1 from Fig. 5. The distributions of the electric field and the carrier densities are approximately the same for both simulated devices. This is valid in the plasma and the space-charge region.

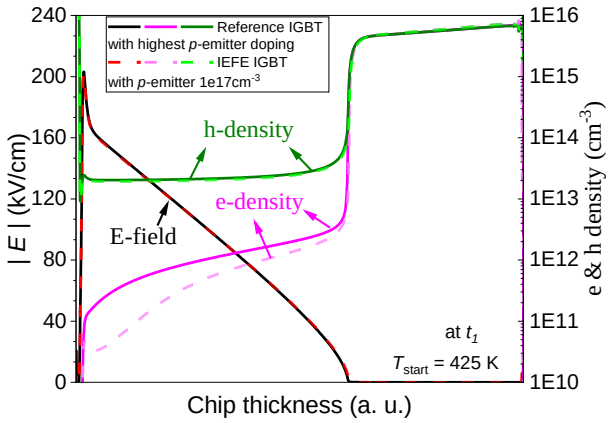


Fig. 7: Comparison of electric field and charge carrier densities between the reference IGBT with highest *p*-emitter doping and the IEFE IGBT at time point t_1 in Fig. 5 (green dotted line).

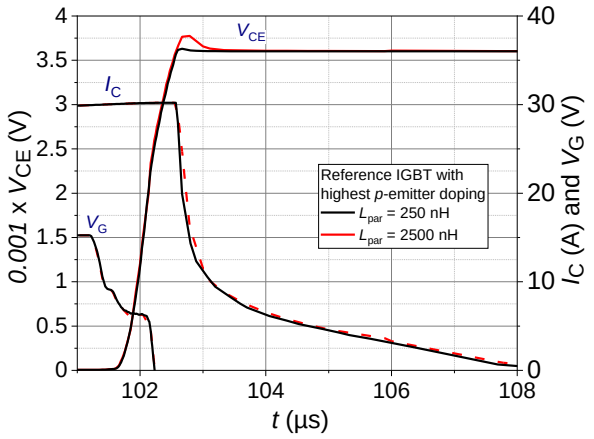
DYNAMIC SWITCHING BEHAVIOR UNDER HIGHER PARASITIC INDUCTANCES

One of the important parameters under switching is the parasitic inductance (L_{par}). Further turn-off simulations are performed for the reference IGBT and the IEFE IGBT with approximately similar E_{off} losses at two different parasitic inductances as shown in Fig. 8. Both IGBTs show a higher turn-off V_{CE} peak at higher parasitic inductance. The dV_{CE}/dt remains approximately the same even at higher L_{par} for both IGBTs. The IEFE and the reference structure turn-off tail current behavior is approximately comparable to L_{par} = 250 nH even if the L_{par} is increased by 10 times.

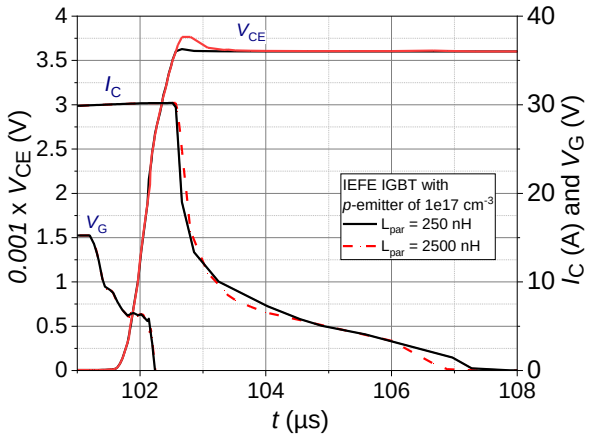
As displayed in Fig. 9, the turn-off behavior of the IEFE IGBT is compared at two different nominal currents at 425 K. The IEFE structure shows a longer tail current at 60 A compared to the rated current. At a higher nominal current, the IEFE IGBT shows a higher turn-off V_{CE} peak and lower dV_{CE}/dt after 2 kV in comparison to 30 A. The IEFE structure does not show any undesirable behavior at two times the rated current.

ELECTRO-THERMAL SC SIMULATIONS

In this section, electro-thermal SC device simulations are performed with a wider structure of 800 µm using a simplified front-side IGBT structure to reduce the simulation time [6]. Also, a wider structure of 800 µm makes possible to investigate the behavior of current filamentation. In order to study the enhanced SC capability of the IEFE IGBTs, the bipolar current gain of the simplified front-side IGBT structure was worsened for both the reference and IEFE IGBT structures. A simple time-dependent SC current pulse was simulated with a 300 K initial temperature (T_{start}) and with a constant DC-link voltage.



(a)



(b)

Fig. 8: Comparison of the turn-off behavior at different parasitic inductances of (a) the reference IGBT with highest *p*-emitter doping and of (b) the IEFE IGBT. Simulation conditions: V_{DC} = 3600 V, V_{GE} = -15/+15 V, I_C = 30 A, L_{Load} = 12 mH, $R_{G,ON}$ = 2 Ω, $R_{G,OFF}$ = 10 Ω, t_{pulse}= 100µs, T_{start} = 425 K.

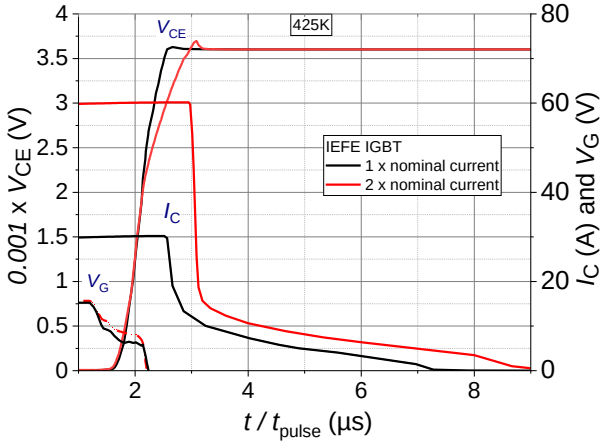
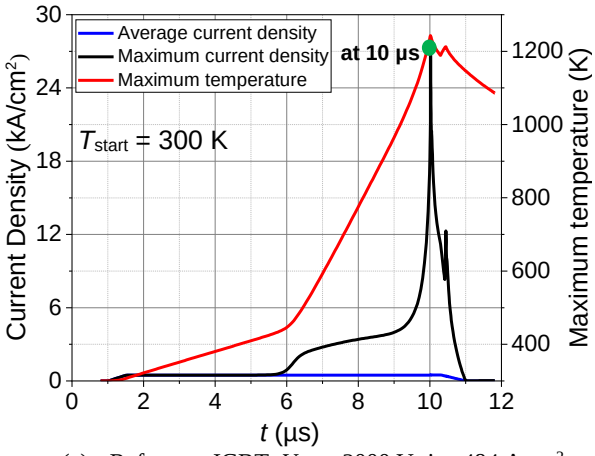
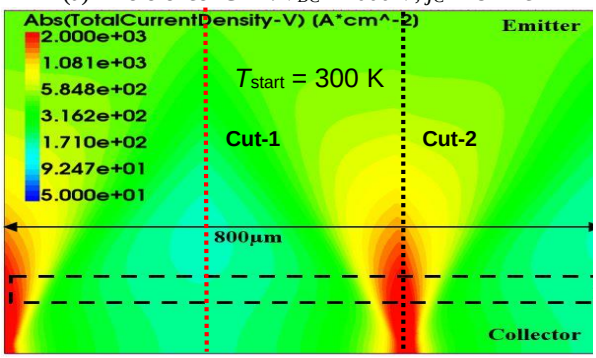


Fig. 9: Comparison of turn-off behavior at different nominal current for the IEFE IGBT. Simulation conditions: V_{CE} = 3600 V, V_{GE} = -15/+15 V, L_{Load} = 12 mH, L_{par} = 250 nH, $R_{G,ON}$ = 2 Ω, $R_{G,OFF}$ = 10 Ω, T_{start} = 425 K.



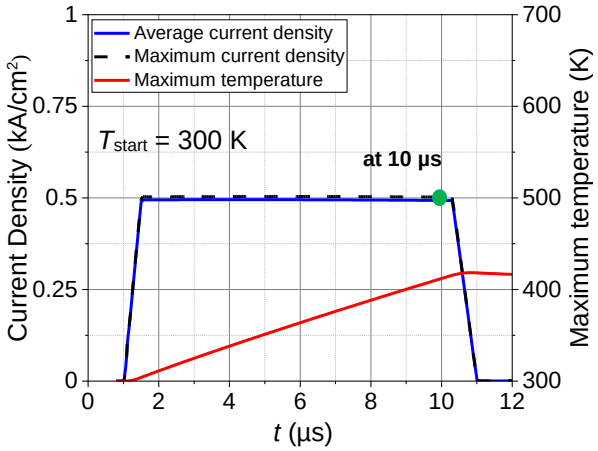
(a) Reference IGBT: V_{DC} = 2000 V, j_C= 484 Acm^{-2}



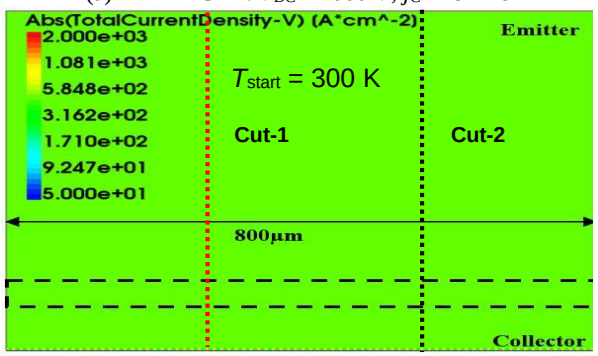
(b) without *p*-islands and V_{DC}= 2000 V at 10 µs

Fig. 10: (a) Transients of the average current density, maximum current density and maximum temperature under given SC conditions for a 6.5 kV reference IGBT (b) absolute total current density distribution at 10 µs.

Fig. 10 shows the transients of the average and maximum current densities and the time-dependent behavior of the maximum temperature during the SC event at V_{DC} = 2000 V, j_C = 484 Acm^{-2}, T_{start} = 300 K and SC pulse length (t_{SC}) of 10 µs for the reference IGBT. The rise time and fall time were set to 1 µs. The bottom picture in Fig. 10 shows the absolute value of the total current density distribution in IGBTs at the beginning of the SC turn-off process (10 µs) for the reference IGBTs. The average and maximum current densities were extracted from a window shown in the black dashed box in Fig. 10(b). The maximum temperature was extracted from the whole silicon region. At 5.8 µs, the average and maximum current density curves start to split in the reference IGBT. The current flow becomes more inhomogeneous throughout the structure. The slope of the maximum temperature transient increases rapidly after 6.0 µs and reaches a value of 1260 K at 10 µs inside the current filament of cut 2. At time point 10 µs, the IGBT device shows one and a half current filaments. The maximum current density is about 26 kA/cm^2 higher than the average current density. The simulated edge-to-edge filament lateral spacing is more than 450 µm. There is a correlation between the lateral distance between the current filaments and the width of the quasi-plasma region and the relationship between the width of the current filament and the width of the high-field region [10].



(a) IEFE IGBT: V_{DC} = 2000 V, j_C= 484 Acm^{-2}



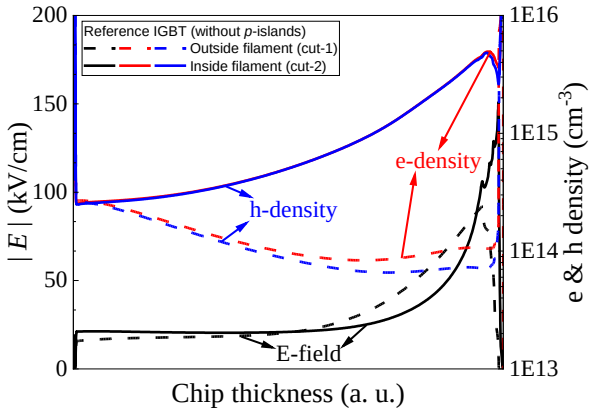
(b) with *p*-islands and V_{DC} = 2000 V at 10 µs

Fig. 11: (a) Transients of the average current density, maximum current density and maximum temperature under given SC conditions for a 6.5 kV IEFE IGBT (b) absolute total current density distribution at 10 µs.

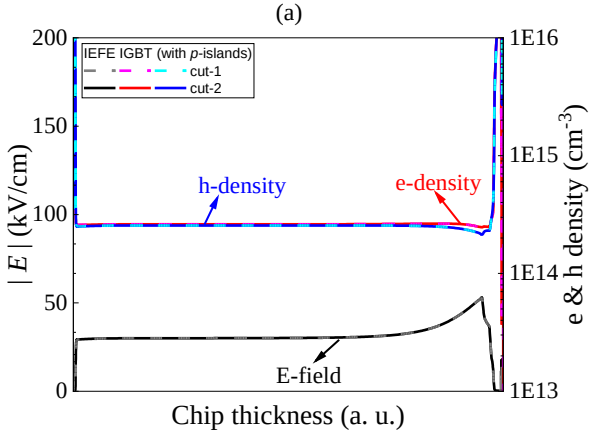
Fig. 11 depicts the transients of the average and maximum current densities and the transient of the maximum temperature during the SC event for the IEFE IGBT with SC conditions of V_{DC} = 2000 V, j_C = 484 Acm^{-2}, T_{start} = 300 K and SC pulse length (t_{SC}) of 10 µs. There is no split in the average and maximum current density curve [Fig. 11(a)] for the same SC conditions as for the reference. The average and maximum current densities were extracted from a window shown in the black dashed box in Fig. 11(b). The maximum temperature for the IEFE structure is 425 K at 10 µs, which is 835 K less than the reference structure with similar SC conditions. Also, the current distribution in the IEFE IGBT is homogenous in lateral direction in Fig. 11(b).

Fig. 12 shows a vertical cross-section of the absolute value of the electric-field strength, electron density and hole density in the reference and IEFE IGBT structures at 10 µs from two different cuts in Fig. 10(b) and Fig. 11(b) respectively.

For the reference IGBT, the shift of the electric field peak to the *n*-base/*n*-field-stop junction is due to the higher number of electrons than the number of holes at the collector-side of the base region. Due to the strong current filaments at 10 µs, the concentration of the quasi-plasma in the reference IGBT is higher inside the current filament than outside the filament [Fig. 12(a)]. The carrier concentration inside the current filament is roughly 50 times larger than outside the filament. There is an increase in the peak electric field at the filament positions. However, the current distribution for the structure with *p*-islands is uniform [Fig. 11(b)]. The electric-field of the IEFE IGBT at the collector-side is three times smaller in comparison to the reference IGBT (Fig. 12). Also, the electric field strength, electron and hole densities show a homogeneous lateral distribution in the device and overlap on each other for both cuts [Fig. 12(b)]. The main reason is the stronger hole injection from the back-side which partly compensates the negative charges in the front of the *p*-emitter.



(a)



(b)

Fig. 12: Absolute value of the electric-field strength, electron and hole density distribution in IGBTs during SC at V_{DC} = 2000 V, j_C = 484 Acm^{-2}, T_{int} = 300 K at 10 µs (a) reference IGBT (b) IEFE IGBT. For the cuts ref. to Fig. 10 and Fig. 11.

SC FILAMENTATION CRITERION

In order to estimate the short-circuit current which provokes strong filamentation and early destruction in the 6.5 kV reference and the IEFE IGBT, a simple simulation procedure is used from [2]. A transfer characteristic of 6.5 kV IGBT structure is simulated for a particular V_{CE}. During the V_{GE} ramp, the ratio in Eq. (1) is considered [11].

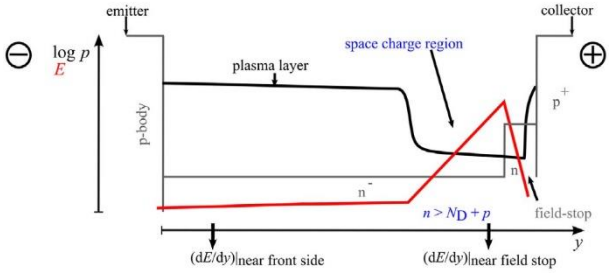


Fig. 13: Schematic representation of the hole density (black) and the electric-field strength (red) during the SC event in IGBT at high current [2].

$$c \cong \frac{(\mathrm{d}E/\mathrm{d}y)|_{\text{near field stop}}}{(\mathrm{d}E/\mathrm{d}y)|_{\text{near front side}}} = 2 \qquad (1)$$

where $(\mathrm{d}E/\mathrm{d}y)|_{\text{near field stop}}$ is the field gradient close to the field-stop junction and $(\mathrm{d}E/\mathrm{d}y)|_{\text{near front side}}$ represents the field gradient close to the emitter-side MOS structure of a short-circuit operation point. If the ratio of the two slopes is close to 1, the whole base region is covered with the space-charge region. Hence, there is no quasi-plasma layer and thus it is an uncritical condition. However, when c is higher than 1, the formation of current filaments is possible due to the bigger quasi-plasma layer [11].

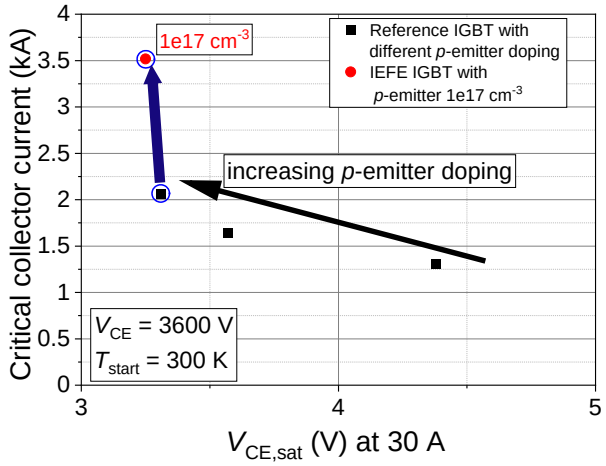


Fig. 14: Comparison of the critical collector current as a function $V_{CE,sat}$ between the reference IGBT with different *p*-emitter doping and the IEFE IGBT with *p*-emitter doping of 1e17 cm^{-3} at 3600 V and T_{start} = 300 K.

The simulated SC robustness of the reference 6.5 kV IGBT with different *p*-emitter doping is compared with the IEFE IGBT in Fig. 14 for a DC-link voltage of 3600V and at 300 K. The criterion from Eq. (1) is used to determine the formation of a current filament. The IEFE structure shows an improved SC robustness of 1.7 times the value of the reference IGBT with comparable $V_{CE,sat}$. Here, the leakage current of the IEFE structure is slightly lower in comparison to the reference IGBT with approximately similar $V_{CE,sat}$.

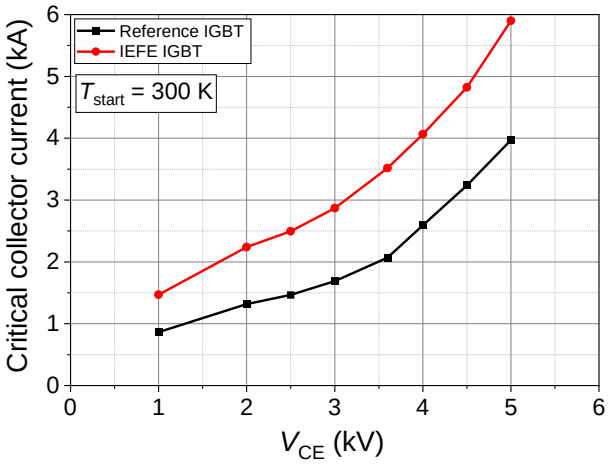


Fig. 15: Comparison of the critical collector current as a function of V_{CE} between the reference IGBT and the IEFE IGBT for approximately similar $V_{CE,sat}$. See Fig. 14 for the considered circle points.

The simulated critical collector current is plotted as a function of high V_{CE} for the reference IGBT and the IEFE IGBT with approximately similar $V_{CE,sat}$ in Fig. 15. As V_{CE} increases, the critical collector current increases. The IEFE structure exhibits higher SC robustness in comparison to the reference 6.5 kV IGBT due to the suppression of the current filaments. For both the simulated IGBT structures, the critical collector current at 1000 V and 2000 V could be much higher than the plotted values in Fig. 15. From the simple criterion used here, Eq. (1), the critical current is determined as soon as c reaches a value of 2. But due to the existence of non-destructive current filaments at 1000 V and 2000 V, the value of c shall be much higher than 2 [11]. Hence, the SC robustness can be expected to be much higher at 1000 V and 2000 V DC-link for both IGBTs [11].

CONCLUSION

The $V_{CE,sat}$ of the IEFE IGBT and the reference IGBT with highest *p*-emitter doping are comparable. The new IGBT structure shows a lower leakage current and the higher forward blocking voltage in comparison to the reference IGBT. The switching behavior is similar. Both IGBTs are on the same E_{off} - $V_{CE,sat}$ trade-off. Even for 10 times higher parasitic inductance and two times nominal current, the IEFE and reference structure does not show an undesired behavior during switching simulations. The SC capability of the 6.5 kV IEFE IGBT has been improved significantly, because the formation of the current crowding during SC can be suppressed to a high extent. This higher SC robustness is achieved without compromising the static and dynamic performance of the IGBT device.

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Experimental Comparison of a New SAG-IGBT and Conventional DAG-IGBT Structures with LTO Design in terms of Turn-on Performance

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Abstract

In this paper, we compare a new Single Active Gate Trench IGBT(SAG-IGBT) with the conventional Double Active Trench Gate IGBT (DAG-IGBT) structures with the LTO (LOCOS Trench Oxide) technology. Both structures have been fabricated with the same design rules and process platform and test chips compared in terms of their Eon performance. The new proposed SAG-IGBT is created by connected one of the active trench to emitter potential which effectively halves the gate capacitance C_{GE} and C_{GD}. It is also shown that the proposed SAG-IGBT can achieve a further 50% reduction in Q_{GC} than the conventional device due to only one trench being used for MOS channel conduction per unit cell. In addition it is shown that the SAG design can improve turn-on energy loss, $E_{ON,}$ by up to 25% for identical Vce(on), with no degradation in the SCSOA.

Keywords: IGBTs, Trench, LOCOS

INTRODUCTION

Nowadays, IGBT devices are key components in power conversion circuitry and primarily used in electric power and energy systems[1-3]. The new generation of IGBT devices are based on a significant increased cell density in conjunction with striped trench gate structures[4-5]. The paralleled trench cell layout consists of active and passive/dummy trenches, which enable smaller cell pitches as well as high controllability of turn-on dI/dt. This cell design allows higher carrier storage at the emitter side, which leads to a significant increase in conductivity modulation in the drift region. At present, improving operational efficiencies and reducing switching losses are the fundamental concerns for engineers using these devices. Moreover, it is also a design challenge to achieve lower E_{ON} due to the presence of significant capacitances (C_{GC} + C_{GE}) leading to high gate charge (Q_G).

The LOCOS Trench Oxide IGBT (LTO-IGBT) (Fig.1a) was presented in ISPSD and PCIM 2019 and shown to achieve 30% Q_G and C_{GC} (C_{RES}) enabling 25% increased current density with competitive E_{ON} and E_{OFF} performance [6-8]. This device is known as the DAGIGBT in this work. The new proposed SAG-IGBT is created by connected one of the active trench to emitter potential which effectively halves the gate capacitance C_{GE}. In this paper, we show that the proposed SAG -IGBT can achieve a further 50% reduction in Q_{GC} than the conventional device due to only one trench being used for MOS channel conduction per unit cell. In addition it is shown that the SAG design can improve turn-on energy loss, $E_{ON,}$ by up to 25% for identical Vce(on), with no degradation in the SCSOA and RBSOA. In summary, lower capacitances, lower gate charge and reduced E_{ON} makes the SAG device structure a very strong candidate for more efficient high voltage trench IGBT designs as well as low voltage devices for automotive applications and other low loss power systems [1-3].

THE SAG/DAG STRUCTURES and DESIGNS

In the proposed SAG-IGBT design, one of the active trenches is connected to ground or emitter metallization by the contact mask as shown in Fig.1b. Other contact schems can also be used in the third dimension. For the same cell pitch, decreasing the number of active trenches within the SAG-IGBT device reduces the conductivity modulation. This is because of reduced MOS channel density for the same device active area. As a consequence, fewer electrons are injected per unit area causing a reduction base current of the PNP transistor hence lower saturation current and Vce(sat) due to lower conductivity modulation.

So a major challenges to solve with the SAG-IGBT device design where only one effective active trench is used, is to achieve identical MOS channel density in

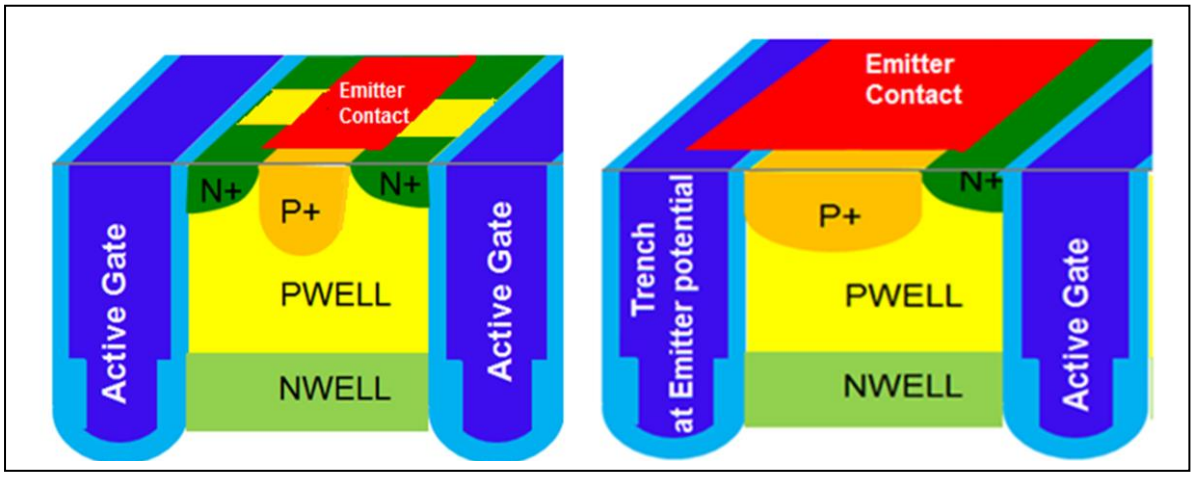

Fig. 1: The simplified top cell schematic of (a) DAG (Double Active Gate) structure with segmented N+/P in the emitter area (b) The SAG (Single-Active Gate) structure with continuous N+ along the single active gate trech

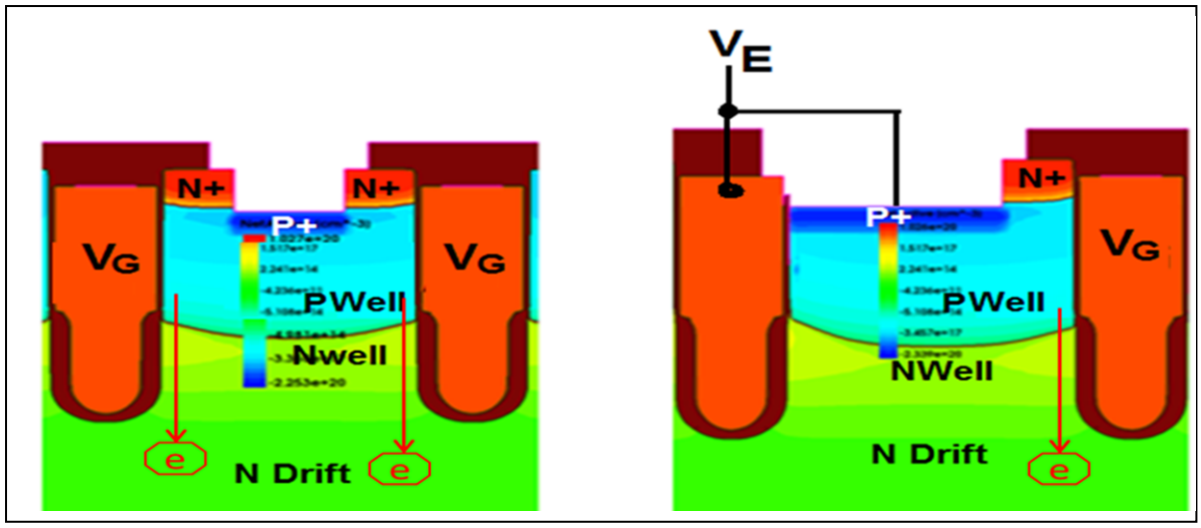

Fig. 2: Top cell of the simulated IGBT structures (a) DAG and (b) SAG device (only one trench is used for MOS channel conduction)

order to maintain Vce(sat), saturation current (I_{SAT}) and short-circuit current (I_{SC}). For identical Nwell(carrier stop layer) and threshold valtage Vth, two approaches are available: (i) reduce the cell pitch /width or (ii) increase emitter N+ area over the active gate trench. The later approach is used in this work which means the SAG device has continuous N+ along the active trench as shown in Fig.1b compared with segmented N+/P+ in the conventional DAG-IGBT device.

SIMULATION & EXPERIMENTAL RESULTS

As a first step, the design parameters of SAG-IGBT and conventional DAG-IGBT using the LOCOS Trench Oxide process [4-5] were studied numerically using Synopsys TCAD Simulator. Fig.2 shows the top cell of the two simulated device structures. These two structures were investigated using calibrated models in Synopsys TCAD tools. In 2D-simulation, the cell pitch/width of SAG-IGBT device is about a half-size of DAG-IGBT device. However, the effect of hole current on the channel inversion in DAG-IGBT/SAG-IGBT devices have also been considered but the study was limited to a 2D device model [9].

Fig.3 shows the simulated Q_G charateristics for DAG and SAG 6.5kV rated IGBT devices with the same simulation conditions. It is shown that the SAG-IGBT device can achieve at least 50% lower total gate charge Q_G and miller charge Q_{GC}. $V_{GE,TH}$ ($\sim 6V$) was matched in the both simulations. Lower miller charge and total gate charge improves the total switching losses (E_{ON} + E_{OFF}) of the device hence switching frequency and speed can be increased.

The simulation results comparing the input capacitance (C_{iss}), and reverse transfer capacitance (C_{res}) are shown in Fig.4. The simulation condition of the AC frequency was 100 kHz. It can be seen that the SAG device (black trace) has a 50% reduction in C_{iss} and C_{res} compared with the DAG device (red trace).

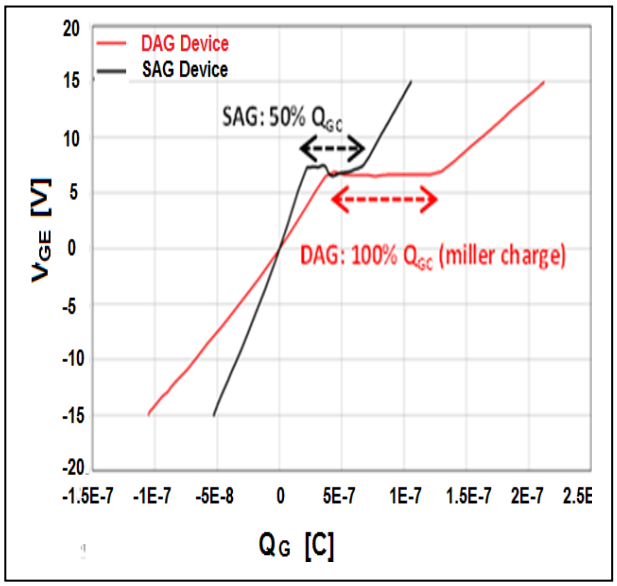

Fig. 3: Simulated gate charge (Q_G) for DAG and SAG 6.5kV rated IGBT devices [Vce=3.6kV, Ice=168A, Tj=25°C]

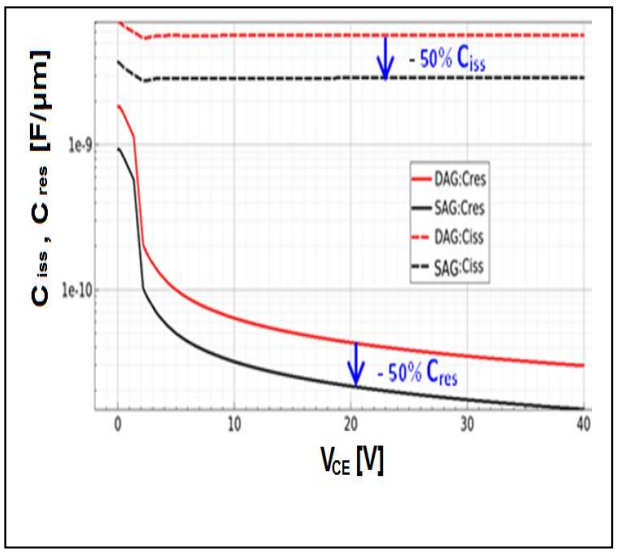

Fig. 4: Simulated C_{iss} and C_{res} of DAG and SAG devices for 6.5kV rated IGBT devices [Vge=0V, f=100 kHz, Tj=25°C]

Optimized engineering samples of both the SAG and DAG devices have been fabricated in silicon and electrical results are presented in this work. The SAG and DAG-IGBT devices are fabricated using the similar processes andthe chip size of 13.5mm x 13.5mm has been used

Fig.5 shows the image of the ceramic substrate, containing a parallel arrangement of 4 x IGBTs and 2x FRDs (Freewheeling Diodes) for testing. Each IGBT is a 6.5kV/42A rated SAG-LTO or DAG-LTO IGBT device which means total current per substrate is 168A.

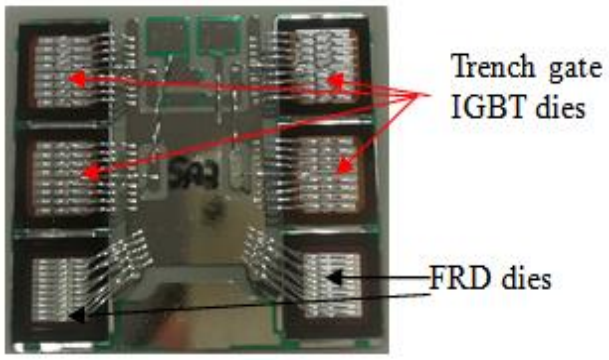

Fig.5: Image of a ceramic substrate, containing 4x trench gate IGBTs and 2x FRDs [rated voltage/current =6.5kV/168A]

Fig.6 shows the short-circuit Ice and Vce waveforms of SAG and DAG-IGBT at 125°C. It can be seen that both devices have a similar short circuit current level (i.e. Isc ~600A) due to matched MOS channel density a shown in fig.1. Therefore, the transconductance is also matched and we can compare E_{ON} and dI/dt of both structures using similar R_{GON} values.

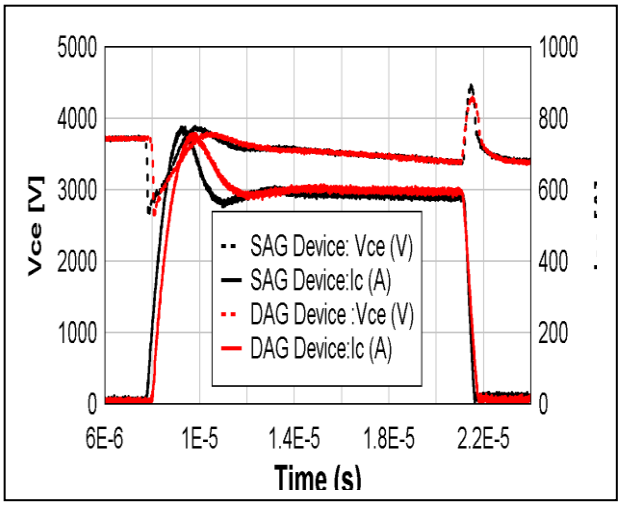

Fig. 6: Typical short circuit test Ice and Vce waveforms for 6.5kV DAG and SAG IGBT substrates. V_{CE}=3.6kV, T_J=125°C, V_{GE}=±15V. It can be seen that I_{SC} is well matched due to identical MOS channel density

Fig.7 shows the turn-on waveforms of SAG and DAG devices for identical R_{GON}/R_{GOFF} (16Ω/33Ω) values at T_J=125°C. It can be seen that reduced capacitance in the SAG structure especially C_{RES} results is faster turn-on in terms of shorter V_{CE} tail during turn-on which results in lower E_{ON}. In addition, reduced gate capacitance in the SAG structure results in small T_{don} values as shown in Fig.8.

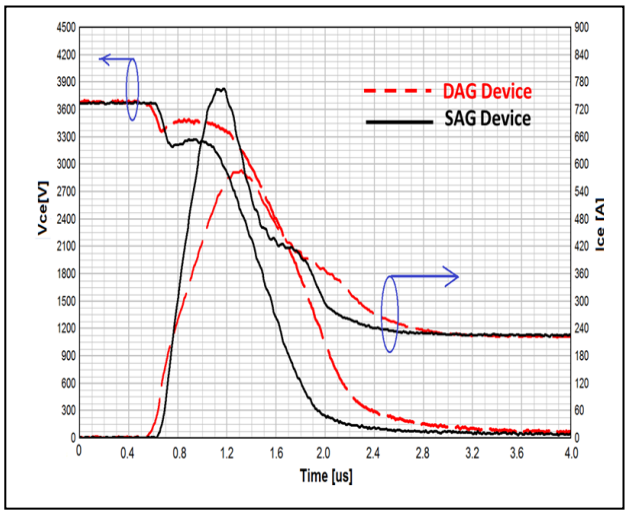

Fig. 7: Typical turn-on I_{CE} and V_{CE} waveforms for SAG and DAG 6.5kV IGBT devices for identical $R_{GON}/R_{G,OFF}$. [V_{CE}=3.6kV, I_{CE}~168A , T_J=125°C, V_{GE}=±15V]

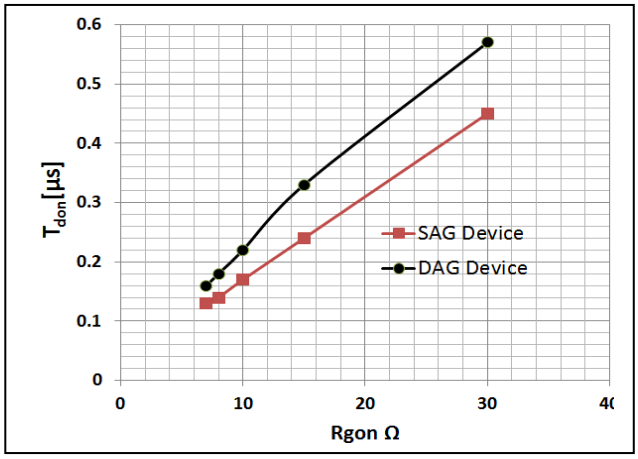

Fig.8: Typical influence of R_{GON} on Td_{on} for SAG and DAG 6.5kV IGBTs. [V_{CE}=3.6kV, I_{CE}~168A, T_J=125°C, V_{GE}=±15V]

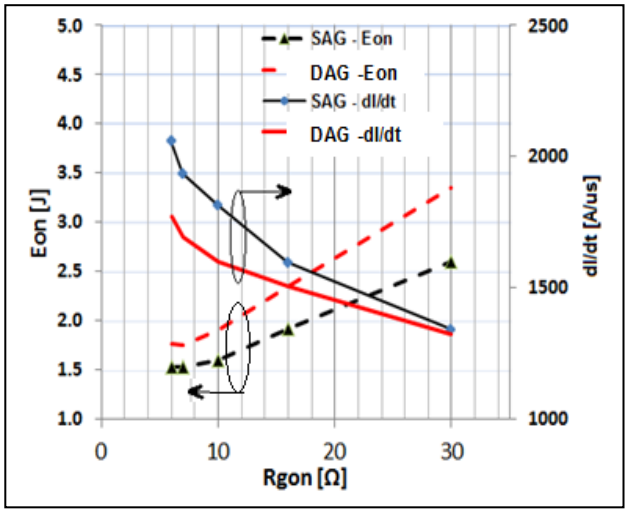

Fig. 9: Influence of R_{GON} on turn-on dI/dt for SAG and DAG 6.5kV IGBTs[V_{CE}=3.6kV, I_{CE}~168A , T_J=125°C, V_{GE}=±15V]

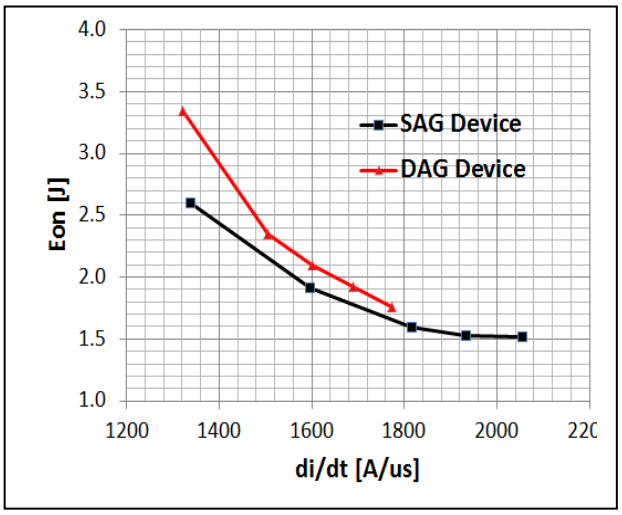

Fig. 10: Influence of turn-on dI/dt on E_{ON} for SAG and DAG 6.5kV IGBTs V_{CE}=3.6kV, I_{CE}~168A , T_J=125°C, V_{GE}=±15V]

Fig. 9 shows the influence of R_{GON} on Eon and dI/dt where it can be seen that both devices show good response to changing R_{GON}. In addition it can be seen that higher dI/dt and lower Eon is possible with SAG-IGBT compared to DAG-IGBT structure, for identical R_{GON}. Fig.10 shows that the SAG device structure can lower Eon by up to 25%. However, beyond dI/dt > 1600 A/µs the E_{ON} benefit of the SAG device becomes much less.

SWITCHING LOSSES COMPARISON OF SAG/DAG DEVICES

The benefit of this work can be summarized through Fig. 11, which shows the switching losses(E_{ON} + E_{OFF}) comparison of SAG and DAG devices under the same Vce(on) and dI/dt($\sim 1600 A/\mu s$) .

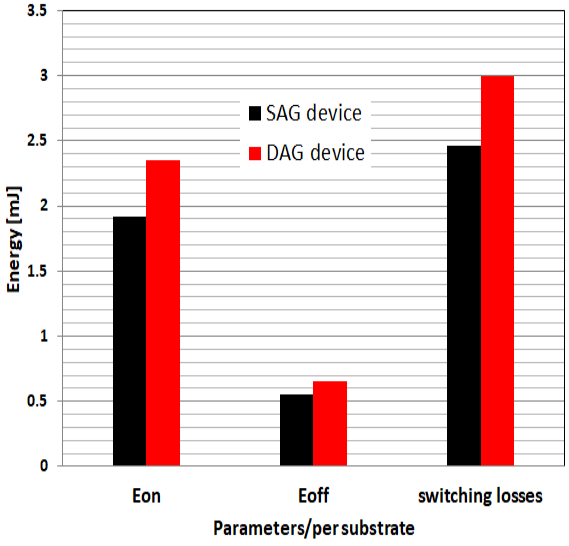

Fig. 11: Switching losses comparison of SAG and DAG devices under the same Vce(on) and dI/dt($\sim 1600 A/\mu s$)

The E_{OFF} performance of IGBT is a function of (i) the turn-off speed of the gate (increases with C_{GE}) which determines turn-off dI/dt, (ii) V_{CE} rise or dV/dt (how fast the depletion moves towards the collector side) which is determined by the plasma density and (iii), the tail current which is determined by carrier lifetime and silicon thickness (hence device rating).

The SAG device shows the 11% lower E_{OFF} than DAG with the same Vce(on) value. For identical Vce(on), the SAG design will speed up only (i) above hence the influence on E_{OFF} is relatively small compared to Eon.

CONCLUSION

In this work we have shown simulation and experimental results comparing 6.5kV SAG and DAG IGBT device concepts using the LOCOS IGBT Trench structures. The LOCOS IGBT concept has been previously shown to reduce Q_G. Herein, it has been shown that the SAG-IGBT concept can achieve a further reduction in Q_{GC} than the conventional device due to only one trench being used for MOS channel conduction per unit cell. In addition it is shown that the SAG design can improve turn-on energy loss, $E_{ON,}$ by up to 25% and Eoff by 11%, for identical Vce(on) and dI/dt, with no degradation in the SCSOA.

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High-Voltage IGBT turn-off at transition from overcurrent to desaturation

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Abstract

The turn-off capability of a power semiconductor is normally given by the datasheet with test conditions. The RBSOA (Reverse Bias Safe Operation Area) diagram limits the collector-emitter peak voltage and maximum turn-off current [1]. As mentioned in the early literature and many datasheets of IGBT power modules, the current which can be turned off is limited to twice the nominal current, in the between this and short circuit it is forbidden to turn off the device [2]. In this paper, the turn-off behaviour of HV-IGBTs at the transition from overcurrent to desaturation is investigated with a 2D half-cell model in Synopsys TCAD as well as with single chip measurements. This article focuses on the classification of the turn-off process near the V_{CE} desaturation, with respect to the plasma- and electric field distribution, dynamic avalanche, as well as electric field peaks which occur during this process. It shows that the IGBT can be operated in this former forbidden region successfully, and a beginning desaturation releases dynamic avalanche.

Keywords: Overcurrent, IGBT turn-off behaviour, RBSOA, desaturation, dynamic avalanche, TCAD.

1 Introduction

In this paper, the overcurrent turn-off is investigated for three situations according to the initial state of the device, see Fig. 1. Turn-off situation I locates the voltage saturation region. The turn-off current is normally limited to two or three times of nominal current according to the RBSOA of the datasheet for situation I. At high current, dynamic avalanche can happen. Nowadays IGBTs can bear significant dynamic avalanche.
When the turn-off current is further increased, the device is turned off at the channel pinch-off region, normally four to five times nominal current. In this situation II, the device is close to the intersection of the voltage saturation and desaturation region.

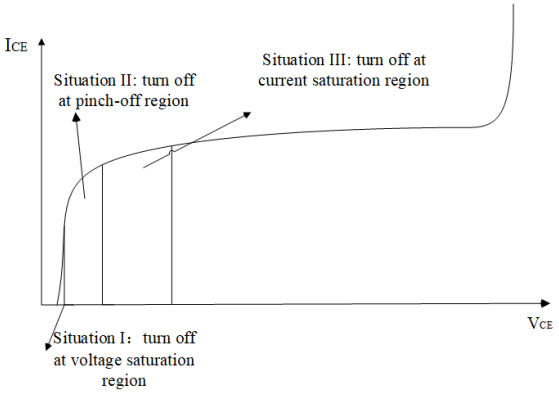

Fig. 1 Schematic diagram of different turn-off situations. Siutation II is forbidden for turn-off in [2]

In situation III, which locates close to the desaturation region, the initial value of the collector-emitter voltage V_{CE} is already much higher than the on-state voltage, the initial state of the device is similar to short circuit.
In the next chapters, these statements will be verified by experiments as well as TCAD simulation results.

2 Experimental results

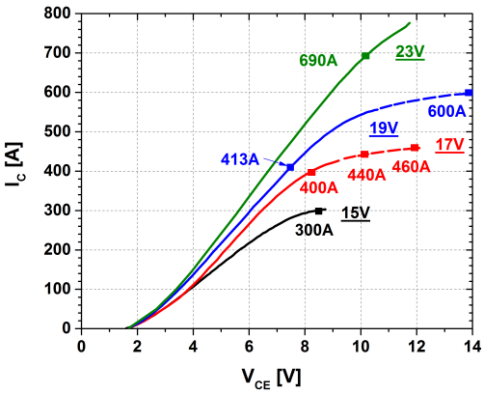

Fig. 2 Output characteristic of 4500 V IGBT, single chip. Points of turn-off measurements are marked. T = 25 °C

In the measurements, the device under test (DUT) is one single chip from a 4500 V press pack IGBT, rated for 50 A with a recommended gate emitter voltage V_{GE} 15 V. The output characteristic of this chip at room temperature at V_{GE} 15 V to 23 V is given in Fig. 2. At V_{GE} 15 V, the chip is in the voltage-saturated region up to 200 A (4 times rated current). With a further increased collector

current I_C, the device approaches towards the desaturation region, the collector emitter voltage V_{CE} increases significantly.

All following turn-off measurements are executed at T = 25 °C. The measurement circuit for the overcurrent turn-off behavior is given in Fig. 3. The circuit includes the DC link voltage V_{DC}, a protection IGBT SIGBT, a stray inductance L_{stray}, a freewheeling diode FWD, a load inductance L_{load} and the DUT. The device is first ramped up with the load inductance to a desired value, it can be controlled by the pulse length, and then the device is turned off. The pulse length has to be rather short to prevent self-heating, but also not too short to ensure that the charge carrier distribution is close to a stationary situation. The protection IGBT will switch off within some micro seconds once a short circuit is detected in the circuit.

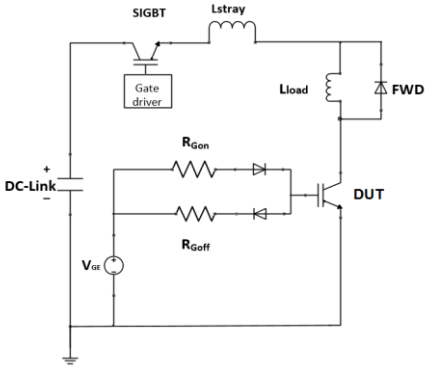

Fig. 3 Schematic diagram of measurement circuit

2.1 Turn-off as a single chip, medium L_{stray}

a) Turn-off with different R_{goff}.

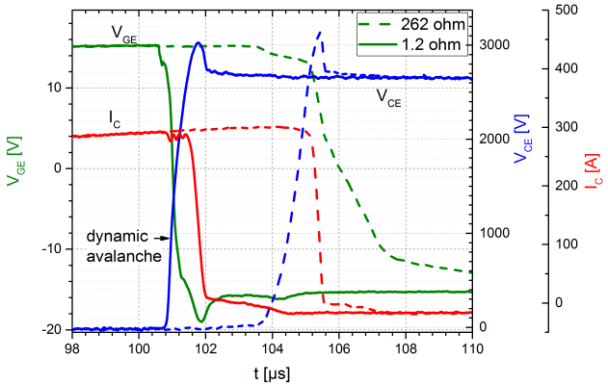

Fig. 4 Turn-off with different Rgoff, V_{GE} 15V

Test	1	2
V_{DC} [V]	2700	2700
I_{OFF} [A]	300	300
L_{stray} [nH]	430	430
L_{load} [µH]	1000	1000
t_{on} [µs]	100	100
R_{gon} [Ω]	1	1
R_{goff} [Ω]	**262**	**1.2**
V_{GE} [V]	-15/+15	-15/+15

Tab. 1 Test condition for turn-off with different R_{goff}, V_{GE} 15V

The measurements were first carried out with a medium L_{stray} of 430 nH with R_{goff} 262 Ω and 1.2 Ω at V_{GE} 15 V. The test conditions are given in Tab. 1. As shown in Fig. 4, after the gate voltage is switched to negative, the current continues to conduct until V_{CE} reaches the DC link value. The voltage peak of the single pulse measurement is determined by the stray inductance L_{stray} in the circuit multiplied by the slope of the current di_C/dt plus the turn-on voltage peak V_{FRM} of the diode. The changing of dv_{CE}/dt during the V_{CE} slope indicates the appearance of dynamic avalanche [3], but in this case it is only weakly pronounced. The device can be turned off at I_C 300 A near the desaturation region even with a very small gate resistance. As the gate resistance increases, the large gate resistance will slow down the discharge of the gate and keep the gate in the on-state for a longer time, so that more electrons are injected to compensate the holes which are injected from the collector side. In this case, a sign of dynamic avalanche by turn-off with 262 Ω is not observed. For 1.2 Ω, the IGBT is in the self-controlled region, which is determined by the plasma dynamics. The voltage peak is higher than the turn-off with a smaller R_{goff}.

b) Turn-off at different current, situation I, II, III

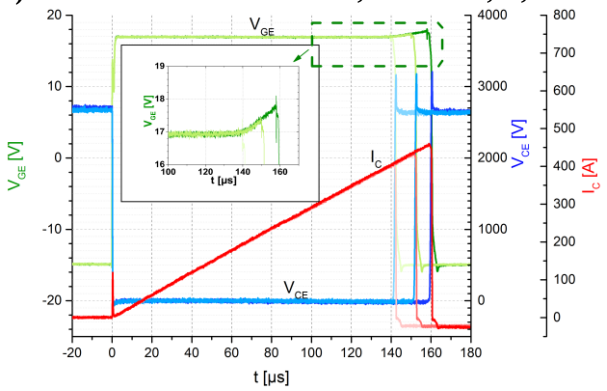

Fig. 5 Turn off at different current, situation I, II, III, V_{GE} 17 V

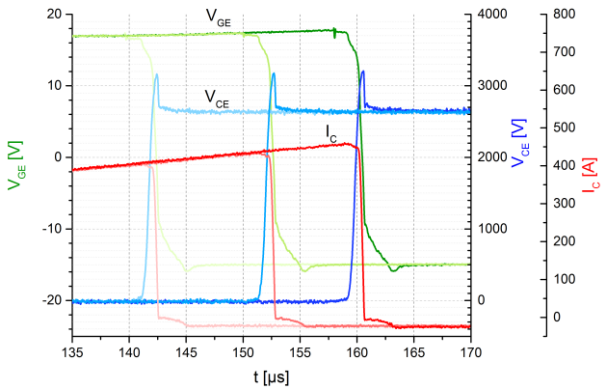

Fig. 6 From 140 µs to 170 µs of Fig. 5

Test	1	2	3
V_{DC} [V]	2700	2700	2700
I_{OFF} [A]	**400**	**440**	**460**
L_{stray} [nH]	430	430	430
L_{load} [µH]	1000	1000	1000
t_{on} [µs]	140	150	160

R_{gon} [Ω]	1	1	1
R_{goff} [Ω]	100	100	100
V_{GE} [V]	-15/+17	-15/+17	-15/+17

Tab. 2 Test condition for turn-off at different current, situation I, II, III

After the devices turned off under V_{GE} 15 V without destruction, the gate voltage was increased to 17 V, so as to achieve a higher turn-off current. In this set of measurements, as the test condition is given in Tab. 2, the device turned off at 400 A, 440 A and 460 A by changing the pulse length. The three turn-off points are also marked in Fig. 2. The initial state of turn-off at 400 A is located just before desaturation. By a further increased turn-off current at 440 A and 460 A, the device is turning off in the region of situation II. The measurement results show an increase of V_{GE} starting from 400 A, see Fig. 5 and Fig. 6. This is due to the increased V_{CE} directly at the beginning of the turn-off process caused by the early desaturation. The gate capacitance is charged further by a feedback across the C_{GE} (Miller feedback). In other words, the turn-off process starts directly at the Miller plateau. Since the current is still rising until the DC-link voltage is reached, also the Miller plateau voltage has to rise. The rise of V_{GE} is the indication that the turn-off initial condition starts entering the desaturation region, which marks the start of the turn-off situation II. To further verify this statement, two turn-off measurements with comparable current values and different gate voltages were carried out.

c) Turn-off at comparable current, different gate voltage.

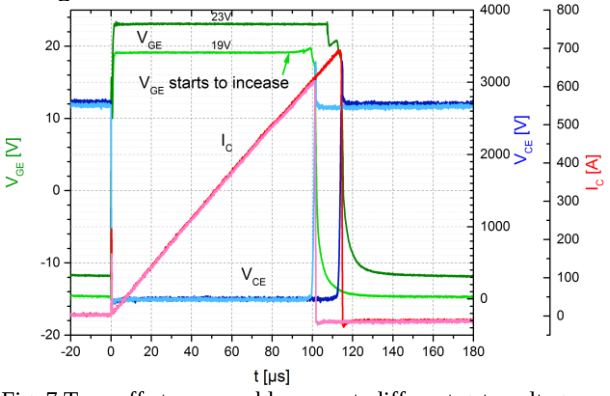

Fig. 7 Turn off at comparable current, different gate voltage

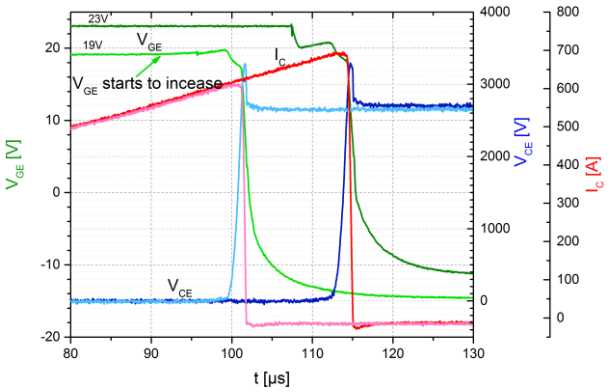

Fig. 8 From 80 µs to 130 µs of Fig. 7

Test	1	2
V_{DC} [V]	2700	2700
I_{OFF} [A]	**600**	**690**
L_{stray} [nH]	430	430
L_{load} [µH]	500	500
t_{on} [µs]	96	108
R_{gon} [Ω]	1	1
R_{goff} [Ω]	330	330
V_{GE} [V]	-15/+19	-12/+23

Tab. 3 Test condition for turn-off at comparable current, different gate voltage

As given in Tab. 3, the device was turned off at V_{GE} 19 V, 600 A, and V_{GE} 23 V, 690 A. From the output characteristic in Fig. 2, it is clear to see that for V_{GE} 19 V the initial state of the device before turning off is already in the region of situation II, however, this current value is still located in the region of situation I for V_{GE} 23 V, even at a higher current of 690 A. Fig. 7 and Fig. 8 show the turn-off behaviour for these two currents. For the measurement at V_{GE} 19 V, the gate voltage starts to increase before it starts the descent process. That means that the device is already in the desaturation region from the beginning of the turn-off process. Compared to the measurement at V_{GE} 23 V, no increase in the gate voltage is observed. This measurements proves the previous explanation.

2.2 Turn-off as a single chip with high L_{stray} and R_{goff}

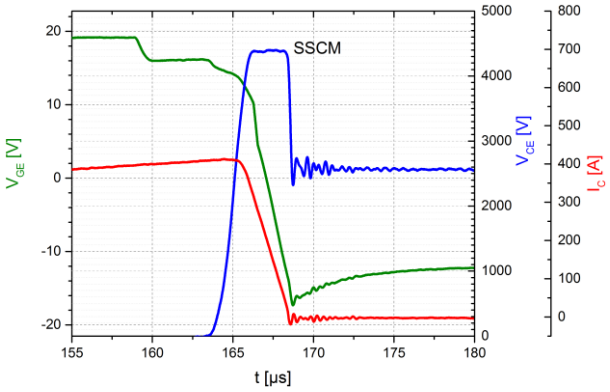

Fig. 9 Turn-off as a single chip with real-application scaled L_{stray} and R_{goff}

In order to achieve a comparable test condition to the measurement with press the pack IGBT, the stray inductance L_{stray} and the gate resistance R_{goff} were scaled according to the data sheet and the amount of chips. Due to the additional L_{stray}, the test condition becomes more critical, as the voltage peak is very close to the static breakdown voltage of 4500 V mentioned in the data sheet. This set of measurements first starts with a large gate resistance and gate voltage of 15 V to avoid too high di_C/dt and dv_{CE}/dt. Afterwards, the gate resistance is gradually reduced or the gate voltage is increased until the device is fails. The device can turn off at V_{GE} 15 V in the desaturation region with comparable test conditions as given in the data sheet. By further increasing the gate voltage and collector current, the chip failed. Fig. 9 and

Tab. 4 show the penultimate pulse before destruction and the corresponding test conditions.

Test	1
V_{DC} [V]	2700
I_{OFF} [A]	**413**
L_{stray} [µH]	13
L_{load} [µH]	1000
t_{on} [µs]	135
R_{gon} [Ω]	1
R_{goff} [Ω]	270
V_{GE} [V]	-12/+19

Tab. 4 Test condition for turn-off as a single chip with real-application scaled L_{stray} and R_{goff}

As shown in Fig. 9, the device turned off at 413 A, V_{GE} 19 V, still located in the $V_{CE,sat}$ region. The chip was already undergoing a lot of stress because the large L_{stray} causes high overvoltage and triggers switching self-clamping-mode (SSCM) [4] [5]. The clamping voltage V_{SSCM} amounts 4400 V which is very close to the static V_{BR} value determined for this IGBT type in [6]. In SSCM holds according to [5]

$$\frac{d i_C}{d t} = \frac{V_{Clamp} - V_{DC}}{L_{stray}}.$$

The dissipated peak power is about 1.7 MW/cm². This shows an excellent overstress capability. By further increasing the turn-off current, the device failed by next pulse.

3 Simulation results

In this part, semiconductor simulations were carried out with Synopsys TCAD. A 2D half-cell model rated for 4500 V, 50 A was used. The turn-off behaviour for three turn-off situations is further explained, the internal characteristics, e.g. electric field, electron/hole density, etc. help to understand the different situations better.

3.1 Simulation of three turn off situations

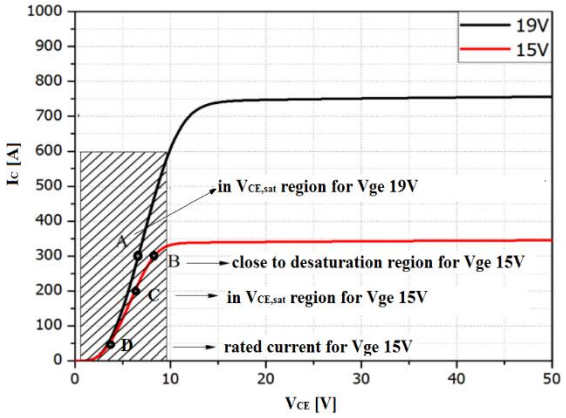

Fig. 10 Output characteristic for simulation model

First, the three turn-off situations were simulated. The turn-off initial states are marked in Fig. 10. In this figure, the point D stands for the nominal current (50 A) and represents the turn-off initial state for situation I. Point C describes a value of four times nominal current (200 A) and represents the turn-off initial state for situation II. Point B holds for six times the nominal current (300 A) and represents the turn-off initial state for situation III.

a) Turn-off at situation I, Fig. 10, point D

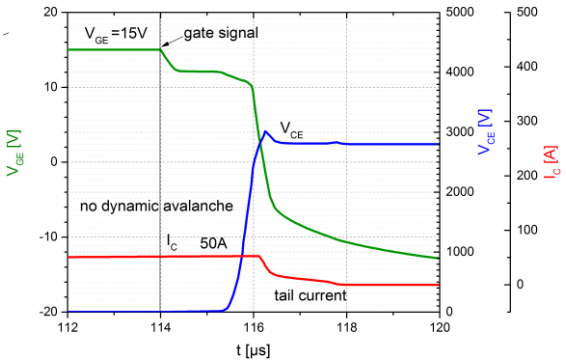

Fig. 11 TCAD simulation for turn-off at situation I, Fig. 10, point D, L_{stray} = 1200 nH, R_{goff} = 72 Ω

Situation I is shown in Fig. 11. No V_{GE} increase can be found. The IGBT is turned off in the normal operating region. At the end of the current slope, the tail current can be seen clearly. No dynamic avalanche was observed as there was no obvious changing of dv_{CE}/dt.

b) Turn-off at situation II, Fig. 10, point C

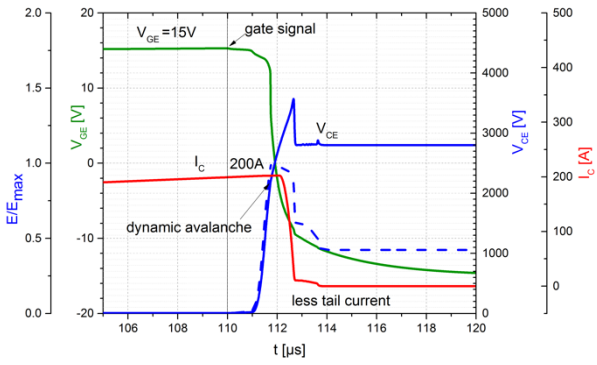

Fig. 12 TCAD simulation for turn-off at situation II, Fig. 10, point C, L_{stray} = 1200 nH, R_{goff} = 72 Ω

The second situation showing the process of turn-off under four times rated current is depicted in Fig. 12. The turn-off region is close to the boundary of the saturation region and desaturation region. At the moment of turn-off, marked as ‘‘gate signal’’ in Fig. 12, V_{CE} increases to 7 to 10 V. As the increase of V_{CE} cannot be ignored, the displacement current through the gate cannot be neglected anymore. The details will be explained in the following.

At the beginning of the inductance charging, the V_{GE} of 15 V stays constant with increasing collector current. When the load current increases to the boundary of the saturation region of the output characteristic, V_{CE} gets greater than the on-state voltage from that time onwards.

The increasing V_{CE} influences the depletion capacitance, since the depletion region extends with the increasing collector-emitter voltage. Therefore, the whole capacitance between collector and gate C_{GC} decreases. The depletion capacitance part of C_{GC} starts to be charged in advance – a displacement current is flowing. This will raise the potential at the gate.

While the current is still increasing, V_{CE} also increases and quickly reaches the condition of pinch-off.

It has to be noted that the n-channel is pinched off at that moment but the electrons flow with a high velocity caused by a stronger electric field strength. Reducing electrons cannot compensate the increasing number of injected holes from the collector. In this case, dynamic avalanche is more prone to happen [3].

In Fig. 12, the dynamic avalanche happens when the maximum electric field reaches the peak value, around V_{CE} of 2500 V. At the same time, the channel is also closed. The dynamic avalanche generated electrons compensate a large number of holes from the collector and plasma. Compared to situation I, the duration of the Miller plateau is shorter. V_{GE} decreases quickly to the threshold voltage. This change in V_{GE} largely results from the fact that the depletion capacitance part of C_{GC} charges before the IGBT is turned off. With the passage of time, the electric field extends towards the n-buffer region, which removes already a large part of the plasma. The maximum electric field drops after the voltage spike.

c) Turn-off at situation III, Fig. 10, point B

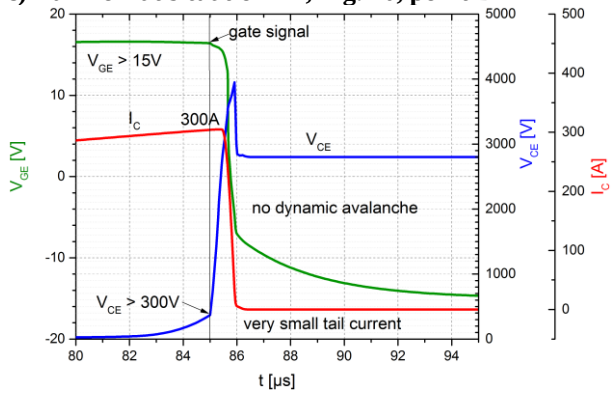

Fig. 13 TCAD simulation for turn-off at situation III, Fig. 10, point B, L_{stray} = 1200 nH, R_{goff} = 72 Ω

The last situation can be described as follows: at the end of the charging pulse, V_{CE} increases much more than the on-state voltage. It goes up along the output curve to the desaturation region and amounts to 300 V, see Fig. 13. In this case, the channel is pinched off early during the pulse and the junction-capacitance part of C_{GC} is charged already significantly. The displacement current through C_{GC} also causes the increase of V_{GE}. After starting the turn-off event at the gate driver there is no dynamic avalanche happening, even though the load current arrives at six times rated current. Furthermore, V_{CE} increases so quickly because there is no dynamic avalanche [7]. Besides, the duration of the Miller plateau is also short. Before V_{GE} has reached the threshold voltage V_{TH}, the electric field has been built up. Therefore, injected holes from the collector flow with high drift velocity through the base region. The current density drops a lot compared to the voltage saturation region. After V_{CE} reaches the DC link voltage, the decreasing I_C induces a high voltage spike in this case. The reason is that without dynamic avalanche, no avalanche generated electrons from the depletion region compensate the holes from the plasma or collector inside the device.

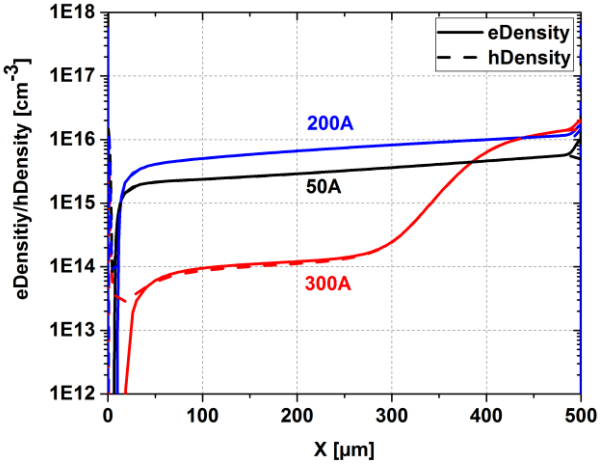

Fig. 14 Carrier density at turn-off moment of point B, C, D from Fig. 10, marked as ‘‘gate signal’’ in Fig. 11, Fig. 12 and Fig. 13

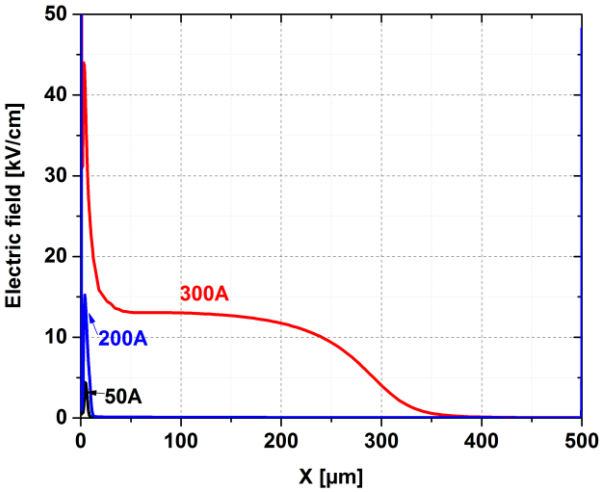

Fig. 15 Electric field at turn-off moment of point B, C, D from Fig. 10, marked as ‘‘gate signal’’ in Fig. 11, Fig. 12 and Fig. 13

To prove the explanation above for situation III, the comparison of the carrier densities and the electric field distribution between situation I, II and III is given in Fig. 14 and Fig. 15. At the moment of the gate signal turned off, which are marked as ‘‘gate signal’’ in Fig. 11, Fig. 12 and Fig. 13, the carrier density has dropped to 1E14 cm^{-3} for 300A, while the carrier density for 200A remains still at 7E15 cm^{-3}. The free carriers occupy the whole base region for 200A, and the electric field peak at that moment is not very high, because the IGBT is still at the boundary of the voltage saturation region. For 300 A, it is clear to see from Fig. 15 that the electric field already expands towards the collector side and occupies the most area of n^- region.

3.2 Simulation of turn-off at different gate voltage

As already measured in the chapter 2.1c, the simulation in this part can also verify that explanation. The device was turned off at the same current but a different gate voltage, see Fig. 10, point A and B. According to the output characteristic at V_{GE} 19 V, the turn-off current 300 A is still in the voltage saturation region. Therefore, V_{CE} stays around the on-state voltage before turn-off. The displacement current can be neglected at the beginning of the turn-off event. With a high carrier density before the turn-off moment, the existence of the dynamic avalanche suppresses the voltage spike visible in Fig. 13. Although the two simulation projects are turned off at the same current 300 A, the behaviour of the turn-off process is quite different.

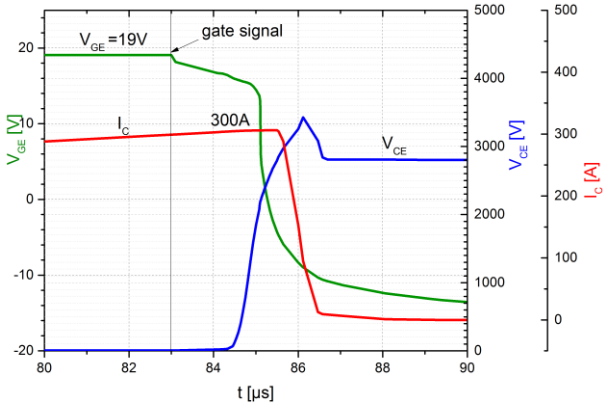

Fig. 16 TCAD simulation for turn-off for point A with V_{GE}=19V, Fig. 10, L_{stray} = 1200 nH, R_{goff} = 72 Ω

Comparing Fig. 16 with Fig. 13, the tail current is smaller at V_{GE} 15 V and the duration of the turn-off process is shorter. Because at V_{GE} 15 V a part of the charge-carrier plasma is already extracted in advance of the negative d*i*/d*t* phase (see Fig. 14 and Fig. 15). The formation of the electric field occurs earlier compared to V_{GE}=19V.

4 Conclusion

In this paper, it has been shown with experiment and simulation that IGBTs can be turned-off at high over-currents and even at the transition from overcurrent to voltage desaturation like in short circuit. The overcurrent turn-off is classified in situation I, II and III based on the simulation and measurement results of 4500 V IGBTs. The initial state of turn-off, e.g. expansion of the electric field and the electron/hole density, is the key to distinguish these three turn-off situations. Additionally, the rise of the gate voltage is an indication of the turn-off towards the desaturation region. The dynamic avalanche is influenced by the charging state of the gate and it can suppress high voltage spikes. The tail current is smaller, if the electric field is already partially established before the gate signal turns to negative. At the transition from voltage saturation to current saturation, the IGBT is released from dynamic avalanche. The simulation shows a stabilizing effect. However, high overvoltage peaks must then be withstood by the device.

There are still some points to be investigated in future work: the behaviour at high operation temperature, the overshoot of V_{CE} and the shape of it and the SSCM mode. Also, a turn-off at even higher gate voltages could be of interest. Further, a possible current filamentation process at multi-cell models should be investigated.

5 Acknowledgements

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Current Instabilities in Large-Area Silicon Diodes: An Accurate TCAD Approach

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Abstract

Fast-recovery diodes can exhibit negative differential resistance during reverse recovery which is associated with the formation of current filaments triggered by the presence of inhomogeneities along the device. Physics concerning the dynamics of current filaments has been widely analyzed in literature through numerical simulations. However, a method to clearly identify the elements that dominate on the current pattern formation is still not available since filaments can appear also in uniform structures. In this work, a novel TCAD approach is provided to suppress the numerical errors due to the discretization of the transport equations which allows us to analyze the effects of the junction depth and the presence of different doping inhomogeneities in the anode doping profile of large-area diodes.

Keywords: Fast-recovery diode, Reverse recovery, Current filaments, Numerical simulations

Introduction

Fast-Recovery Diodes (FRD) play a fundamental role the state-of-the-art power converters. Any active switch adopted for power conversion, such as MOSFET, IGBT and IGCT requires a complementary free-wheeling FRD [1] [2]. The circuit with IGCTs require also clamping FRD. All these FRDs have to cope with high dynamic stress during the turn-off of inductive load. That is, they must be able to safely turn off even with very high *dI/dt* rate and high DC link voltage V_{DC}. During the switching process the so-called dynamic avalanche condition occurs: the charge carriers extracted from the plasma cross the space charge region of a blocking junction and increase the effective positive/negative charge hereby enhancing the electric field peaks [3]. For this reason, the effective breakdown voltage (BV) during the reverse recovery transient can be significantly lower than the static BV, leading to current instabilities [4] [5] [6]. During the reverse recovery, diodes can exhibit a negative differential resistance which is correlated with the inhomogeneous current density distribution along the device [7] [8]. The consequent current filamentation may lead to the destruction of the device [9] [10] [11]. The physical mechanism concerning the pattern formation have been successfully analyzed through numerical simulations in several works. Even if the non-linear dynamics of current filamentation was nicely investigated in the previous works, the fundamental origin of the instability was not addressed. As it is known, the current filaments can be easily caused by the numerical errors in the discretization of the transport equations, providing the formation of current filaments in perfectly uniform structures, as e.g. in [7] [8]. Under such conditions, it becomes very difficult to study how the different non-homogeneities which may arise in a real device contribute to the formation of current filaments [12]. In this work, a method to suppress the numerical error and to clearly distinguish fluctuation due to the discretization of transport equation from those coming from a non-homogeneity in the device is provided and applied to 4.5kV FRD [13].

TCAD setup

Numerical simulations are a useful tool in the analysis of current fluctuations in power diodes under reverse recovery conditions. It is well known that the presence of any kind of non-homogeneity can be the starting point for the formation of current filaments. It is then fundamental to find a precise TCAD setup minimizing the non-homogeneous distribution of the numerical errors so as to allow for the study of specific physical inhomogeneities in the device.

Device used for simulations

The simulated device is the FRD with a wafer thickness of $660\mu m$. The effective device area is in the order

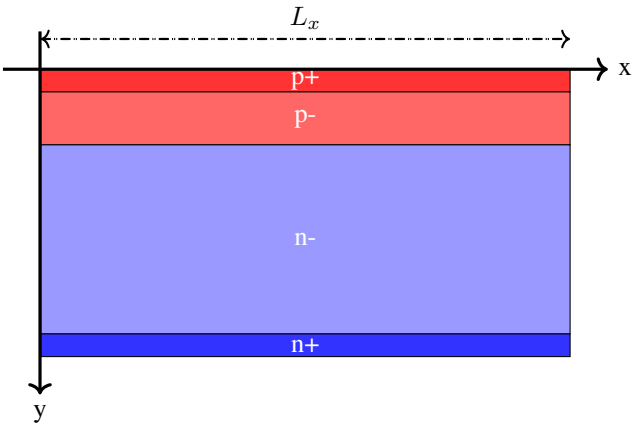

Fig. 1. Schematic representation of the power diode

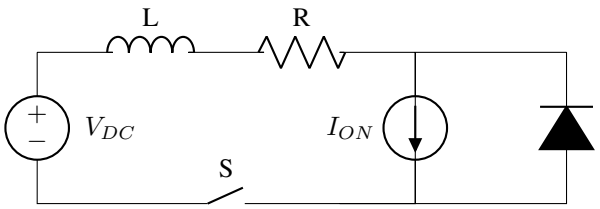

Fig. 2. Test circuit used for reverse recovery simulations. $V_{DC} = 2800V$, $I_{ON} = 2500A$, $L = 325nH$, $R = R_0 e^{-t/\tau}$ with $R_0 = 23\Omega$ and $\tau = 0.75\mu s$

of $10^8 \mu m^2$ regardless of the lateral width L_x of the structure. Device simulations have been performed by the drift-diffusion transport equations in two dimensional (2D) structure under transient condition [14]. The SRH recombination has been accounted for with lifetimes equal to $\tau_e = \tau_h = 1ms$. Avalanche generation (UniBo impact ionization model), Auger recombination, mobility doping dependence and carrier-carrier scattering have been accounted for with default parameters. Default values of the surface recombination velocities have been used at the Aluminum/Silicon interfaces. Iso-thermal conditions have been assumed with a fixed ambient temperature of T = 413K. A schematic view of the device is shown in Fig. 1. The circuit used to simulate the reverse recovery transient is reported in Fig. 2 along with the corresponding component values corresponding to real power converter.

Meshing Criteria

In order to limit the current instabilities due to non-homogeneous meshing of the device, a specific grid has been created to simulate the FRD under reverse recovery transient. In this section the criteria adopted to generate the grid are given. Starting from the uniform diode we checked that the proposed meshing criteria would give rise to grids with negligible current fluctuations as expected when an ideal device is used. The lateral width of the device is fixed at $L_x = 1000\mu m$. A uniform rectangular grid geometry was chosen because, differently from a triangular mesh, it reproduces the

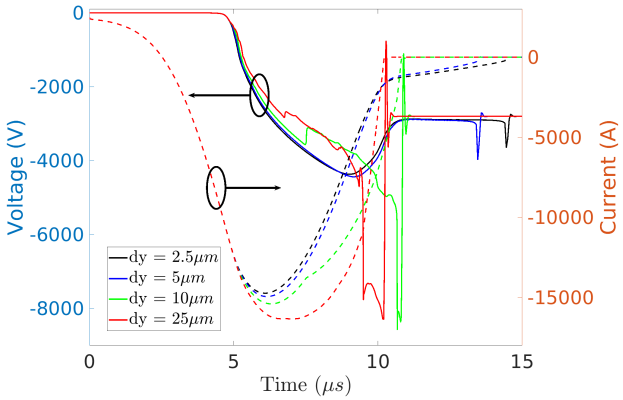

Fig. 3. V(t), I(t) for the same device but with different mesh spacing in the drift region

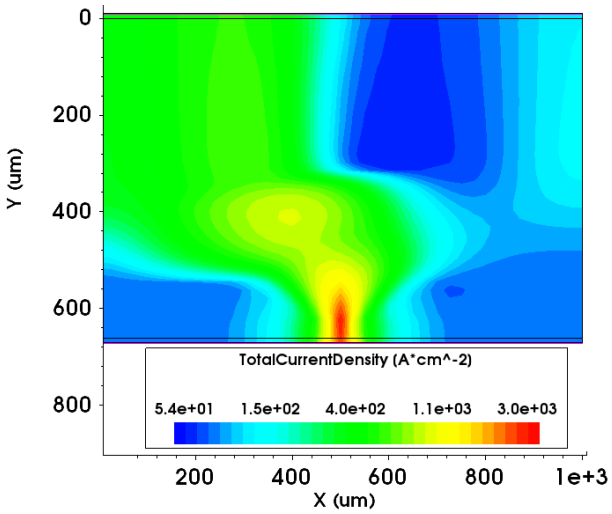

Fig. 4. 2D contour plot of the simulations with mesh-spacing dy = 25μm at t = 7.41μs showing the presence of cathode-side current filaments.

homogeneity of the current distribution as shown in [12]. The grid used to simulate the diode was defined as follows. A uniform spacing along the x-axis (dx) is fixed with $dx = 25\mu m$. Differently, in the vertical direction the p-n junction requires to adopt fine grid spacing close to the p-n junction and near the electrode. To this purpose the spacing along the y-axis (dy) is $1\mu m$ for all simulations. Different dy in the drift region have then been tested. In Fig. 3, the simulated voltage and current curves for the FRD in reverse recovery conditions are reported for different vertical grid space. The V(t) curves of structures with larger dy ($10\mu m$ and $25\mu m$) show significant voltage overshoots, which correspond to the presence a of moving anode filaments and static cathode-side filament in the middle of the device as shown in Fig. 4. In the case of shorter dy, smooth and regular curves were observed for both $dy = 5\mu m$ and $dy = 2.5\mu m$. However, by monitoring the maximum current contribution to current density in the x-direction during reverse recovery, which should be ideally zero due to the uniformity of the p-n junction, a significantly higher contribution was found for $dy > 2.5\mu m$ as shown

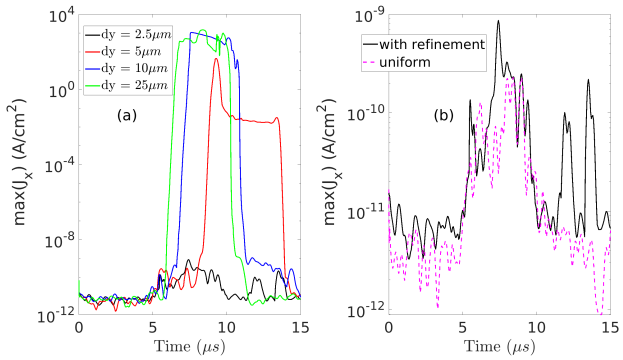

Fig. 5. Maximum value of the current density x-component as function of time. (a) $\max(J_x)$ corresponding to simulations of Fig. 3. (b) both simulations have $dy = 2.5\mu m$ in the drift region. Black solid line: with refinement ($dy = 1\mu m$) at the p-n junction and at the contact. Magenta dashed line: with $dy = 2.5\mu m$ everywhere.

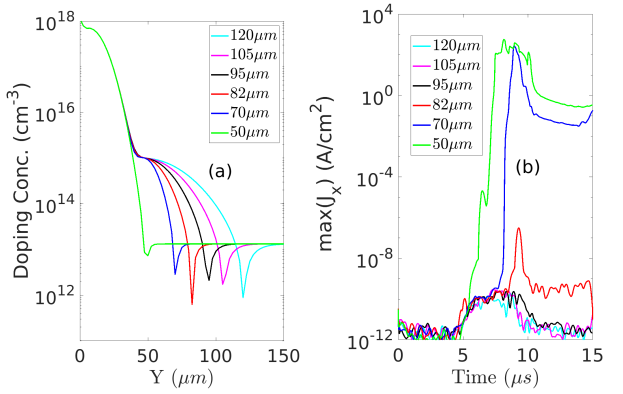

Fig. 6. (a) Anode doping profile with different junction depth (y_J). (b) Maximum value of J_x as function of time.

in Fig. 5(a). This led to the choice of the best dy in the drift region, which gives a numerical error on the current fluctuations comparable to the case of a uniform grid as shown in Fig. 5(b). In conclusion, the most suitable setup for the reverse recovery simulations of power diodes consists of a uniform rectangular grid with spacing along the y-axis small enough to suppress as much as possible what needs to be checked by monitoring the x-component of the current density.

Factors enhancing the generation of current filaments

With the setup described above, we will further investigate three different factors that can cause pattern formations.

Anode doping profile

Simulations of the FRD with different anode doping profiles have been carried out as shown in Fig. 6 (a). The depth of the p-n junction, y_J, has been chosen so as to have the same static breakdown conditions due to the punch through, but, viceversa, to strongly affect the electric field peak at the p-n junction leading to a larger impact ionization in dynamic conditions. This is

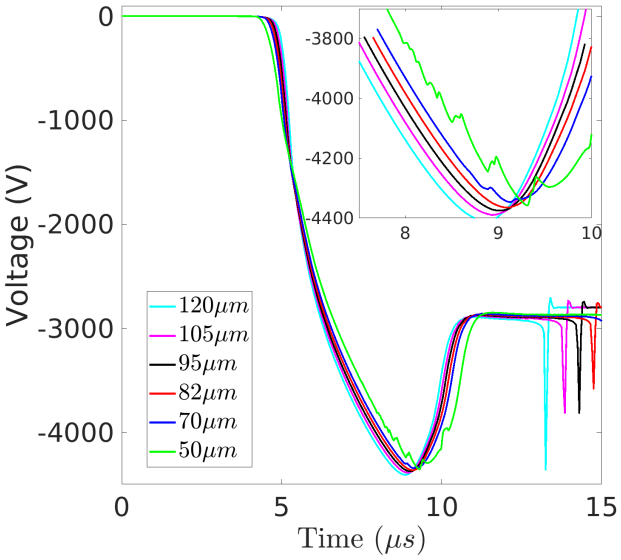

Fig. 7. V(t) reverse recovery curves of diode with the doping profile shown in Fig. 6(a).Inset: zoomed curves in the time range from 7.5 to 10us.

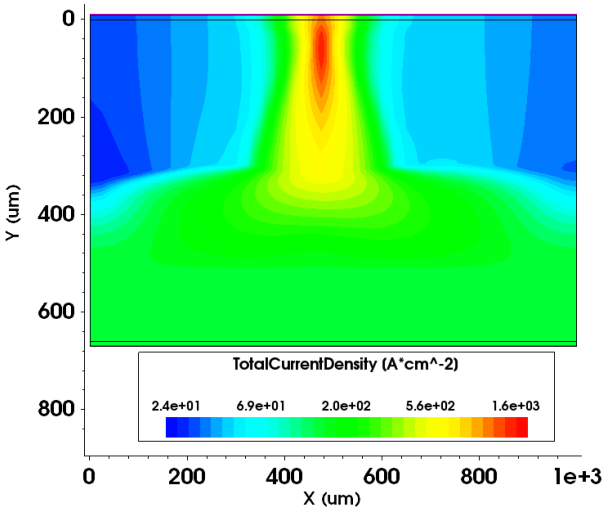

Fig. 8. 2D contour plot of the diode with the $50\mu m$ deep p-base from Fig. 6(a) at t = $8.65\mu s$ showing the presence of anode-side current filaments.

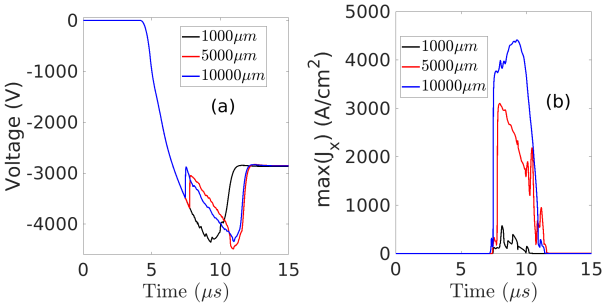

Fig. 9. (a) V(t) curves of the diode with $50\mu m$ deep anode doping profile and different lateral width L_x (b) Maximum value of J_x corresponding to simulations shown in (a).

clearly shown in Fig. 6 (b) where the J_x fluctuations are compared for the different y_J. No significant fluctuations are observed for $y_j \geq 95\mu m$. On the contrary, there is no way to suppress current fluctuations for lower y_j,

even if the device is ideally uniform. This gives rise to current filaments occurring in the time range from 7.5 and 10 μs, as shown in Figs. 7 and 8. By using this kind of simulations, the smallest value of y_j providing high ruggedness to dynamic turn-off can be extracted.

Lateral width of the simulated device

It is known form literature [15] that instabilities can easily develop into current filaments if the device has large lateral dimension L_x. This can be shown by performing simulations of the same diode but with different L_x. In Fig. 9(a), simulations of three diodes with $y_J = 50\mu m$ and lateral lengths L_x = 1000, 5000 and 10000μm are compared. The shortest one corresponds to the reference diode used in the analysis of the anode doping profile which gives rise to the anode current filament shown in Fig. 8. The comparison of the V(t) curves shows, that the significant voltage peaks in the V(t) of the diodes with larger Lx (Fig. 9(a)) correspond to the sudden increases of Jx (Fig. 9(b)) manifested by the formation of a cathode-side filament in addition to the anode-side one (not shown). This result is in good agreement with expected theoretical results and experimental evidence as well.

Doping Fluctuations

Small doping inhomogeneities in the anode profile, which are common in all power diodes [16], are suspicious to play a role in the onset of current instabilities. In order to investigate the effect of such non-uniformities on the generation of current filaments, a single doping inhomogeneity has been added in the middle of the diode structure with $y_J = 95\mu m$ and $L_x = 1000\mu m$, which is one of the stable structures in Fig. 6. The lateral extension of the inhomogeneity was fixed to $100\mu m$, while different possible profile shapes of a potential non-uniformity have been tested as shown in Fig. 10 (a). The corresponding magnitudes of the maximum J_x reported in Fig. 10 (b) clearly show that the worst case is given by the doping profiles with locally lowered concentration (B1 and B2) contrary to the increased one (A1 and A2). Even if no filaments were generated by such fluctuations, a larger instability with respect to the homogeneous reference case is found, which might be the cause of the onset of instability, if other factors promoting the instabilities discussed above take place.

Conclusion

In this work, a method to suppress the numerical error in reverse recovery simulations of power diodes has been provided to precisely analyze the formation of current filaments through TCAD simulations. Analysis of current fluctuations along the lateral direction shows that a rectangular mesh with uniform spacing along the x and y axis is the most suitable one to prevent the formation of current filaments in a uniform structure. Such method has been applied to study the factors

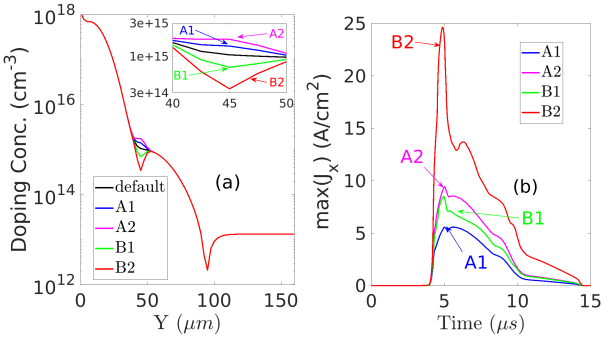

Fig. 10. (a) Vertical doping profile with small inhomogeneities (A1, A2, B1, B2) magnified in the inset (b). Maximum value of J_x corresponding to the simulations shown in (a).

that enhance the probability of filaments generation. A criterion to find the smallest value of the junction depth that provides a high dynamic ruggedness has been described. Theoretical predictions about the role of lateral dimension are confirmed by simulations performed with different values of L_x. In addition, the effects of different doping inhomogeneities has been considered showing how region with locally lower doping concentration are more susceptible to current instabilities. The proposed approach is a solid starting point for a rigorous analysis of the impact of different inhomogeneities, which may appear especially in the real large-area high-voltage fast recovery diode, hereby providing a useful tool for further enhancement of their ruggedness and reliability.

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Power device solutions for highly efficient power supplies

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Abstract

Switched mode power supplies (SMPS) for target applications covering a wide range from telecom rectifiers through servers to solar inverters or electric vehicle chargers share the need for high efficiencies in order to minimize the overall energy consumption and the total cost of ownership. With the appearance of wide bandgap semiconductors designers cannot only choose between different devices but also may benefit from using advanced topologies. This work compares important properties of a CoolSiC™ Silicon-Carbide MOSFET, a CoolGaN™ E-mode GaN power transistor, a TRENCHSTOP 5™ IGBT accompanied by a SiC Schottky diode and a CoolMOS™ Superjunction (SJ) device, and discusses an approach to avoid the limitations of SJ devices with respect to hard commutation of the body diode and evaluates the achievable efficiency in the AC-DC conversion stage of a power supply.

Keywords: power semiconductor, super-junction, wide bandgap, MOSFET, IGBT, SMPS

INTRODUCTION

The investigated four device technologies with a voltage rating of 600 V to 650 V differ substantially in their device structure in order to benefit most from the respective semiconductor material. Examples of the fundamental device structures are shown in Fig. 1 in order to explain the basic device properties [1-4]. The SJ- and the SiC-MOSFET are both vertical structures. However, the purpose of the incorporated p-regions in the vertical structure is different. While the SJ p-columns provide charge compensation to optimize the trade-off between low on-resistance and high breakdown voltage, the buried p-region of the SiC-MOSFET limits the electric field at the gate oxide to maintain the required oxide lifetime. Both devices have the drain on the backside. The IGBT is also a vertical but bipolar device with a backside pn-junction that provides the carriers for conductivity modulation in the drift region. The SiC device requires a roughly ten times smaller drift region length compared to the IGBT or SJ MOSFET, enabling both a strongly reduced area-specific on-resistance $R_{DS(on)}$ and small reverse recovery charge Q_{RR}. In contrast, the GaN device consists of a lateral structure placed on a (not shown) Silicon substrate. The Silicon backside is electrically isolated but typically tied to the source potential. The GaN device is based on the heterojunction High Electron Mobility Transistor (HEMT) structure and does not contain physical pn-junctions between source and drain. Instead, the channel builds through a highly conductive two-dimensional electron gas (2DEG) at the AlGaN/GaN interface. A recessed, non-isolated p-GaN gate is provided for local interruption of the 2DEG to achieve a normally-off (E-mode) device. This GaN transistor can be operated as a power switch or also as a diode in the reverse direction with practically zero reverse recovery charge Q_{RR}.

APPLICATION REQUIREMENTS

Fig. 2 shows the main building blocks of a power supply designed for a universal input voltage range of 85 – 265 VAC. The compared devices are intended for use in the AC-DC conversion power factor correction

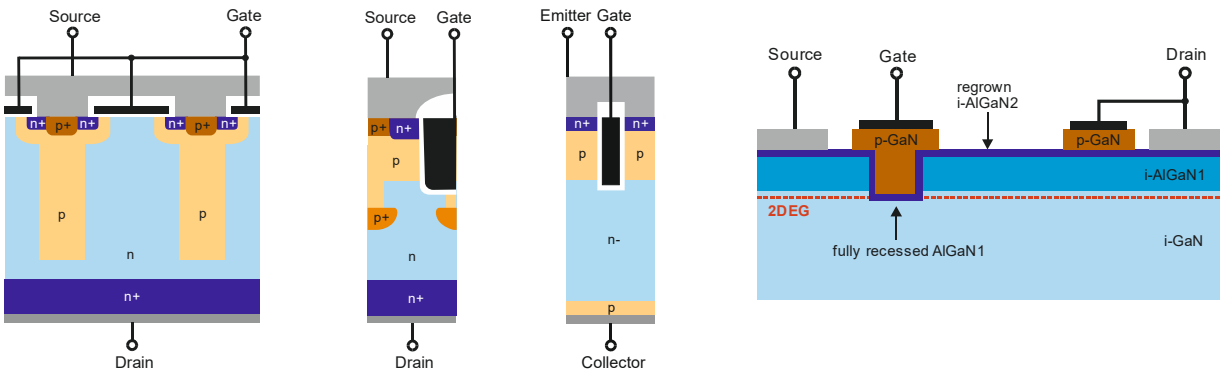

Fig. 1: Exemplary device structures: SJ-MOSFET [1], SiC-MOSFET [2], IGBT [3], E-mode GaN Power Transistor [4]

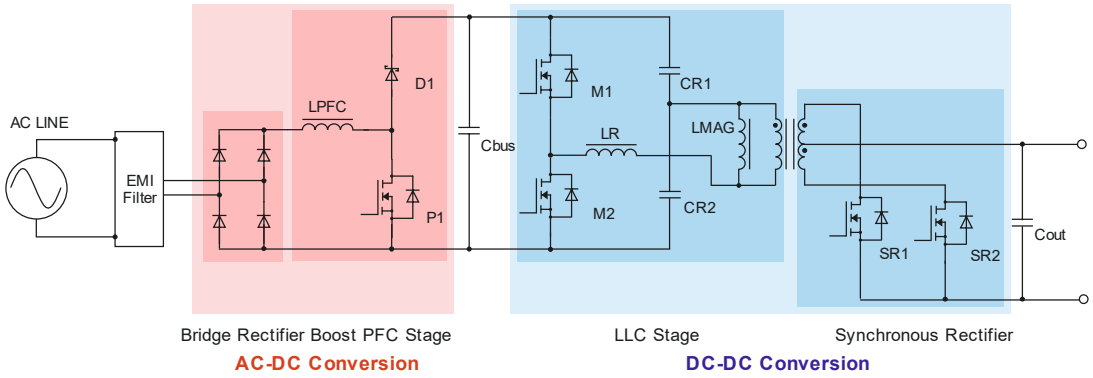

Fig. 2: Main building blocks of a power supply

(PFC) stage. The different device properties require the use of different topologies.

The PFC stage as shown in Fig. 2 employs a common Boost PFC topology as typically used with SJ devices. The typical operating frequency is limited to 70 kHz to keep the fundamental and second harmonics below 150 kHz due to EMI reasons. A higher operating frequency also clearly increases the switching losses. The typical control mode is the Continuous Conduction Mode (CCM) as here the ripple current losses and switching losses are well balanced. The PFC stage may also be operated in Discontinuous Conduction Mode (DCM) or Critical Conduction Mode (CrCM) at the cost of a much higher ripple current while at the same time enabling quasi Zero Voltage Switching (ZVS) for reduced switching losses. However, the input bridge rectifier is the dominant source of losses and is responsible for an efficiency loss of between 1 %…2 %. The switching losses of the transistor P1 strongly depend on the energy stored in the output capacitance; consequently it is good to use devices with low E_{OSS} values here. To achieve a higher efficiency, the use of a Dual Boost PFC stage is possible [5,6]. As shown in Fig. 3, the higher efficiency is paid for with a higher effort on the system side. To gain an even higher efficiency, one could replace the input diodes D3 and D4 by SJ MOSFETs working as synchronous rectifiers. This further minimizes the conduction losses, but the overall system effort and control complexity becomes even higher. Another topology offering comparable efficiency is the H4 PFC [5].

A better-suited topology is the Totem Pole PFC as depicted in Fig. 4 [7]. This bridgeless topology eliminates the need for traditional bridge rectifiers which contribute substantially to the overall losses in the PFC stage. While being a rather simple topology, the Totem Pole PFC is intrinsically capable of providing a bi-directional power flow and provides the highest practically achievable efficiency. However, this topology imposes serious challenges for the power semiconductors. The switching frequency of the power semiconductors WBG1 and WBG2 is relatively high with values of up to 100 kHz, with one transistor working as a boost switch and the other as a synchronous rectifier. The Totem Pole usually operates in Continuous Conduction Mode (CCM), however other control modes including DCM or CrCM may also be employed [8]. In any case, this topology requires devices with low values of reverse recovery charge Q_{RR} to enable the repetitive hard commutation operation of a conducting body diode. The output capacitance dependency on the drain voltage must avoid sharp drops, in addition a low output charge Q_{OSS} is needed to facilitate short dead times and to enable higher switching frequencies. This low output charge together with a small value of E_{OSS} helps to achieve high efficiencies. Wide bandgap devices provide all these properties and are a perfect match for this topology.

IMPACT OF DEVICE TECHNOLOGY ON THE DEVICE PARAMETERS

Thermal Considerations

Being wide-bandgap semiconductor devices, the chip area for SiC and GaN devices of a given on-resistance is several times smaller than for a silicon device. A smaller area leads to an increase in the thermal resistance from junction to case R_{thJC}. SiC is advantageous in terms of its much higher thermal

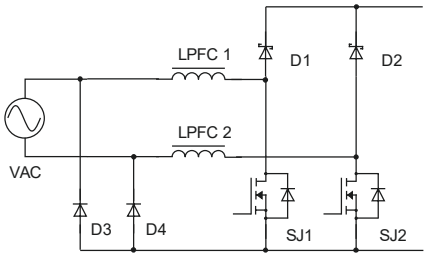

Fig. 3: Dual Boost PFC stage

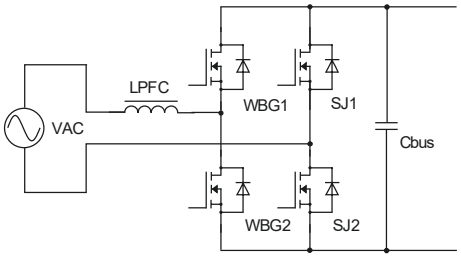

Fig. 4: Totem Pole PFC stage

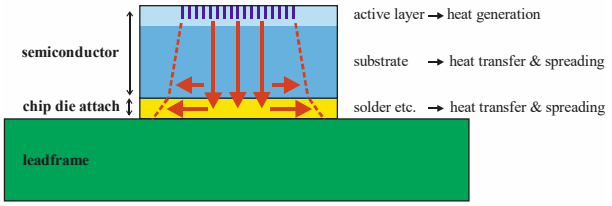

Fig. 5: Simplified illustration of heat flow (red arrows) and heat spreading (dashed lines) in the power device

conductivity of 360 W/m K compared to 150 W/m K for the other two devices. This better thermal conductivity largely compensates the increased R_{thJC} value due to the reduced chip area. The GaN device is limited here by the thermal conductivity of the Silicon substrate. As it is a lateral device, the chip area is larger compared to a SiC MOSFET. Still, this cannot fully compensate for the increased thermal resistance, and a good thermal design becomes crucial. A higher thermal conductivity is also beneficial for the lateral heat spreading within the chip itself as illustrated in Fig. 5 for two reasons: Firstly, the heat is only generated in the active area of the chip and not in the surrounding inactive parts (like the edge termination). Secondly, the heat is not generated over the full thickness of the semiconductor die. Instead, almost all of the power dissipation occurs within the active region of the device. Its thickness depends on the properties of the semiconductor material. Wide bandgap semiconductors require much less thickness here than Silicon. Also the die attach from the chip to the lead frame plays a significant role. The use of a traditional soft solder process introduces a solder layer with a thickness of up to 120 µm. This increases the thermal resistance from junction to case and limits the thermal performance especially for smaller chips. Diffusion solder processes [9] enable much thinner layers for the die attach and, in addition, the use of thinner semiconductor substrates. All these factors can reduce the thermal resistance R_{thJC}.

Temperature dependence of on-resistance

The temperature dependence of the on-resistance, shown in Fig. 6, indicates major differences between the investigated device technologies. The SiC-MOSFET shows the smallest increase with junction temperature T_J. From an application point of view, this small increase with temperature offers a benefit. It means that if all devices come with an identical $R_{DS(on)}$ at the datasheet condition of 25 °C, the on-state resistance for the typical operation junction temperature of 100 °C of the silicon SJ device is 45 % higher and for the GaN device it is 25 % higher than for the SiC MOSFET.
Considering the thermal behavior discussed before and the junction temperature dependence of the on-resistance, the SiC device and the IGBT show the best overall performance. To give an example, a CoolMOS CFD7 57 mΩ device operated at a temperature of 100 °C could ideally be replaced by a 62 mΩ CoolGaN device or by a 84 mΩ CoolSiC part. An appropriate selection of the device on-resistance at the targeted operation temperature is key to enabling cost savings and achieving substantially lower dynamic losses.

Transfer Characteristics

Another aspect that needs to be considered is the proper choice of the gate drive voltage. While the CoolSiC devices can generally be used with the same standard gate drivers as CoolMOS parts, this is not recommended due to differences in the transfer characteristics.
Fig. 7 compares the transfer characteristics for all technologies at temperatures of 25 °C and 150 °C. The CoolMOS device reaches its full current capability with gate voltages of V_{GS} = 10 V while the IGBT is still far from saturation The characteristics of the CoolSiC device shows a lower transconductance and the use of higher gate voltages gives a benefit as the on-resistance reduces. So it is recommended that a gate drive voltage of V_{GS} = 18 V is used for CoolSiC devices.
The further comparison of the different transfer characteristics depicted in Fig. 7 indicates that the impact of junction temperature is lowest for the IGBT and the CoolSiC part. In contrast, the CoolGaN devices reach the required current capability at much lower gate voltages due to the low typical achievable threshold voltage of 1.2 V. To gain immunity against unwanted parasitic turn-on, a negative gate voltage of down to V_{GS} = -5 V should be considered for use of these parts in hard-switching totem-pole configurations.

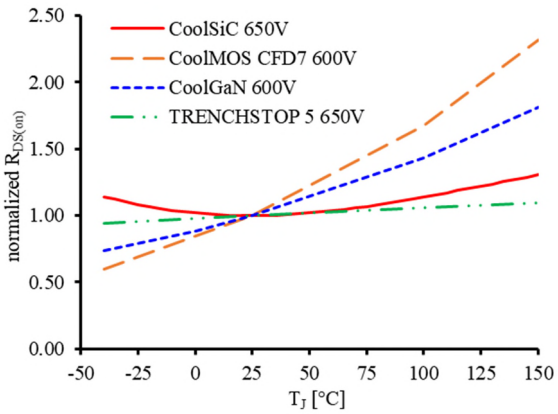

Fig. 6. Normalized temperature dependence of $R_{DS(on)}$ for the different device technologies

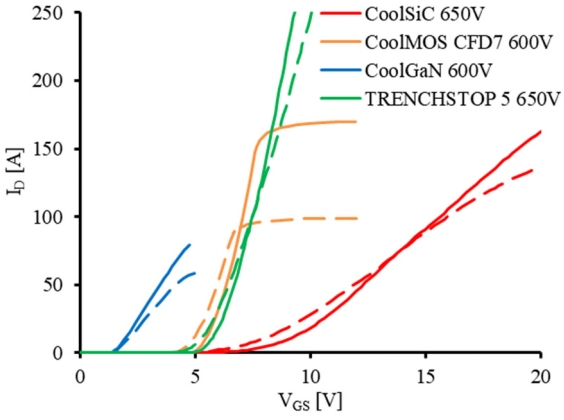

Fig. 7: Transfer characteristic comparison at two temperatures (solid lines – 25 °C, dashed lines – 150 °C)

Device breakdown

Due to the differences in the properties of the semiconductor materials and the device structures, also the drain-source breakdown behavior differs.
In the case of the two MOSFETs and the IGBT, the breakdown mechanism is due to impact ionization at a pn-junction once the electric field in the device structure exceeds the critical electric field strength. The breakdown voltage is temperature dependent and governed by the impact ionization rates that reduce at elevated temperatures, therefore the breakdown voltage increases with temperature. Fig. 8 compares the temperature dependent breakdown voltages of the silicon and silicon-carbide devices, indicating a stronger dependence for the silicon part. From an application point of view, the higher breakdown voltage at low temperatures for the CoolSiC and IGBT devices is beneficial for usage in outdoor applications or if devices need to start up at lower temperatures.
In the case of the GaN device, the breakdown mechanism is different due to the device structure [10]. The breakdown is not limited by the critical electric field of the semiconductor but by the dielectric strength of the surface materials in the lateral GaN HEMT structure. The breakdown mechanism is a dielectric breakdown similar to the one found in ceramic capacitors. This behavior requires a destructive failure limit that must be at least 50 % larger than the maximum rated peak voltage of the device in order to safely avoid device degradation. This different breakdown behavior as well as the much higher breakdown voltage are clearly visible in the breakdown characteristics as depicted in Fig. 9. In contrast to the MOSFET and IGBT devices, the CoolGaN device shows an exponential current increase.

Forward voltage of body diode

There are significant differences in the body diode conduction between the device technologies. The CoolMOS and CoolSiC devices both incorporate an intrinsic pn-diode structure as is usual for a power MOSFET. Nevertheless, the forward voltage of the SiC

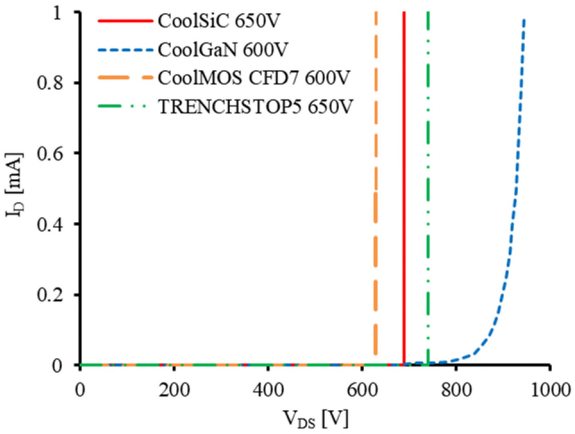

Fig. 9: Breakdown characteristics for the different device technologies at room temperature

device is around four times higher than that of the silicon MOSFET due to the wide bandgap of the silicon-carbide material. The forward voltage V_F shows a negative temperature coefficient for both materials. Due to the larger conduction losses of the CoolSiC body diode it is not efficient to use the intrinsic diode to conduct current over long periods of time. The impact on the light-load efficiency in an LLC converter can be as big as 0.5 %. As such it is recommended to limit body diode conduction to dead-time operation and employ synchronous rectification to limit the body diode conduction losses. Synchronous rectification has the additional benefit that the positive temperature coefficient of $R_{DS(on)}$ supports current sharing.
The IGBT does not contain an intrinsic body diode and requires a separate freewheeling diode. The IGBT is accompanied by the latest SiC Schottky diode technology [11] that comes with the lowest forward voltage V_F currently available in this voltage class.
In the case of the CoolGaN device, the structure does not incorporate an intrinsic diode structure. However, with the gate driven to the on-state, the GaN HEMT will conduct current equally well in either direction. If the gate is turned-off at $V_{GS} = 0$ V and the drain potential exceeds the gate threshold voltage, the HEMT structure turns-on and begins conducting in the reverse direction with a voltage drop of about 2 V. Applying a negative

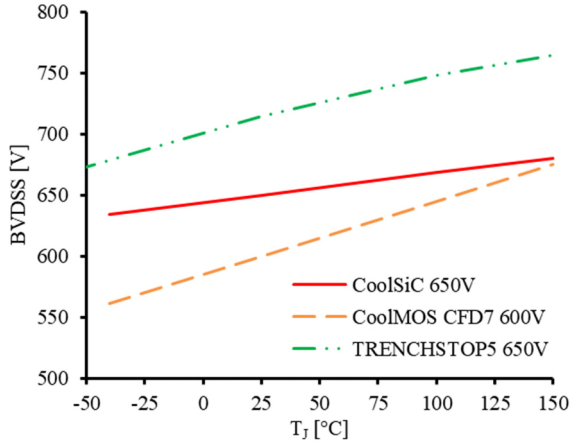

Fig. 8: Comparison of temperature dependence of breakdown voltage for CoolMOS, CoolSiC and IGBT devices

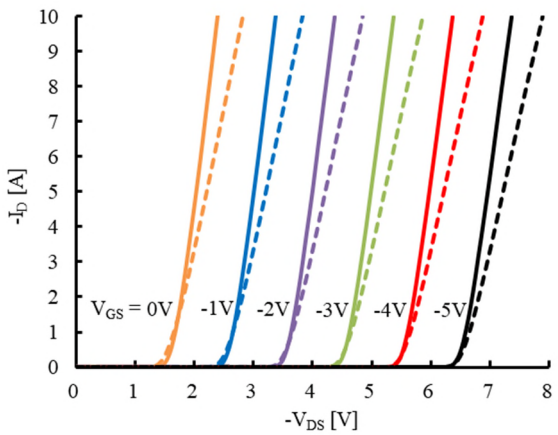

Fig. 10: CoolGaN 3rd quadrant characteristics at two temperatures (solid lines – 25°C, dashed lines – 125°C)

gate-source voltage will shift the onset of reverse conduction appropriately and the "diode-like" voltage drop increases as depicted in Fig. 10. Consequently one should also limit this "diode-like" conduction mode to a brief period during the dead time between switching intervals as in the case of SiC devices.

Gate drive considerations

The gate drive requirements are practically identical for SJ- and SiC-MOSFETs and IGBT, however the SiC device benefits a lot from a higher $V_{GS} = 18$ V. The GaN device is a gate injection transistor (GIT) and the required gate-driving scheme differs significantly. Different to all other devices, the CoolGaN device has a non-isolated gate with a pn-diode between gate and source. The forward voltage V_F of 3.0 … 3.5 V is defined by the GaN band structure. It is evident that the V_F must always be higher than the threshold voltage of the transistor, which is ensured by the comparably low achievable threshold voltage of GaN devices. However, it is this gate diode that requires a different driving scheme compared to devices with insulated gates.
As for any MOSFET, the switching speed depends on the gate current available in the Miller plateau phase. In the case of a GaN device with a non-isolated gate, a permanent current I_{SS} will flow into the gate diode during the on-state, see Fig. 11. As this current causes additional losses, it should be kept as small as possible. However, gaining low switching losses requires large peak currents I_{ON} and I_{OFF} in the transition phases. To achieve this, the classic gate resistor is substituted by a RC network that provides two parallel branches as depicted in Fig. 12. Here, a small resistor R_{on} is coupled to the gate via the capacitor C_C while a large resistor R_{ss} provides the direct current path for the stationary on-state. The capacitor C_C provides the required charge to drive the transient current I_{on} defined by the value of the resistor R_{on}, assuming properly dimensioned values of the parts [12]. If the device is turned off, the gate-drive voltage level shifts to negative values again due to the capacitor C_C. This guarantees a fast turn-off transient and the avoidance of a potential re-turn-on.

Capacitances and Charges

Fig. 13 - Fig. 16 compare the output capacitance, the output charge, the energy stored in the output capacitance, and the gate charge of the different

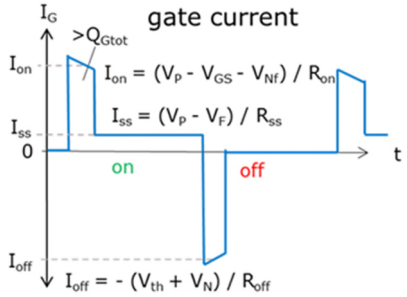

Fig. 11: Driving scheme of the GaN Power Transistor

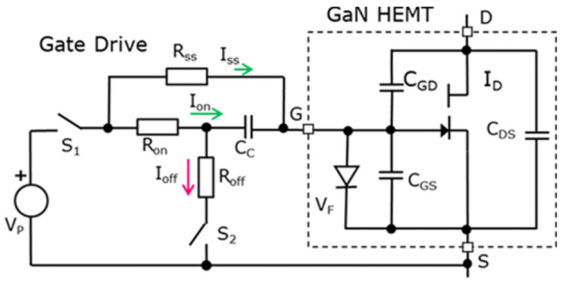

Fig. 12: Equivalent circuit to properly drive the gate of the GaN Device

technologies using devices with a comparable on-resistance of 50 - 55 mΩ at nominal current and room temperature (e.g. for normal datasheet conditions). With respect to the output capacitances as shown in Fig. 13, the CoolMOS technology offers a smaller output capacitance than the other devices at $V_{DS} > 24$ V. Therefore, the CoolMOS is capable of offering lower switching losses in a standard boost PFC application. However, the CoolMOS shows a more sensitive behavior to PCB and design related parasitic elements as well as larger V_{DS} overshoots during turn-off. At drain voltages larger than 24 V, the output capacitances of the SJ-MOSFET and the GaN device are almost identical. However, the lower output capacitances of the GaN and SiC MOSFET and the IGBT below $V_{DS} = 24$ V represent a clear benefit as it allows an overall faster transition of the drain voltage. GaN offers the lowest C_{OSS} values below $V_{DS} = 24$ V which translates into a lower output charge Q_{OSS} and a lower E_{OSS} of the GaN transistor as indicated in Figs. 14 & 15.
In terms of output charges, both wide bandgap devices offer a clear benefit over the SJ MOSFET. The lower Q_{OSS} value allows either the discharge of the output capacitance with a lower re-circulating current or the minimization of the dead time. Short dead time settings are important in conjunction with wide bandgap devices in order to minimize body diode conduction losses related to a forward voltage drop which is four times higher than the CoolMOS device. As shown in Fig. 15, CoolSiC has a higher E_{OSS} than CoolMOS and CoolGaN technology. The E_{OSS} represents the minimum energy that translates into switching losses in standard hard switching topologies. However, the large output charge together with the dramatically larger reverse recovery charge of SJ devices usually prevents these devices from being used in hard-switching bridge topologies such as in a Totem Pole.
Fig. 16 compares the gate charge characteristics at a drain current of ~9 A as typically used in the targeted application. Lower overall gate charge values result in lower driving losses at higher switching frequencies and enable higher efficiencies in light-load operation. Here the SiC-MOSFET shows a clearly smaller value than the CoolMOS and IGBT devices, nevertheless the difference gets smaller if the SiC device is driven with the recommended on-state gate voltage of $V_{GS} = 18$ V.
In comparison, the gate charge of the CoolGaN device is substantially smaller, acting as an enabler for high-frequency applications. However the losses due to the

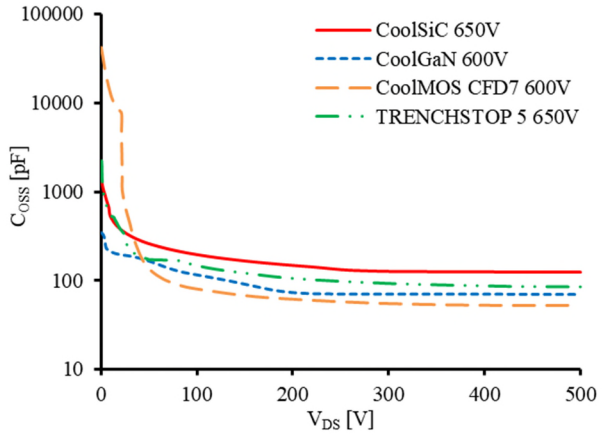

Fig. 13: Comparison of the output capacitances

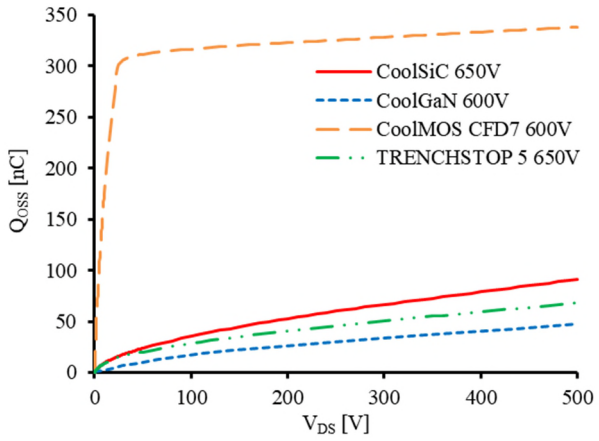

Fig. 14: Comparison of the output charges

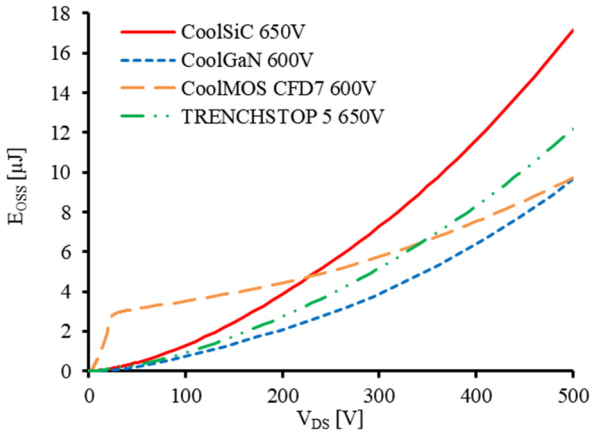

Fig. 15: Comparison of the energies stored in output capacitance

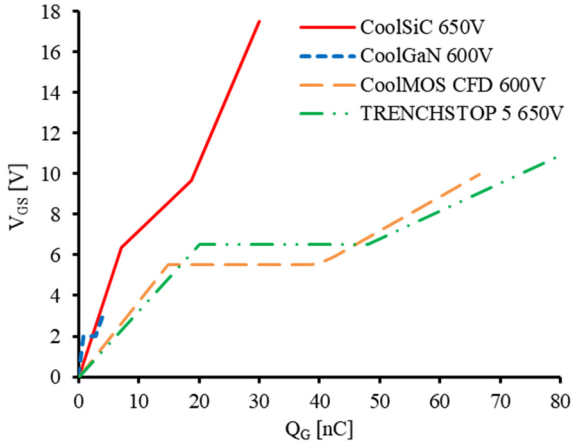

Fig. 16: Comparison of the gate charges

stored energy in the output capacitance E_{OSS} remain at comparable levels to other device technologies. A high-frequency operation will be most efficient in soft-switching or resonant topologies.

Reverse Recovery Charge

The reverse-recovery charge Q_{RR} is a very important factor for highly efficient hard-switching topologies like the CCM Totem Pole PFC discussed in this work. This charge builds-up during conduction of the intrinsic body diode of Si and SiC MOSFET devices and needs to be removed during hard commutation of the body diode. The amount of charge generated depends on internal device properties like doping profiles, thickness of the drift layer or carrier lifetimes as well as on external conditions controlled by the application such as current density, temperature or the conducting time of the body diode. The part of this charge that does not recombine during the body diode commutation must be removed by the reverse-recovery current and represents the reverse-recovery charge.

In the case of the CoolMOS CFD7 technology, the amount of stored charge was significantly reduced by a factor of 10 over the standard CoolMOS technology. Still, the stored charge Q_{RR} remains too large to allow the direct use of the device in the CCM Totem Pole PFC. This is very different for the SiC MOSFET. Being a wide bandgap device, the drift region thickness required for the targeted blocking voltage is much smaller. Also the active area is clearly reduced compared to even the best Superjunction MOSFET. Due to the dramatically reduced volume of the drift region, the amount of stored charge in the device becomes significantly smaller, which is further supported by the short carrier lifetimes in SiC. A low stored-charge also supports an improved robustness in hard commutation, as the risk of a snap-off at high reverse-recovery currents is much lower.

Fig. 17 compares the reverse-recovery waveforms of all three technologies, clearly indicating the much higher stored charge within the CoolMOS device, although a 50 % lower forward current was running through the device. The CoolGaN part does not actually generate any reverse-recovery charge because the device does not contain an intrinsic bipolar diode. As discussed before, the structure conducts in the third quadrant due to an open channel. Consequently, the “reverse-recovery” current here is purely capacitive and driven solely by the output charge of the device. This is also valid for the IGBT accompanied by the SiC Schottky diode. Being a unipolar device, the SiC Schottky device

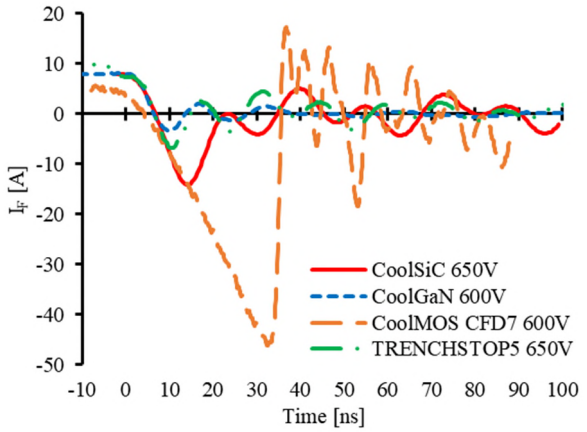

Fig. 17: Comparison of reverse-recovery current waveforms

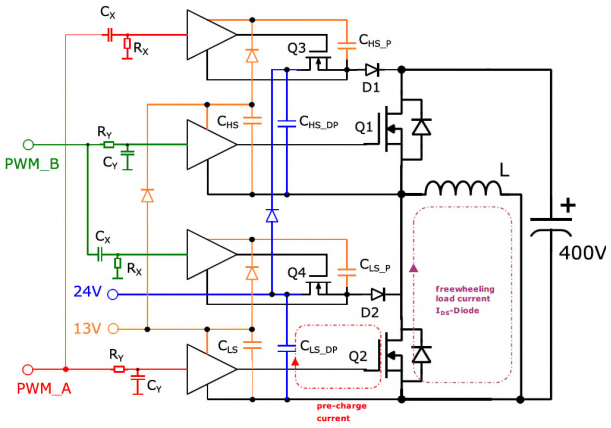

Fig. 18: Schematic of the pre-charging circuitry for the use of CoolMOS devices in a half-bridge configuration [15]

does not build-up a bipolar charge and commutation losses are again related only to the output charge, explaining the lower Q_{RR} of the SiC MOSFET.

PRE-CHARGING OF THE SJ DEVICE

It is not possible to use SJ MOSFETs in a half-bridge configuration in CCM operation due to the high output charge Q_{OSS} and the significant reverse recovery losses of the intrinsic body diode. There are several proposals that try to tackle this issue [13,14], but these solutions suffer from the use of extra switches and magnetics which limit the performance and power density.
However, the output capacitance and output charge characteristics of the SJ device as shown in Fig. 13 and Fig. 14 indicate that the major part of the linked losses are generated within a relatively small voltage range. If the output capacitance could be pre-charged to this respective voltage level, for example to 24 V, the commutation losses due to the output charge Q_{OSS} and reverse recovery charge Q_{RR} would dramatically reduce.

[15] describes such a solution that avoids the utilization of additional inductors and instead provides the previously discussed current into the switching node from a low-voltage source. This approach pre-charges the output capacitance of the SJ device operating in diode mode to a certain level. This enables the use of the SJ MOSFET in the Totem Pole PFC with normal CCM operation.
Fig. 18 depicts this implementation within a common half-bridge solution that reflects the situation in the Totem Pole PFC operating in CCM mode with hard commutation of the body diode. This pre-charge solution requires one high-voltage Schottky diode (D1, D2) and a low-voltage (LV) MOSFET (Q3, Q4) per device in the half-bridge and two separate supply voltages to drive the LV-MOSFET and provide the pre-charge voltage. This solution implements a level-shifting technique using bootstrap capacitors with traditional drivers for both the driver power supply (highlighted in orange) and the depletion voltage (highlighted in blue). The additional filter networks at the driver inputs, provided by C_X-R_X and C_Y-R_Y, allow the proper timing of the PWM signals to both the half-

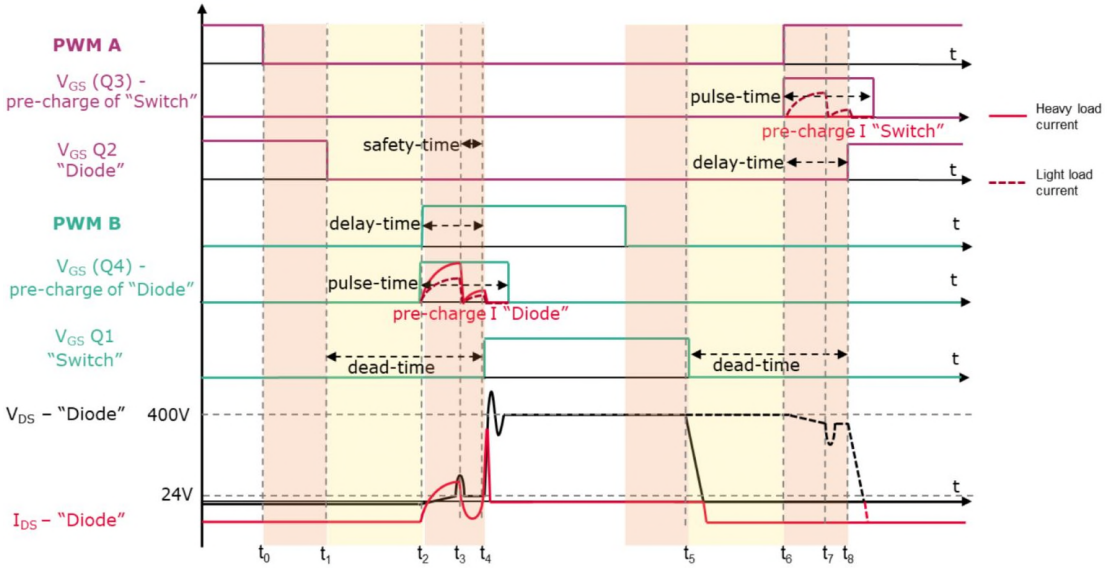

Fig. 19: Commutation waveforms of the pre-charge solution [15]

bridge devices and the added LV switches. This avoids the need for extra PWM control signals from the controller.

Fig. 19 shows the commutation waveforms of the pre-charge solution to indicate the intended effects of this approach. As can be seen, the C_X-R_X network at the input of the gate driver of Q4 generates a pulse that turns-on the pre-charging MOSFET Q4 at t_2. This results in a pre-charging current (I "Diode") circulating through Q2, Q4, D2 and C_{LS_DP}. At the end of the pre-charging period at t_3, the body diode of Q2 is deactivated and the drain-source-voltage of Q2 is pre-charged to 24 V. This sets the stage for a smooth diode-to-switch transition, avoiding the otherwise high losses due to Q_{OSS} and Q_{RR} as Q2 is already depleted to 24 V.

As depicted in Fig. 19, the pre-charge current has a second peak between t_3 and t_4 that originates in the resonance of the output capacitance with the stray inductances of the pre-charging loop. A detailed description of the hard-commutation transition and the design of the pre-charge circuit is found in [15].

EFFICIENCY COMPARISON

The performance of the different devices is evaluated in the PFC stage of 3.3 kW power supplies. For the purpose of this comparison, the SJ devices are used with a Dual Boost PFC stage whilst all other devices are used in a Totem Pole topology:

- CoolSiC Trench MOSFET with $R_{DS(on),typ}$ = 48 mΩ in a Totem Pole PFC
- CoolGaN E-mode HEMT with $R_{DS(on),typ}$ = 33 mΩ in a Totem Pole PFC
- CoolMOS CFD7 with $R_{DS(on),typ}$ = 37 mΩ pre-charged in a Totem-Pole PFC
- TRENCHSTOP 5 IGBT and SiC Schottky Diode with equivalent $R_{DS(on),typ}$ = 54 mΩ in a Totem Pole PFC
- CoolMOS P7 (2x) with $R_{DS(on),typ}$ = 26 mΩ in a Dual Boost PFC
- CoolMOS CFD7A with $R_{DS(on),typ}$ = 41 mΩ in a Classic Boost PFC

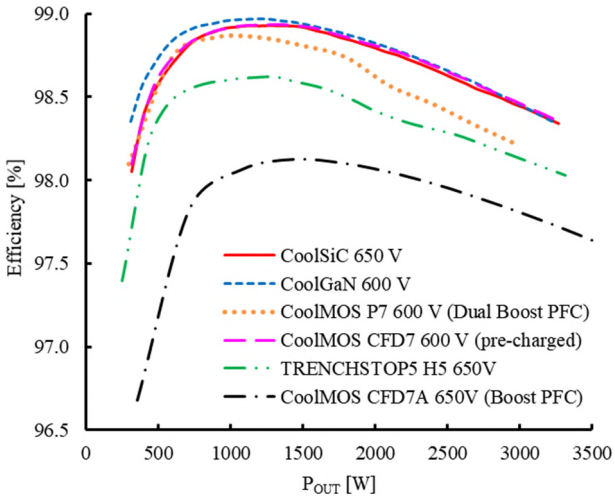

Fig. 20: Comparison of the absolute efficiency achievable in the respective 3.3 kW PFC stage (CoolSiC, CoolGaN, IGBT and pre-charged CoolMOS measured in Totem Pole topology, CoolMOS measured in Classic and Dual Boost topology, V_{IN} = 230 VAC, V_{OUT} = 400 VDC, f_{sw} = 45 – 65 kHz (Dual Boost PFC), f_{sw} = 65 kHz (Totem Pole & Classic Boost PFC))

The need to use different topologies for the different devices in combination with the need for varying gate drive schemes for MOSFET, IGBT and GaN devices makes a true performance comparison challenging. Consequently, the measurements were performed using different evaluation boards which introduces further uncertainties related to the different parasitic elements introduced by the different layouts.

However, the comparison shown in Fig. 20 reveals a clear trend of the capabilities of the different technologies. Both wide bandgap devices clearly enable higher efficiencies of around 99 % which is similar to the CoolMOS SJ device with pre-charging circuitry. The CoolGaN enables the highest peak efficiency but requires a significantly more complex driving scheme and hence more effort in the system design compared to the CoolSiC devices. The CoolMOS SJ device used in a Dual Boost configuration is capable of delivering a peak efficiency of 98.8 % but loses efficiency at high loads. The IGBT solution is capable of yielding a peak efficiency of almost 98.6 %, making this solution attractive for price-driven applications. In direct comparison with the efficiency delivered by a Classic Boost PFC representing the standard solution employed in most of today's power supplies, all alternatives offer a much better performance.

CONCLUSION

SJ devices in a standard boost PFC will remain the first choice for the PFC stage of a SMPS with an overall efficiency below 97 %. The devices are easy to drive, offer the most granular portfolio and offer a proven quality and reliability. Due to the higher output capacitance shape at V_{DS} > 20 V, wide bandgap devices do not offer clear advantages in this topology.

SiC MOSFET, GaN HEMT and pre-charged SJ MOSFET offer comparable solutions for SMPS with standard form factor and an efficiency range of 97 % to 98 %. This better efficiency is linked to the move to a Totem Pole topology and the elimination of the bridge rectifiers. The use of SJ devices in a Dual Boost PFC falls behind those solutions in terms of efficiency.

Although C_{OSS}, Q_{OSS} and E_{OSS} are all higher than for a GaN transistor, the SiC device clearly benefits from a much lower increase of on-resistance with temperature. The SiC MOSFET is easy to drive although it is recommended to use a gate drive voltage of 18 V to benefit from the further lowered $R_{DS(on)}$. SiC MOSFET are especially beneficial for high power applications. However, the application of a pre-charge circuitry with SJ devices could currently offer a more cost efficient solution for power levels beyond 3 kW.

The combination of a fast IGBT and a SiC Schottky diode enables the use of IGBTs in the Totem Pole topology. This approach offers the best solution for cost-driven applications whilst still delivering peak efficiencies clearly beyond 98 %.
Solutions using GaN devices are currently capable of delivering the highest efficiencies, exceeding 98 % in standard form factor. They are the first choice for high frequency applications where the form factor is the key requirement. However, GaN solutions use a dedicated gate drive concept that requires additional effort for its implementation.

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A Simulation study of 6.5kV Gate Controlled Diode

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Abstract

Gate Controlled Diode (GCD) with micro-pattern trench structure, allows charge carrier modulation at the anode region by gate control. This is utilized to operate the diode at low saturation mode and desaturate the diode before IGBT turn-on, to achieve a better trade-off. The paper demonstrates the concept of a silicon bi-polar power diode with micro-pattern trench gate, for 6.5 kV applications. Thereby, a detailed study of switching behaviour and the switching pattern were conducted, so as to reduce the overall switching loss and improve the efficiency. The efficiency also depends on the robustness of the diode, several issues concerning the reverse recovery robustness of the Gate controlled diode were investigated.

Keywords: Gate Controlled Diode, micro-pattern trench, 'tdsat', desaturation

Introduction

The advancement in the processing technology has led to the development of micro-pattern trench (MPT) cell structures. The capability to achieve low on-state voltage and a better dynamic performance of MPT IGBT's [1, 2], has increased the speed and efficiency of high voltage power converters. To comprehend such fast-switching applications and increase the power quality of the overall system, a robust high performance controllable diode is necessary.

Several controllable silicon power diodes have been published, such as MOS controlled diode (MCD) [3], diode with controlled emitter efficiency [4], Anode controlled diode (ACD) [5]. However, they require pre-triggering to avoid short circuit or have turn-off robustness issues due to possible electron injection during open nchannel operation. In this paper a silicon high voltage diode based on the micro-pattern trench gate cell structure, is proposed.

The aim is to realize a diode for 6.5 kV HVDC and traction applications, with good controllability, and which has a low conduction loss and low switching loss. A numerical device level simulation of Gate controlled diode (GCD) is demonstrated in this paper, using Sentaurus TCAD.

Gate Controlled Diode Structure and Principle

The concept of the Gate controlled diode with MPT cell structures, is to use the high carrier confinement of the MPT cell design to achieve a low on-state voltage drop [1]. The vertical charge carrier profile realized by MPT cell design, enables highly controlled stored charge removal during diode turnoff [2], leading to low switching loss and better trade-off behaviour.

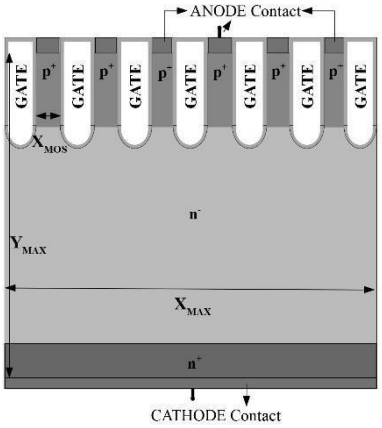

Fig. 1. Schematic cross-section of Gate controlled diode (GCD), with micro-pattern trench gate structures.

A schematic cross section of the Gate controlled diode (GCD) is shown in Fig. 1. The diode is based on PiN configuration with MPT cell structure on the anode side. The MPT cell structure and gate for the

diode were realized based on literature [2]. A 6 µm (X_{MAX}) wide MPT structure was designed with a mesa width of 0.4 µm (X_{MOS}) and a carefully selected mesa width to cell pitch ratio [6]. A 2.5 µm thick p^+ anode region with a doping concentration of 5e16 cm^{-3} was realised into the sub-µm mesas between the trench gate. A very thin highly doped p^+ layer was formed near the anode contact to make the region low ohmic. A 0.5 µm n^+ cathode layer of doping density 5e17 cm^{-3} was diffused into the n^- intrinsic base region. The thickness (Y_{MAX}) of the model and doping concentration of the base region was designed to handle a reverse blocking voltage of 6.5 kV.

Depending on the operation of GCD, a high injection of charge carriers can be achieved to lower conduction loss or have a controlled plasma density reduction, to lower the switching loss. This is possible by charge carrier modulation at the anode region, achieved from varying gate potential. When negative potential is applied, strong injection of holes leads to high plasma density. When a positive voltage is applied, an electron channel is developed around the oxide region which reduces the hole density from the anode side.

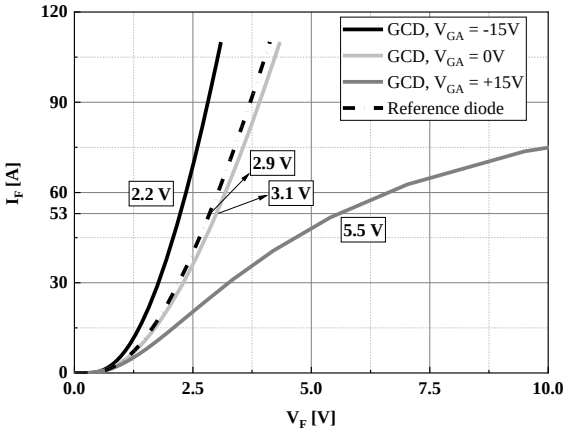

Fig. 2. Static I-V characteristics of GCD compared with reference diode. I_{nom} = 53A, T = 150 °C.

Static I-V characteristics of GCD is shown in Fig.2, where the diode is simulated for a nominal current (I_{nom}) of 53 A at 150 °C. The simulation model is designed to have active gate control over all the MPT gate structures and they are driven with respect to anode potential (V_{GA}). Compared to the I-V characteristics of the reference diode in Fig. 2, GCD operating with V_{GA} = -15V has a low on-state voltage drop (2.2 V at nominal current) due to high plasma density on the anode side, achieved by strong hole injection. The strong hole density during V_{GA} = -15 V is reduced, when the biasing to the gate is removed and the diode behaves as a simple PiN diode with reduced charge carriers at the anode side. This behaviour of plasma distribution when V_{GA} = 0 V is shown in Fig.3, along with plasma density curves from V_{GA} = -15 V, +15 V, +5 V, +30 V. Furthermore, positive gate voltages reduce the plasma density on the anode side further down. This reduced plasma at V_{GA} = +15V, results in a higher voltage drop across the diode (5.6 V at nominal current).

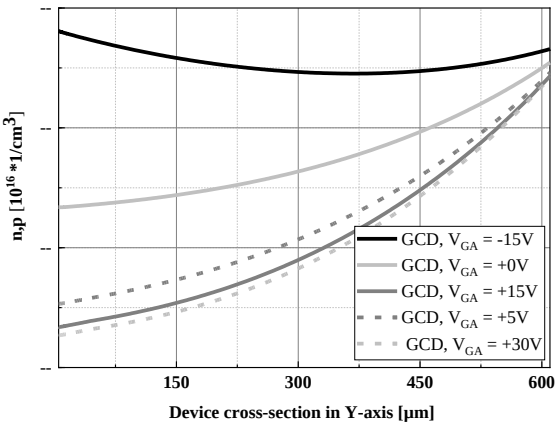

Fig. 3. Plasma denisty across the cross-section of GCD for corresponding Gate potenials from Fig. 2. under static condition. I_{nom} = 53A, T = 150 °C.

Switching control and Trade-off

It is observed from Fig. 2 and 3 that the operating point of the device changes with gate bias. The effect of changing plasma density due to change in applied gate potential can be used to desaturate the plasma density during GCD's turn-off. This reduces reverse recovery charge and switching losses, improving the overall efficiency of the system.

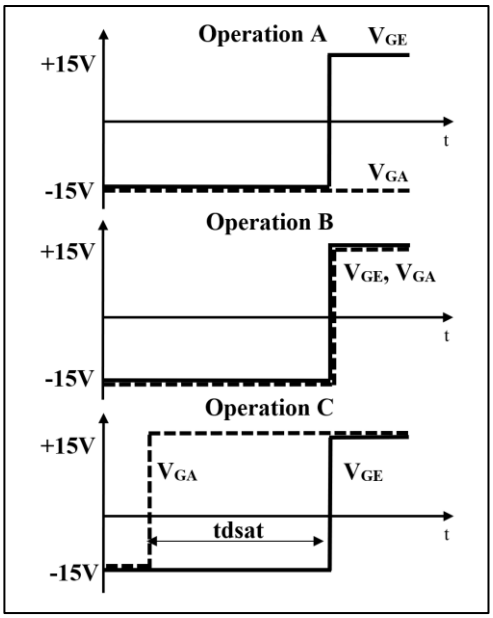

Fig. 4. GCD and IGBT, gate drive operations.

In order to understand the control that can be achieved by the gate, three driving conditions of V_{GA} are considered, as in Fig. 4. Operation A describes a constant V_{GA} of -15V on the GCD. Operation B, simultaneous switching of both the diode and the IGBT from -15V to +15V. Operation C shows switching of GCD (V_{GA} = -15V to +15V) before the IGBT, with a time difference 'tdsat'. The simulations were performed for a nominal current of 53 A, a DC-link voltage of 3.6 kV and at a temperature of 150 °C. A 6.5 kV MPT-IGBT, similar to a model scaled from [2], with half the current density as of the diode is considered. For the traction application standards, the simulations were performed with a boundary condition of reverse recovery peak power (P_{RR}) 150 kW and the circuit inductance (L_S) of 1.6µH in accordance with L_{stray}*I_{nom}.

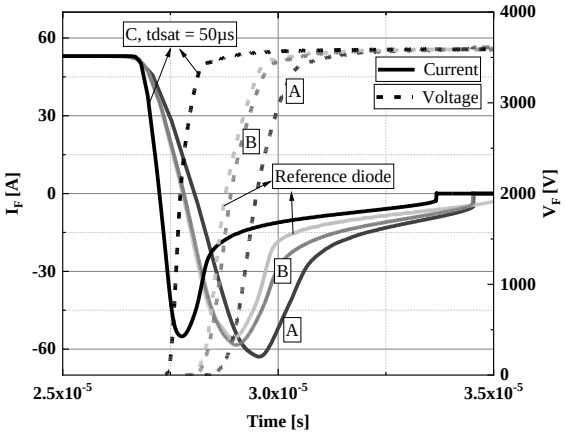

Fig. 5. Transient I-V characteristics of GCD during switching operations described by A, B, C. V_{DC} = 3.6 kV, I_{nom} = 53A, T = 150 °C, L_S = 1.6µH, P_{RR} = 150 kW.

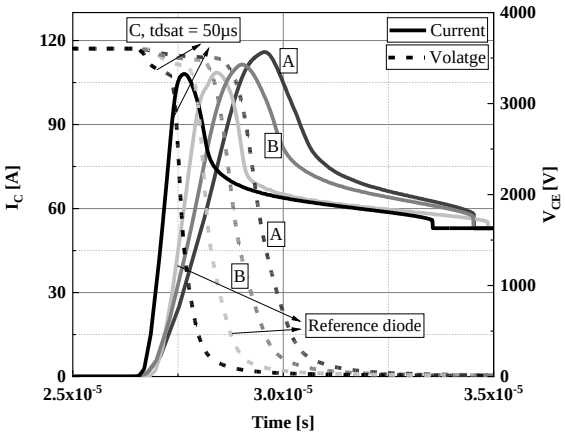

Fig. 6. Transient I-V characteristics of MPT-IGBT during switching operations described by A, B, C. V_{DC} = 3.6 kV, I_{nom} = 53A, T = 150 °C, L_S = 1.6µH, P_{RR} = 150 kW.

Fig. 5 and 6 show the transient I-V behaviour of GCD and IGBT switching during the above described operations A, B and C with 'tdsat' = 50µs. Operation A, with a constant V_{GA} = -15V has the slowest dI_F/dt and highest switching loss, because of high stored charge in the diode. Only a small amount of charge reduction takes place by simultaneous switching of GCD and IGBT during Operation B. GCD has slightly high reverse recovery charge than the reference diode, because of high plasma density of GCD at V_{GA} = -15V. Due to fixed peak $P_{RR,}$ the additional charge carriers left in the diode slows the dI/dt of IGBT during Operation B, when compared with the reference diode.

'tdsat', the switching time between upper side IGBT and lower side GCD, has a great influence on switching loss. In this paper, different diode 'tdsat' times 5µs, 20 µs, 50 µs and 100 µs are investigated. From Operation B, it is noted that simultaneous switching is not advantageous so the IGBT is switched after GCD as in Operation C. Since changing V_{GA} from -15 V to +15 V reduces device plasma, GCD utilises the time 'tdsat' to desaturate plasma [3, 7, 8]. Rate of desaturation varies in accordance with stored charge.

Fig. 7 shows the removal of charge carriers from GCD during Operation C, with a 'tdsat' of 50µs. As observed, the total switching time to completely remove the charge carriers of the GCD is 60 µs. For the first 50 µs, the GCD desaturates and is driven into reduced plasma state by V_{GA} = +15V while the IGBT is still in the blocking mode. The IGBT is turned on at 50 µs and the GCD starts taking up the voltage. Due to the reduced plasma after 50µs the reverse recovery charge that needs to be removed becomes low. For a fixed peak P_{RR} and L_{stray}*I_{nom} of the diode, steep dI_F/dt is observed with I_{RRM} remaining similar to I_{RRM} of the reference diode.

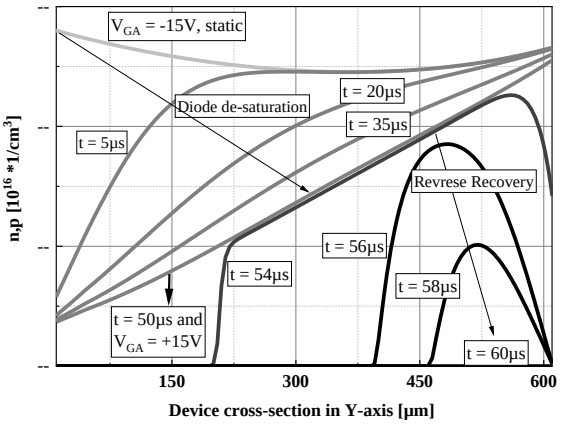

Fig. 7. Plasma density distribution across the cross-section of GCD, during the transient Operation C, with 'tdsat' of 50 µs. V_{DC} = 3.6 kV, I_{nom} = 53A, T = 150 °C, L_S = 1.6µH, P_{RR} = 150 kW.

Fig. 8 compares the influence of different 'tdsat' (0 to 100µs) to turn-on switching loss, distinguishing the GCD's reverse recovery loss (E_{RR}), IGBT's turn-on loss (E_{ON}) and the desaturation loss occurred during 'tdsat' (E_{dsat}). In addition, total switching loss of the reference diode is also shown at the specified nominal current density. It is observed for a longer 'tdsat', the reverse recovery loss and the IGBT turn-on loss reduces, reducing the total turn-on loss. Although a small amount of desaturation loss exists with 50 µs and 100 µs, when compared to the total reduction it is a small number.

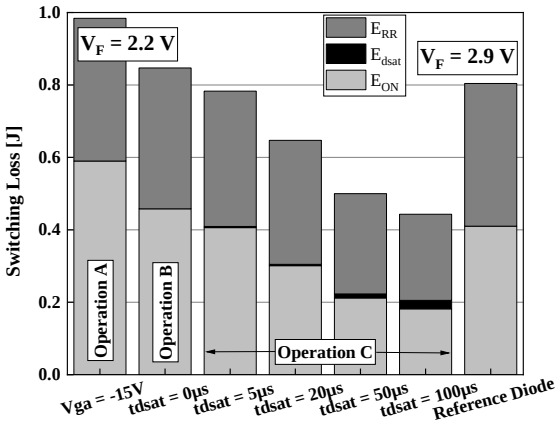

Fig. 8. Overall switching Energy loss comparison, distinguishing GCD's E_{RR}, E_{dsat} and E_{ON} for Operations A, B and C for 'tdsat'= 5µs, 20µs, 50µs, 100µs. V_{DC} = 3.6 kV, I_{nom} = 53A, T = 150 °C, L_S = 1.6µH, P_{RR} = 150 kW.

Table 1 shows the comparison of loss reduction achieved by influence of 'tdsat' in Operation B and C, when compared with Operation A i.e., GCD at a constant V_{GA} = -15V during switching. In case of 'tdsat' 50 µs and 100 µs respectively, a 50% and 55% of overall turn-on loss reduction is observed for a given peak reverse recovery power.

tdsat [µs]	$R_{GON-IGBT}$ [Ω]	% Reduction in E_{RR}	% Reduction in E_{ON}	% Reduction in E_{TOTAL}
0	25	1.3	22.4	13.9
5	23	5.1	31.2	20.4
20	17	13.1	49.0	34.2
50	12	29.7	64.1	49.2
100	9	39.6	69.2	55.0

Table 1. Percentage energy loss reduction of Operations B and C when compared with Operation A.

A 50 % loss reduction obtained from longer 'tdsat' promises a significant improvement in the efficiency of the converter. For traction applications with 400 Hz switching frequency or HVDC application with 150 Hz switching frequency, the 100µs 'tdsat' lies well within the limit. As long as the 'tdsat' time is no longer than the applied pulse width, the PWM rectifiers and inverters should be capable of driving such a switching sequence.

The influence of 'tdsat' and changing diode current are investigated in order to understand the GCD's behaviour in different operating conditions. Fig. 9 gives a total turn-on energy loss comparison of GCD during Operation C for varying 'tdsat', I_F, temperature. It is to be noted that, for a low current range, diode reverse recovery loss dominates the total turn-on loss from Fig. 9 a. Fig. 9 b, for I_F of 2 I_{nom} the energy loss distribution indicates that GCD with 'tdsat' of 50µs gives the best loss reduction. Even though the reverse recovery loss of GCD reduces with 100µs, the desaturation loss increases significantly. This is due to the high voltage drop (55 V) across the GCD at V_{GA} = +15V with 2 I_{nom}. The diode operates at a high saturation phase because of very high minority carriers at cathode side for such high current densities. Fig. 9 c, gives the variation in switching energy loss at 25 °C and 150 °C, it is observed for decreasing temperature the diode reverse loss decreases and IGBT loss increases.

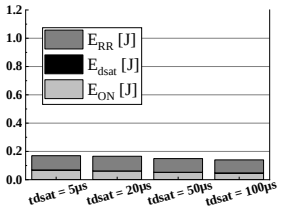

Fig. 9 a. I_F = **0.1 I_{nom},** T = 150 °C

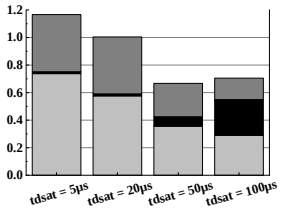

Fig. 9 b. I_F = **2 I_{nom},** T = 150 °C

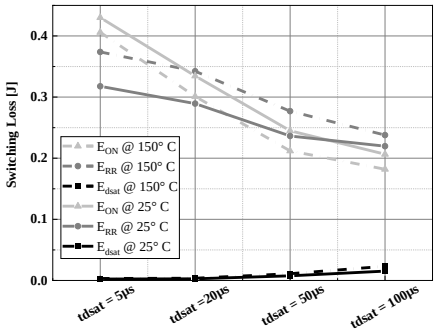

Fig. 9 c. I_F = **1 I_{nom},** T = 25 °C and 150 °C

Fig. 9. Overall switching Energy loss comparison, distinguishing GCD's E_{RR}, E_{dsat} and E_{ON} for changing,'tdsat'= 5µs, 20µs, 50µs, 100µs, I_F = 5A, 53A, 106A and T = 25 °C and 150 °C. V_{DC} = 3.6 kV, L_S = 1.6µH.

Fig. 10 and 11 compares dI_F/dt of GCD with reverse recovery charge, Q_{RR} and turn-on loss, E_{ON} of the IGBT for varying 'tdsat' and currents. For different 'tdsat', $R_{GON-IGBT}$ are varied as in the Table 1. With

increasing 'tdsat' it is observed the dI_F/dt gets steeper and the turn-on loss of IGBT and reverse recovery GCD gets smaller. The effect of I_{nom} and $2I_{nom}$ on Q_{RR} appears to be minimal, whereas the IGBT turn-on loss increase is significant with changing I_F.

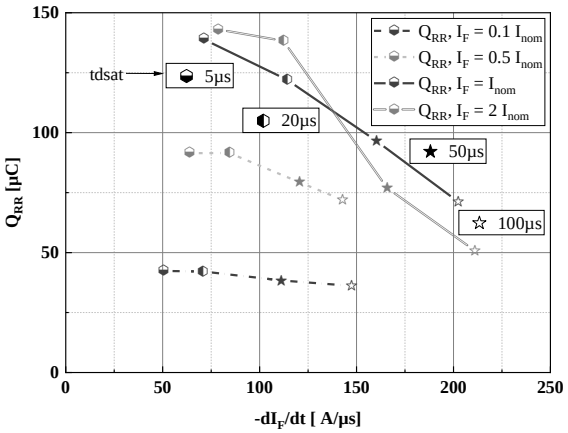

Fig. 10. Comparison of change in slope of diode current - dI_F/dt to the reverse recovery charge Q_{RR} of GCD for changing, 'tdsat'= 5µs, 20µs, 50µs, 100µs, I_F = 5A, 26A, 53A, 106A, V_{DC} = 3.6 kV, T = 150 °C, L_S = 1.6µH.

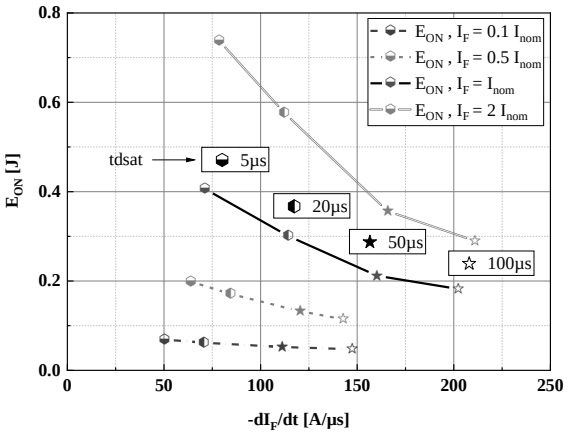

Fig. 11. Comparison of change in slope of diode current - dI_F/dt to the MPT-IGBT turn-on loss E_{ON} of GCD, for changing 'tdsat'= 5µs, 20µs, 50µs, 100µs and changing diode current, I_F = 5A, 26A, 53A, 106A, V_{DC} = 3.6 kV, T = 150 °C, L_S = 1.6µH.

Reverse Recovery Robustness

The Blocking Voltage. The GCD was designed to block a reverse voltage of 6.5 kV. Fig. 12 shows the simulation of static blocking condition of the diode at V_{GA} = -15V and V_{GA} = +15 V at 150 °C. In both the cases, the device shows a blocking capability up to 6.5 kV. At negative gate voltage, the leakage current appears to be low; during positive gate potential, the device shows marginally higher leakage current. To achieve a low on-state voltage, a higher n^+ cathode doping concentration was used for the GCD. To reduce the leakage current, the cathode efficiency may be optimised.

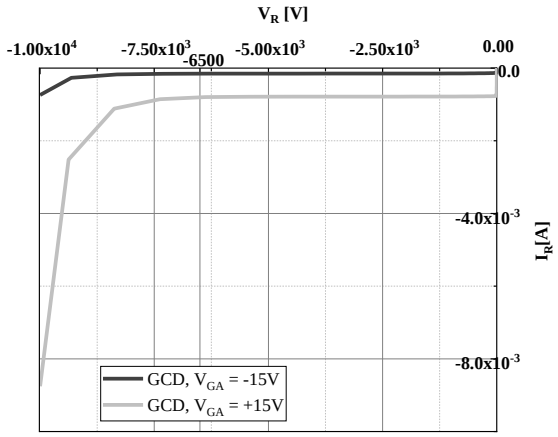

Fig. 12. Static blocking simulation, 6.5kV GCD, T = 150 °C.

Investigation of possible electron injection. The punch through of the device must be investigated at high reverse current densities to study the possible electron injection from the anode contact, when the electron channel is active at V_{GA} = +15 V. The influence of electric field upon reaching the contact may induce an electron current from anode into the substrate which is an undesired effect. To simulate such an induced scenario, a work-around structure was designed as shown in Fig. 13. The main design modifications were highly doped p^+ layer fused at the cathode alongside the n^+ cathode. Two separate contact terminals provided for the p^+ and n^+ layer to bias the p-n junction. Anode ohmic contact was changed to Schottky contact. A high reverse blocking voltage of 50 kV was applied to the work-around structure under static condition, with a positive voltage to bias the p-n junction and the avalanche parameter was de-activated

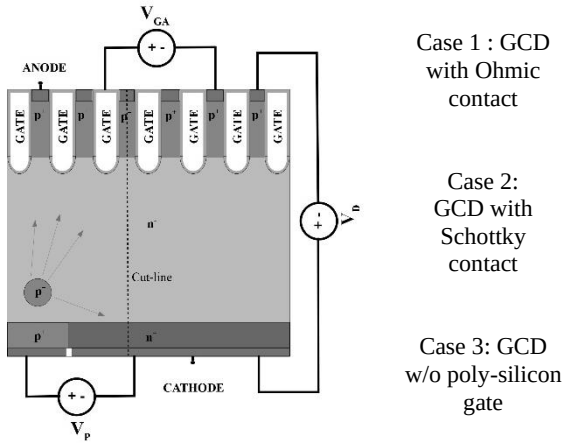

Fig. 13. Work-around structure of GCD to simulate possible electron injection. V_{GA} = +15V, V_D = 50 kV, V_P = 1.7V, de-activated avalanche parameter.

Three different cases of work around GCD structures were simulated. Case 1, GCD with normal anode ohmic contact. Case 2, GCD with Schottky anode contact. Case 3, the same structure with Schottky anode contact and micro-pattern trenches filled only with oxide to de-activate gate control. It is observed from Fig. 14, that the electric field doesn't reach the anode contact in case 1 and 2, with active MPT gate structures. Whereas in case 3, electric field reaches the anode contact and punch through is observed at a voltage of 1 kV as shown in Fig. 15, with increase in electron current (I_{eR}) and hole current (I_{pR}).

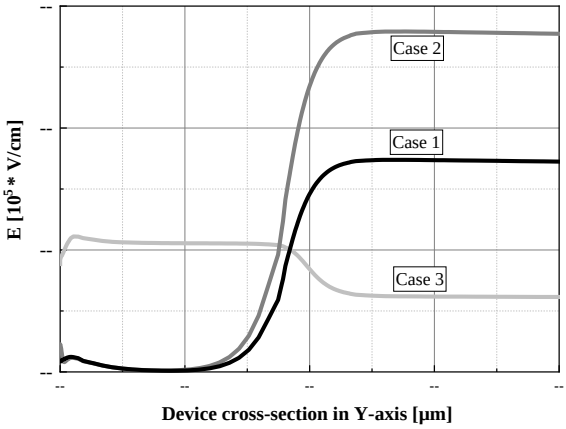

Fig. 14. Electric field distribution across the cross-section of the device (partial cross-section of the structure is shown). V_{GA} = +15V, V_D = 50 kV, V_P = 1.7V, de-activated avalanche parameter.

Fig. 15 shows the simulation of static I-V behaviour of the work around structures in case 1, 2, 3. As seen, a high hole current (I_{pR}) is flowing to the anode contact due to additional injection from p^+ layer at high reverse blocking voltage of 50 kV and a V_{GA} of +15V, without the avalanche generation. During cases 1 and 2, punch through of device is not observed due to field shielding effect provided by micro-pattern trench structure and device shows negligible electron current. This shows no electron injection from the anode contact and demonstrates a robust anode side of GCD structure.

Investigation of Cathode side Dynamic Avalanche and Softness. Typically, soft reverse recovery behaviour is observed from Fig. 5, at nominal current 53 A and DC link voltage of 3.6 kV, during Operation C. When GCD (at V_{GA} = -15V) is at high plasma density state, a short-circuit type IV leads to high carrier concentration on both sides of the diode. Specifically, the minority charge carriers at the back side of the diode leads to a high electric filed and a cathode side avalanche. This may lead to double side fed current filaments on both sides of

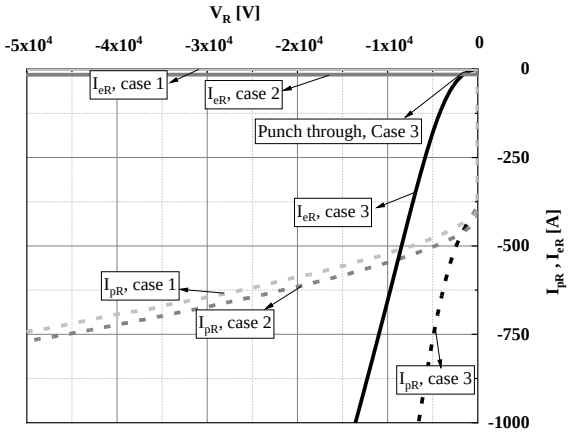

Fig. 15. Static reverse I-V simulation of GCD at high blocking voltage from Fig. 12. V_D = 50 kV, V_P = 1.7V, de-activated avalanche parameter.

the GCD. Furthermore, at 0.1 I_{nom} and lower temperature, the diode shows a snappy reverse recovery behaviour.

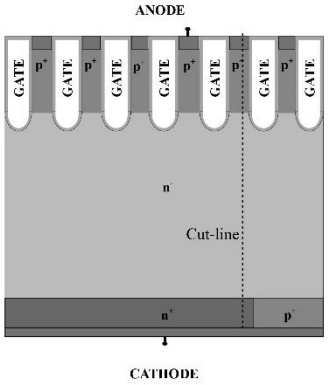

Fig. 16. GCD w/ p^+ shorts at cathode.

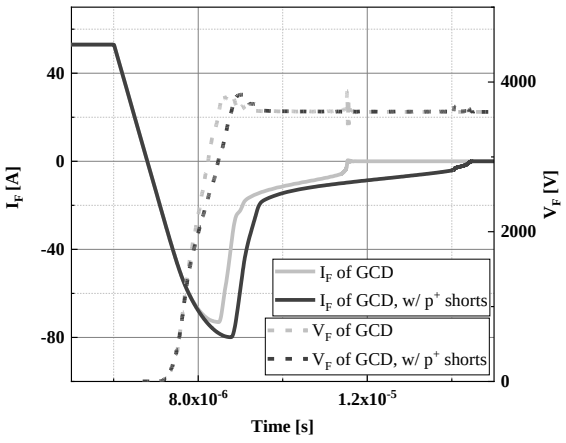

Fig. 17. Transient I-V characteristics of GCD and GCD w/ p^+ short, during short-circuit type IV. L_{SC} = 52 µH, L_S = 1.6 µH, V_{DC} = 3.6 kV, I_{nom} = 53A, T = 150 °C.

To avoid snappy recovery and cathode side dynamic avalanche, an addition of high doped p^+ short at cathode terminal is considered, similar to Field Charge Extraction (FCE) diode [9]. Fig. 16, depicts

a GCD with p^+ shorts at the cathode side. The n^+ cathode and p^+ short is electrically connected to each other. Simulations were based on wide (large X_{MAX}) model, to obtain inhomogeneous plasma distribution across the width of the diode. The short-circuit type IV simulations were performed at 3.6 kV DC-link voltage and I_F of 53A at 150 °C. The short-circuit inductance (L_{SC}) of 52µH, was chosen to have a similar dI_F/dt as during a normal switching.

The p^+ short provides an additional injection of holes, which delays the removal of minority carriers in the region. This slows down the depletion and avoiding a huge space charge region being formed, reducing the electric field and hence the dynamic avalanche on the cathode side. Additional hole current from p^+ short adds to the reverse recovery current and softens the tail current which can observed from Fig. 17.

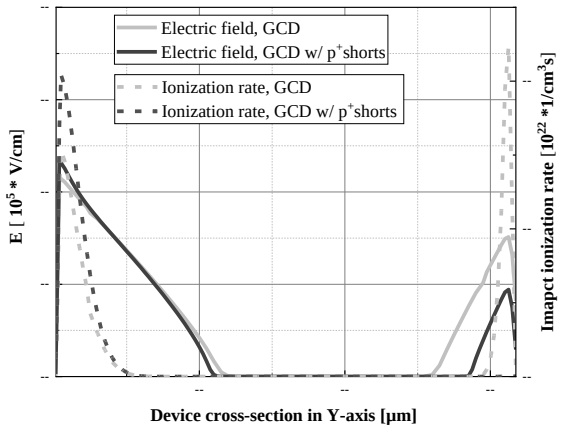

Fig. 18. Electric field distribution and Impact ionization rate distributed across the cross-section of the GCD and GCD w/ p^+ short. L_{SC} = 52 µH, L_S = 1.6 µH, V_{DC} = 3.6 kV, I_{nom} = 53A, T = 150 °C.

Fig. 18. shows the distribution of Electric field and Impact ionization rate, during short-circuit type IV. High electric field is observed on both sides, in the case of GCD. The GCD with p^+ shorts show decreased electric field on cathode side. The impact ionization shown in the figure depicts, no dynamic avalanche on the cathode side of GCD with p^+ short. The disadvantage of this modified structure would be additional reverse recovery charge which increases the losses, and also increased front side dynamic avalanche.

Conclusion

A Gate controllable diode concept is proposed based on the micro-pattern trench gate design. The simulation results of GCD MPT diode with an efficient control allows two operating points of the GCD, a low on-state voltage mode (V_{GA} = -15V) for diode conduction and a moderately high saturation mode (V_{GA} = +15V), used to de-saturate the diode during switching. The GCD showed a significant improvement over the reference diode of same class, with 25% reduction in conduction loss and 40% to 60% reduction in switching loss after an effective desaturation achieved by gate control.

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DEGRADATION OF POWER SIC MOSFET Under REPETITIVE UIS and SHORT CIRCUIT STRESS

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Abstract

This paper investigates the reliability of commercial planar and trench 1.2-kV 4H-SiC MOFSETs under repetitive unclamped inductive switching (UIS) and short circuit (SC) stresses. The degradation of device characteristics, including the transfer characteristics, drain leakage current Idss, and output characteristics, is observed. Repetitive SC stress was performed for 400 and 600 V bus voltages. Increased buss voltages during stress have higher impact on electrical performance of tested devices. The hot carriers injection and trapping into the gate oxide in the channel region may occur during the aging experiments and are believed to be responsible for the variation of electrical parameters.

Keywords: Reliability, degradation, SiC MOSFET, TrenchMOSFET, repetitive UIS, repetitive short circuit

INTRODUCTION

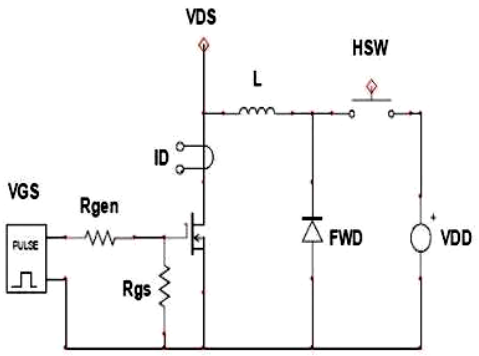
Silicon Carbide (SiC) power MOSFET fabrication technology has considerably matured over the recent years and therefore, they are now commercially available to buy in large quantities from various different manufacturers [1]. Because of their superior properties, SiC devices can be used for higher temperature, higher switching frequency, and higher power density applications [2-3]. Nevertheless, before they could completely replace silicon (Si) counterparts, robustness and reliability remain a main issue [3-4] for the devices under a number of extreme operational conditions, such as overcurrent, overtemperature, short circuit, and unclamped inductive switching (UIS) [5]. With trend of decreasing chip size for cost reduction purpose, the avalanche robustness and short circuit withstand capability became more critical, as they are strongly sensitive to the chip size design as the maximum energy density of the chip is fixed. In UIS test, the MOSFET is usually connected to an inductance without antiparallel free-wheeling diode to commutate the loop current when switching OFF the device. As a consequence of this, the device has to absorb all the energy previously stored in the inductance during the operation stage. The MOSFET, therefore, will be driven into the avalanche mode as long as the stored energy is sufficiently high, resulting in a gradual increase in the junction temperature of the device [6]. During avalanche operation at high currents, high concentrations of hot carriers are generated that may cause degradation of interfaces and insulation (oxide) layers.

Due to the smaller chip size and thinner gate oxide, the robustness of SiC MOSFETs regarding the SC condition is lower than their Si counterpart. When comparing Si IGBTs and SiC MOSFETs with similar current ratings, SiC MOSFETs have 5-10 times higher current density under short circuit conditions. Higher instantaneous power density and smaller thermal capacitance results in faster temperature rise and lower short circuit withstand time. Because an undesirable SC fault may occur in a variety of ways during the lifetime of the devices and at least 2 μs is needed for the commercial drivers to react. However, due to external effects and oscilations, SC event may occur many times during operational lifetime, therefore, the repetitive SC tests could reflect the impact of a single SC event and also provide more insights about the degradation process [7-8]. With the aid of repetitive SC tests, aging indicators can be explored comprehensively.

Therefore, this paper investigates the reliability of commercial 1.2-kV 4H-SiC MOFSETs under repetitive unclamped inductive switching (UIS) and short circuit (SC) stresses. The degradation of device characteristics, including the transfer characteristics, drain leakage current I_{dss}, and output characteristics, is observed.

EXPERIMENTAL SETUP

For all tests, two types of commercially available 1.2kV SiC MOSFET devices were used. The first samples were transistors with planar gate and on-resistance of 100mΩ. Second samples were devices with the trench gate



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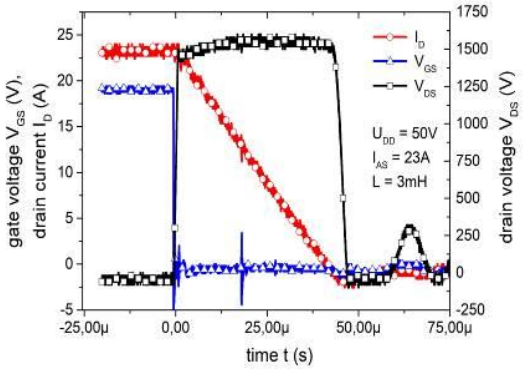


(b)

Fig. 1a) Basic UIS test circuit. b) Typical current and voltage waveforms ***of*** *SiC MOSFET* under UIS test conditions.c) Typical current and voltage waveforms ***of*** *SiC MOSFET* under SC conditions

structure and 200 mΩ of on-resistance. Both devices were packaged in TO247. **UIS test** – Commercial UIS tester ITC55100 was used for UIS testing. The circuit diagram and typical voltage and current waveforms during the test for Si MOSFET are shown in Figure 1a-b. The device under test (DUT) is connected to the power supply through the inductor and high side switch HSW. When HSW is shorted and DUT is turned ON, the current limited by inductor starts to linearly rise. In the experiments, DUT and HSW are turned off when the current I_D reaches the required (pre-set) value. The magnetic field in the inductor L induces a counter electromagnetic force (EMF) that can build up surprisingly high potentials across the switch (DUT). If no protective circuits are added to the switch, all the energy accumulated in the inductor is dissipated directly in the device switch. [9] Conditions set for the repetitive UIS stress measurements were: inductance L = 1mH, supply voltage V_{DD} = 100V, switched current I_{AS} = 15A. The switching period between two pulses was set to 5ms and an additional time of 800ms was set after every 100 pulses. Current and switching period was set with accordance to minimize heat accumulation in samples and maximum non-destructive single pulse current for given inductive load.

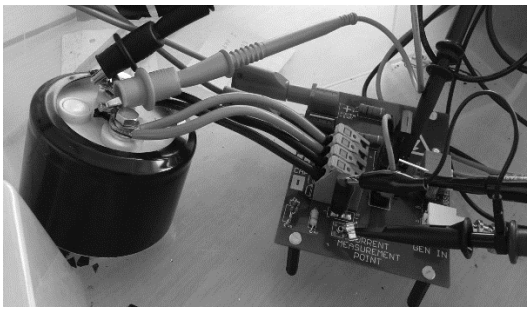
SC test – Short circuit measurements were done on the custom-built tester. Test parameters were defined for SC-I defined by JEDEC standards. Typical current and voltage waveforms during the short circuit test are shown in figure 2b. Test conditions were V_{DD}= 400/600V, SC pulse length t_P= 5us, time between pulses was set to t_T= 0.4s to prevent heat accumulation.

RESULTS - REPETITIVE UIS

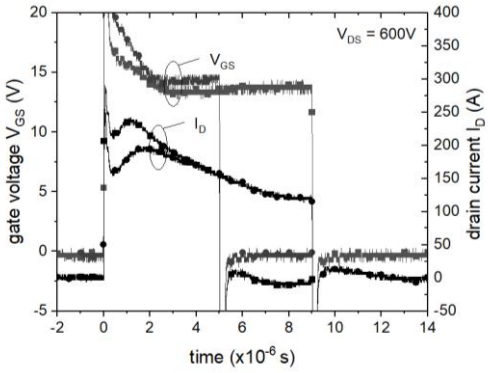
First single pulse UIS capability of tested devices was verified. Obtained values of destructive currents of TrenchMOS and planar devices measured for different inductances are shown in Figure 3. Observed results are in good agreement with basic UIS theory where if the intrinsic temperature of the blocking PN junction is assumed as a critical value for the passive mode of destruction and tests start at a constant temperature, then the relation between the inductance L and the critical value of avalanche current I_{Avcrit} can be written as [8]:

$$\Delta T_M = \frac{\sqrt{2}}{3} C_{th0} . I_{AV} . V_{B\,Reff} . \sqrt[2.2]{\frac{LI_{AV}}{V_{B\,Reff}}} \rightarrow$$

$$I_{AVcrit} \sim \sqrt[3.2]{\frac{1}{L}} \quad .$$



(a)



(b)

Fig. 2a) Custom built SC-I test board. b) Typical drain current and gate voltage waveforms of planar SiC MOSFET under SC conditions at 600V supply voltage, V_{GS} = 15 V and pulse lengths of t_p = 5 and 9 µs.

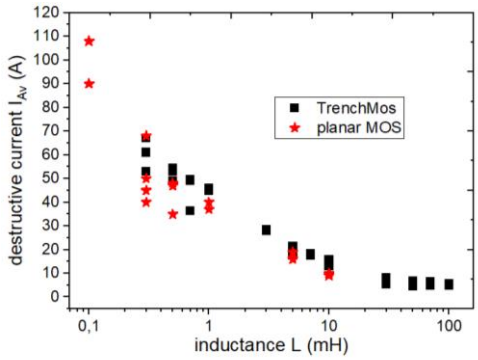
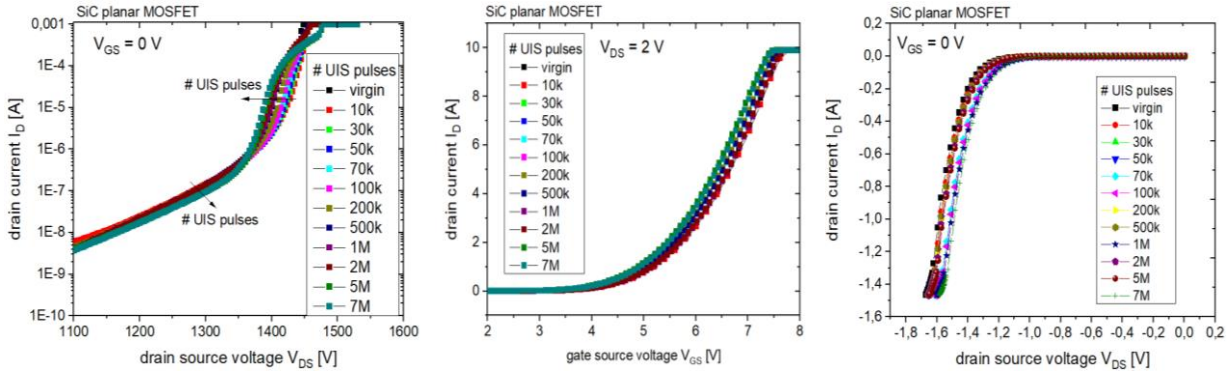


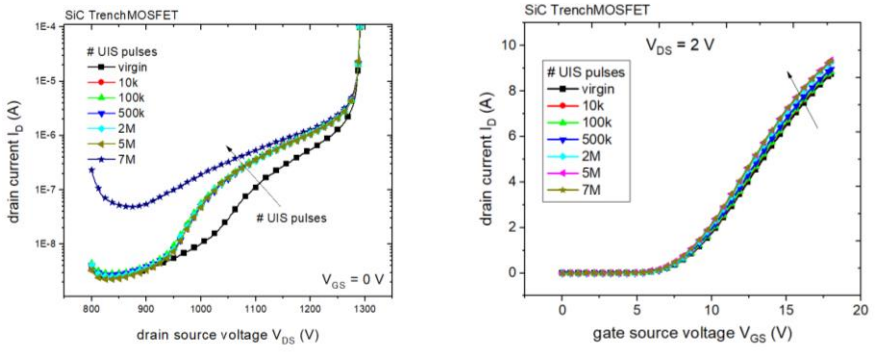
Fig. 3 Measured destructive currents of TrenchMOS samples for different inductive loads.

An interesting observation was that samples have very similar single pulse UIS capability, despite the fact that the active area of planar devices was more than 2 times larger than that of trench devices. Set conditions for the repetitive UIS stress measurements (L = 1mH, I_{AS} = 15A) were significantly lower than destructive currents for given inductance. Because during switching significant heat is generated in transistors, I-V measurements were performed after device cool down to prevent impact of temperature on device parameters shift. First, parameter shift induced by repetitive UIS was analysed on planar transistors. Measured I-V characteristics for virgin and stressed samples up to 7 million UIS pulses are shown in Figure 4. Observations were as follows: Repetitive UIS pulses induced shift all analyzed I-V curves. The shift in output, transfer, and diode characteristics was not uniform. However, after 7 million of stress pulses samples exhibit lower on-resistance RDSon than virgin samples, which can be attributed to change of threshold voltage VTH which decreased from a value of 3,13 V to a value of 2.87 V. It is a known fact that during the avalanching phase of UIS pulse, large concentrations of high energy carriers are generated close to blocking PN junction. The negative shift of threshold voltage, therefore, indicates the trapping of positive charge on the gate interface or in the gate dielectric. The origin of this positive charge can be attributed to high energy holes generated during UIS. The shift of diode characteristics indicates the presence of trapping effects also in the volume of the device on / close to blocking PN junction. Also, in this case, a decrease of diode threshold voltage indicates the trapping of the positive charge. Both effects, trapping on gate interfaces and in the volume, have a strong impact on the breakdown voltage of the device, which was most impacted. Due to repetitive UIS stress decrease of static breakdown voltage ΔBVDSS = -46 V was observed. Next, repetitive UIS was performed on samples with trench technology of the gate electrode. The impact of repetitive UIS on I-V characteristics is shown in Figure 5. Similar to a transistor with the planar gate electrode, the negative shift of threshold voltage was observed with the corresponding decrease of on-resistance. Indifference to the planar transistor, a significant increase of the drain



(a) (b) (c)

Fig. 4 planar SiC MOSFET - Measured impact of repetitive UIS on stability of electrical characteristics of planar SiC MOSFET. a) breakdown characteristic, b) Transfer characteristic, c) diode characteristics.



(a) (b)

Fig. 5 SiC TrenchMOSFET - Measured impact of repetitive UIS on stability of electrical characteristics. a) breakdown characteristic, b) Transfer characteristics.

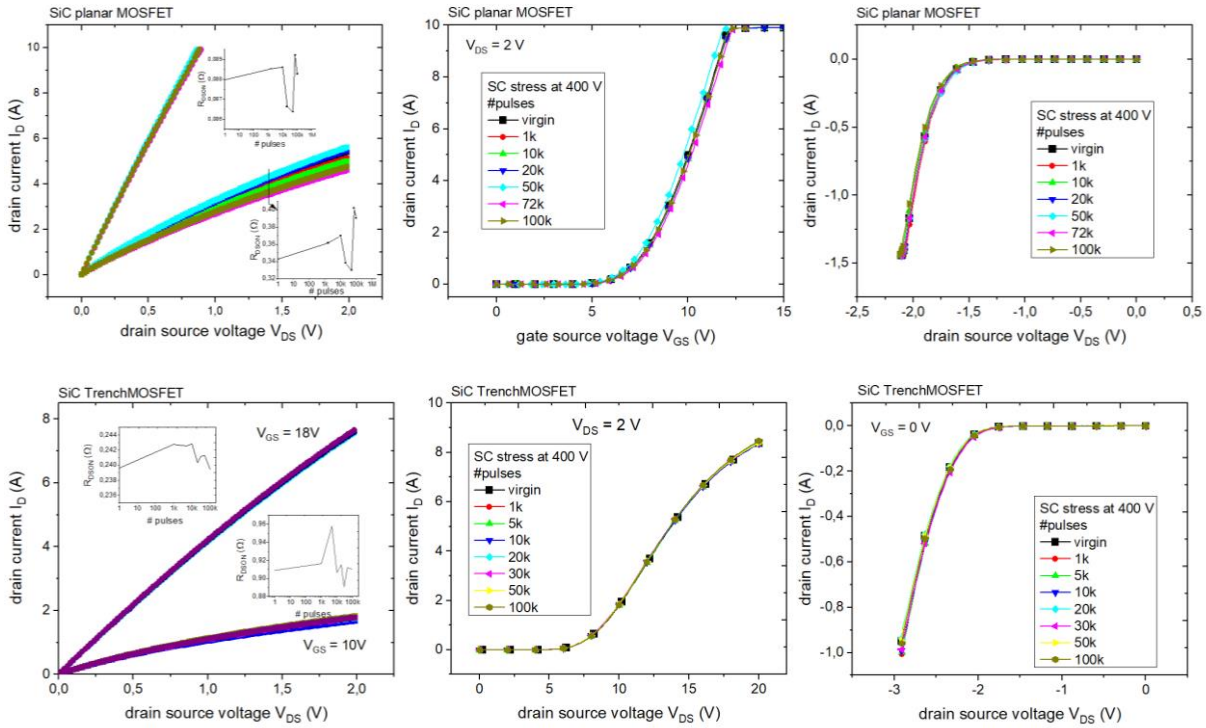


Fig. 6 Measured impact of repetitive SC stress on stability of electrical characteristics for buss voltage 400V for planar device (top) and TrenchMOSFET (bottom). Measured characteristics from left: output for V_{GS}= 10V and 18V, transfer characteristics for V_{DS} = 2V and antiparallel diode forward characteristics.

leakage current was observed (from 10 nA to 193 nA at V_{DS} = 1000V) and no impact on the breakdown voltage was observed.

RESULTS - REPETITIVE Short Circuit

Before repetitive SC experiments were performed it was necessary to determine maximum operating conditions for both trench and planar types of samples. TrenchMOS devices were capable to sustain short circuit pulses with pulse lengths of more than 20 µs at 600V bus voltage and VGS = 15 V. Planar devices performed worse. Most of the devices were able to sustain short circuit pulses in the range of 10 - 12 µs at 600V bus voltage. Therefore, the length of short circuit pulses was set to 5 µs for both types of samples. Repetitive short circuit experiments were performed at two buss voltages 400 V and 600 V. In Figure 6 are compared I-V characteristics for trench and planar MOSFET obtained from experiments performed at 400V bus voltage. The only very small impact of repetitive SC stress at 400V on output, transfer, and diode characteristics was observed for TrenchMOSFET. In the case of the planar device, a small shift of threshold voltage was observed and associated shift of on-resistance and shift of output characteristics. First, on-resistance was increasing for the first 10k pulses, the next a significant decrease down to 96% of the original value was observed after 50k of stress pulses. After the next 30k pulses on-resistance significantly raised to 114% of the original value.

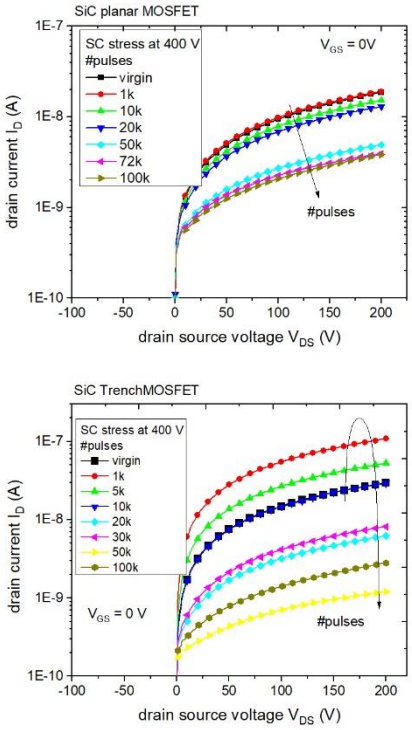


Fig. 7 Impact of repetitive SC stress at 400V on leakage current of planar and trench MOSFET device.

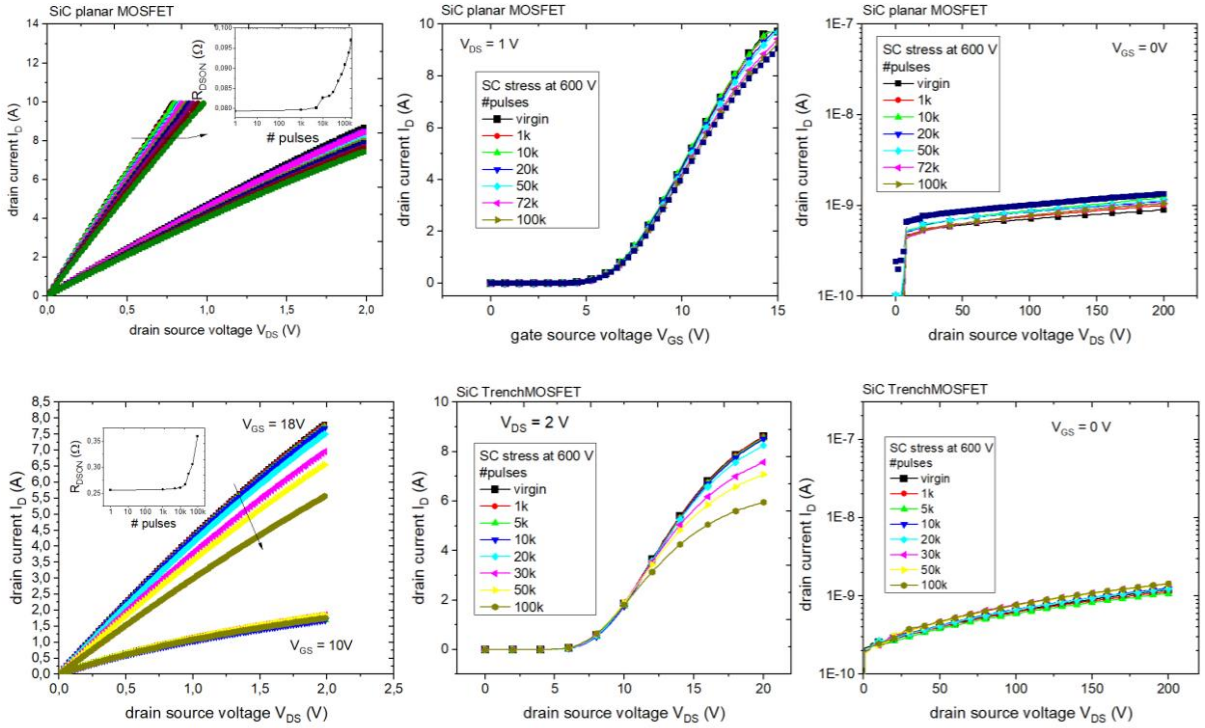


Fig. 8 Measured impact of repetitive SC stress on stability of electrical characteristics for buss voltage 600V for planar device (top) and TrenchMOSFET (bottom). Measured characteristics from left: output for V_{GS}= 10V and 18V, transfer characteristics for V_{DS} = 2V and drain leakage current characteristics.

This nonuniformity in changes indicates that at least two degradation mechanisms are present with the opposite effect on threshold voltage and on-resistance. Also, significant impact of SC stress was observed on leakage current (Fig. 7) in both devices. First, the leakage current was increasing with a number of stress pulses. For planar MOSFET this increase saturated after 1k of stress pulses and for devices with trench gate structure, increase saturated after 10k of stress pulses. After that leakage current was decreasing and after 100k of stress pulses its value was more than one magnitude lower than for virgin sample.

The next impact of repetitive SC stress at 600V was analyzed. Fresh devices were used for this analysis. Results are shown in Figure 8. At first glance, we can state that SC stress at 600V has a more significant impact on the performance of both devices especially on the threshold voltage and on the on-resistance of devices. A positive shift of threshold voltage ΔV_{TH} = +0.2 V was observed for planar devices. For TrenchMOSFETs threshold voltage was increasing for the first 10k pulses (ΔV_{TH} = +0.1 V) and then it was decreasing. After 30k it reached the initial value and next after 100k pulses it was 0,2 V lower than the initial value. A Uniform increase of on-resistance was observed for both devices. It was increasing first slowly for the first 10k pulses and the next dramatic increase was observed. After 100k pulses on resistance increased by 23,5% in the planar device and by 38,5% in TrenchMOS device. Surprisingly SC stress at 600 V had minimal impact on leakage current, and similar to stress at 400V small impact on diode characteristics was observed.

CONCLUSION

The degradation of commercial planar and trench gate 1,2 kV 4H-SiC MOSFETs subjected to the repetitive avalanche and short circuit pulses is investigated in this paper. ITC55100 UIS tester and custom-built SC tester are utilized to generate the stress. The strong impact of both stresses on the electrical performance of tested devices was observed. After repetitive UIS stress test devices show an almost consistent degradation tendency characterized by the decrease of Vth, an increase of RDSON, and leakage current. Moreover, a significant decrease in breakdown voltage was observed for planar devices. SC stress was performed at two bus voltages 400 and 600 volts. For SC stress performed at 400V, only a small impact on the electrical performance of TrenchMOSFET was observed, while a small increase of on-resistance was observed for planar devices. Stress at 400 V had a strong impact on drain leakage current. For SC tests performed at 600V significant increase of RDSon with the increase in the number of stress pulses was observed for both devices. TrenchMOSFET performs worst than the planar device at 600 V stress. A significant increase of on-resistance (38,5%) of TrenchMOSFET was measured after 100k stress pulses.

This may be caused by the lower maturity of trench technology on SiC. It is believed that the main impact on the variation of the electrical characteristics and parameters have hot carriers injection and attributed trapping and traps generation in the gate oxide and/or at the channel interfaces.

ACKNOWLEDGEMENTS

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Degradation of 600V GaN HEMTs under Repetitive Short Circuit Conditions

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Abstract

This paper describes impact of repetitive short-circuit stress on commercially available 600V e-mode GaN HEMTs with p-GaN gate. The devices were subjected to up to 10^5 short circuit stress cycles at 100V and 300V drain voltage. Tests at voltages over 300V resulted in destruction of the devices. Electrical characteristics were measured prior to, and after each sequence of pulses to observe gradual effects of repetitive SC stress. The devices were also analysed by DLTS. A shift in all of the measured characteristics was observed. Amount of the shift does not correlate with the number of SC cycles, which suggests more parameters of the devices are affected. The shifts were also more pronounced at higher drain voltage. The trapping was also analysed using DLTS. Due to high complexity of the spectra, only the traps verified by simulation were investigated. At 100V stress voltage, the shift in DLTS spectra was small, at 200V it was significant. Full analysis of possible origin of the observed deep levels is still ongoing.

Keywords: GaN HEMT, repetitive short circuit, DLTS, degradation

INTRODUCTION

Gallium nitride high-electron mobility transistors (GaN HEMT) are one of the most promising technologies for future medium-power, high-efficiency semiconductor switches. However, to completely replace silicon power MOSFETs, they need to be able to withstand the harsh conditions that occur in real-world switching applications. One of the most commonly occurring extreme conditions is the type-I short circuit or hard-switching fault, a turn-on event of a switch that is experiencing a shorted complementary switch (Fig. 1a). In this condition the transistor is subjected to high drain-source voltage (V_{DS}) and current (I_D) simultaneously. Such stress can result in degradation or destruction of the transistor due to high amount of energy delivered to the device. Although GaN HEMTs exhibit good performance in standard operating conditions, their behaviour and reliability under extreme stress needs to be thoroughly analysed. Short-circuit (SC) behaviour of e-mode GaN HEMTs has been already adressed by researchers, mostly focused on destructive tests without analysis of impacts of repetitive non-destructive SC stress [1, 2]. Degradation after repetitive SC test was addressed e.g. by [3] who observed that repetitive SC stress results in channel and gate structure parameter changes, which lead to reduction of conductivity. Gate threshold voltage is also affected. The elevated temperature of the device during a SC event seems to be the trigger of the degradation. According to [4], in repetitive SC tests, local temperature fluctuates between room temperature and a high value, generating strong mechanical stress during the thermal expansion and contraction phases. Physical cracks are formed in the structure due to the high temperature spike and local temperature fluctuations in the GaN layer. However, there is not much research on how greater amounts (more than 10^4) non-destructive SC pulses at lower V_{DS} affect the transistor performance.

TEST EQUIPMENT

GaN HEMTs stand out among other power switching devices mainly due to exceptionally short switching time.

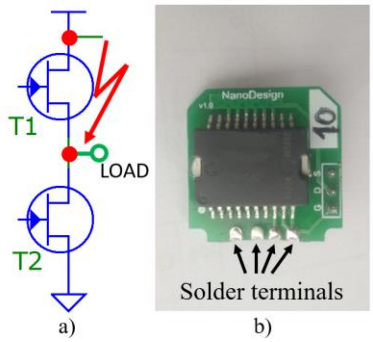

Fig. 1: a) Typical short circuit type I event. T2 turns on to shorted complementary transistor. b) Device under test soldered to a sample board.

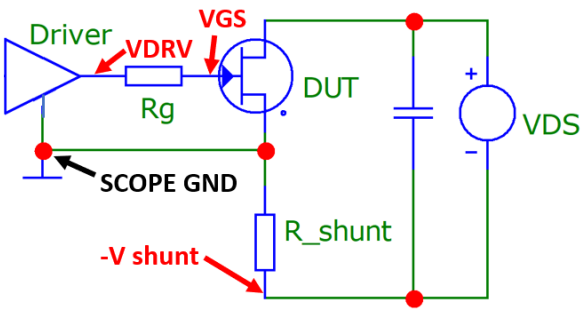

Fig. 2: Simplified schematic of the test setup.

To exploit this advantage effectively, circuit designers try to eliminate as much parasitic impedance as possible in gate-source loop and drain-source loop of the device [5]. To accurately simulate a real-world application, a custom tester device was designed and built. It consists of a main PCB fitted with high-voltage capacitor bank, gate driver, current-sense resistor and support circuits. A device under test (DUT) is soldered to another PCB, which is then soldered to the main board (Fig 1b). This soldered connection reduces the parasitic inductance and resistance to a greater extent than a connector, while the DUT can still be fitted and removed in a convenient manner. The PCB also features a Kelvin source contact to the gate driver. Figure 2 shows a simplified schematic of the tester. The main board is fitted with a gate driver IC optimized for driving GaN HEMTs. The gate voltage can be adjusted continuously from 4V to 12V between on-state and off-state levels. Negative off-state voltage is also supported. Input signal connector is optically isolated. Gate-source loop is only approx. 16mm^2 in area and can be fitted with a simple gate resistor or with a R-C network optimized for a rapid charge and discharge of a gate capacitance while preventing unnecessarily high steady-state current. This current is a consequence of the transistor gate diode structure. The drain-source capacitor bank is charged from an external DC power supply. It is rated up to 450V with a total capacitance 83µF and uses combination of ceramic and polypropylene capacitors capable of fast high-current discharge. This amount of capacitance is sufficient for GaN HEMTs with short-circuit saturation current up to 100A and 10µs pulse duration at higher V_{DS}. The decrease of capacitor voltage during the pulse is ~12V according to equation for constant current capacitor discharge:

$$v(t) = V_0 - \frac{i\,t}{C} \qquad (1)$$

The main board is fitted with a 10mΩ current-sense resistor in series between DUT source terminal and the capacitor bank negative terminal. In this configuration, current can be measured as a negative voltage drop across the resistor with an ordinary oscilloscope probe grounded at DUT source, a common ground terminal for all measured signals. In an event of a type-I short circuit in a well-designed real application circuit, turn-on drain current rise is steep, but turn-off V_{DS} overshot is relatively small due to reduced stray inductance.

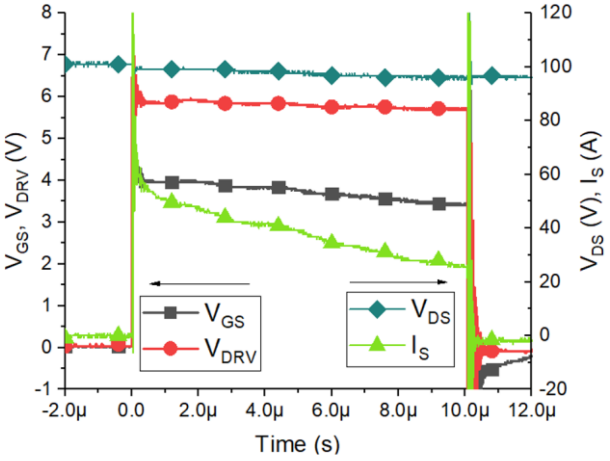

Fig. 3: Typical waveforms during short circuit. Gate voltage is limited by the transistor's gate diode to ~4V.

However, the overshot can still affect degradation of the DUT, particularly in repetitive tests. To eliminate this high-voltage stress affecting the test results, a typical high-speed gate-driving circuit has been substituted for a larger gate resistor that extends the turn-off time and reduces the voltage spike.

EXPERIMENTAL RESULTS

Sample transistors used for these experiments are commercially available enhancement-mode AlGaN/GaN HEMTs on Si substrate with p-GaN gate structure. Some of their key parameters are V_{DSmax} = 600V, on-resistance $R_{DS(on)max}$ = 70mΩ, max. pulsed current I_{Dmax} = 60A. At first, some samples were stressed at increasing voltages from 50V to 400V and pulse durations from 1µs to 10µs. Typical short circuit waveforms are shown in Fig. 3. Drain voltage over 300V often resulted in destruction of DUT (Fig. 4), in some cases even after the first SC pulse.

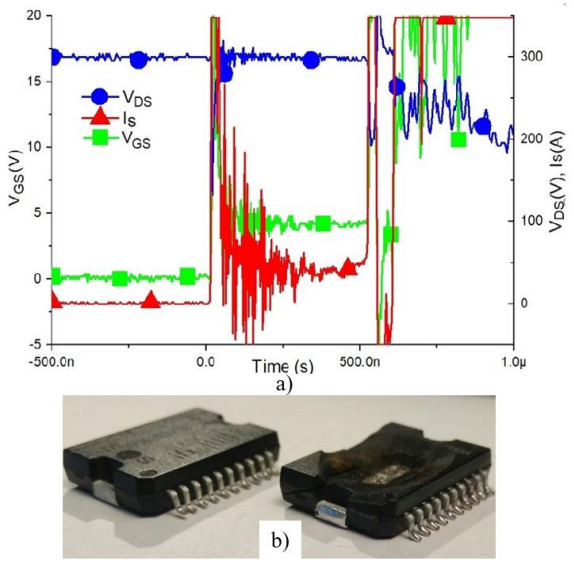

Fig. 4: a) Waveforms during device failure. b) Visible destruction of the transistor.

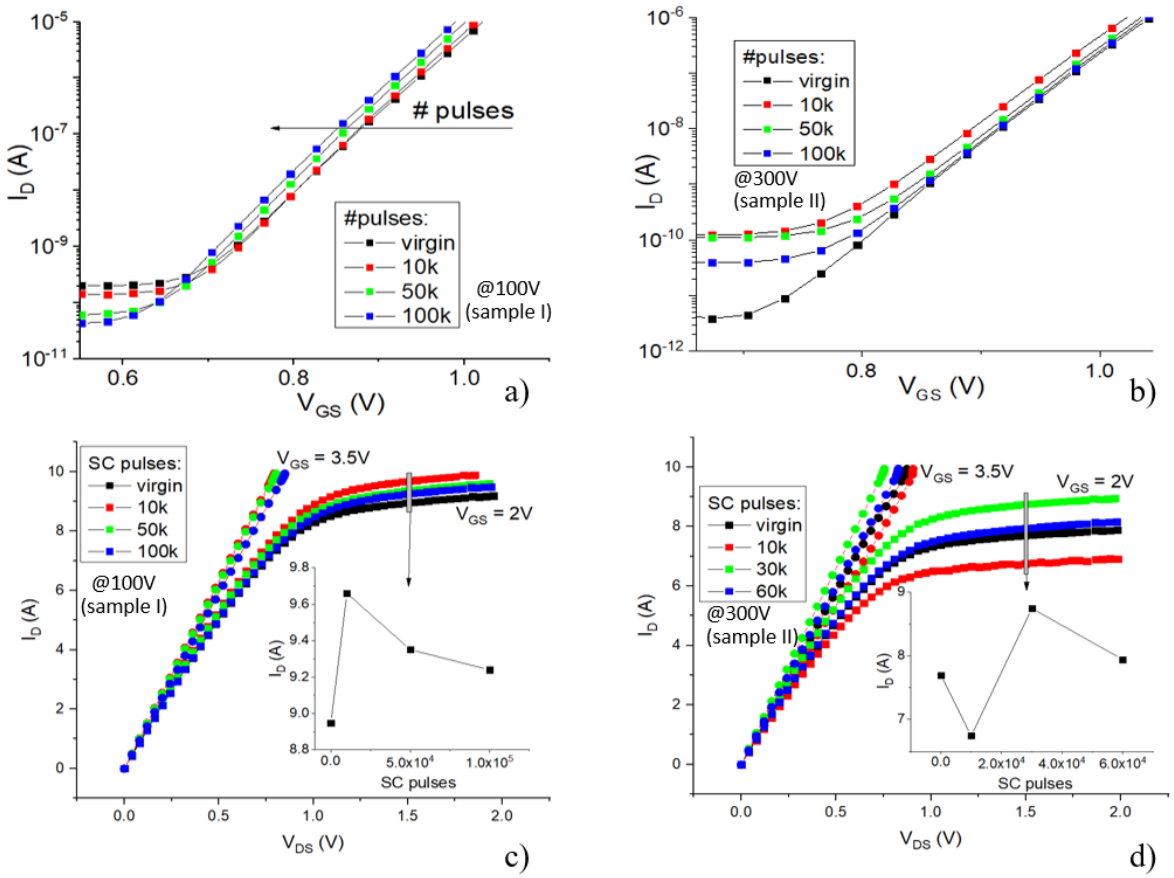

Fig. 5: Transfer and output characteristics measured after several sequences of SC pulses. a) Transfer at 100V. b) Transfer at 300V. c) Output at 100V. d) Output at 300V. Inset in c) and d) shows change of drain current at gate voltage VGS = 2V and VDS = 1.5V in relation to number of SC pulses While a) exhibits a decreasing trend in gate threshold voltage (V_{TH}), other data suggest that at least two device parameters are significantly affected by the test.

Therefore, the transistors were repetitively tested at V_{DS} up to 300V. Duration of the pulses was set to 2µs in all of the tests performed. The highest thermal stress occurs within this period [4]. To allow the structure to cool down between the repetitions, consecutive SC pulses were separated by 250ms period. The test was performed in several sequences of 10^3 to $5 \cdot 10^4$ pulses. Characteristics of the samples were measured on virgin samples and then after each sequence of pulses to observe gradual effects of repetitive SC stress. Although both were the same type devices, their initial characteristics varied observably, however this is common among current commercial GaN HEMTs. Repetitive SC stress had different effects depending on test voltage. Figure 5 a) and b) show a shift of transfer characteristics and gate threshold voltage (V_{TH}). Figure 5 c) and d) depict output characteristics with saturation current evidently affected. From measurements at different drain voltages it is clear that higher V_{DS} during stress is responsible for more significant shift of characteristics. However, uniform shift of characteristics was not observed. Based on previous studies, it is known that shift of characteristics is caused by trapping effects in AlGaN layer. Based on literature, three mechanisms apply during stress but not to the same extent. First charge trapping under gate electrode is responsible for threshold voltage shift [6]. Trapping in drain access region causes decrease of free charge in the 2DEG [7] and both trapping effects are decreasing mobility of carriers in the 2DEG [8] affecting on-resistance and saturation current. Drain leakage current ($I_{D(LEAK)}$) is strongly affected by the stress and in principal, is the main indicator of degradation and a critical parameter limiting the overall reliability of the element. At first, significant decrease of $I_{D(LEAK)}$ was observed, however after $4 \cdot 10^3$ stress pulses it increases again and after $4 \cdot 10^4$ pulses the leakage surpasses the virgin sample at V_{DS} from less than 100V (Fig. 6).

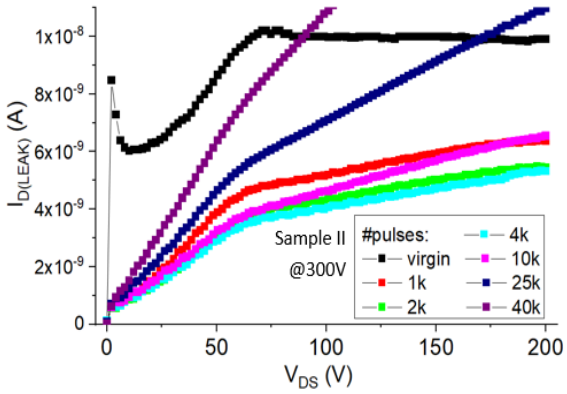

Fig. 6: Drain voltage dependence of drain leakage current $I_{D(LEAK)}$ at gate voltage V_{GS} = 0V. $I_{D(LEAK)}$ decreases up to 4000 pulses, then rapidly increases.

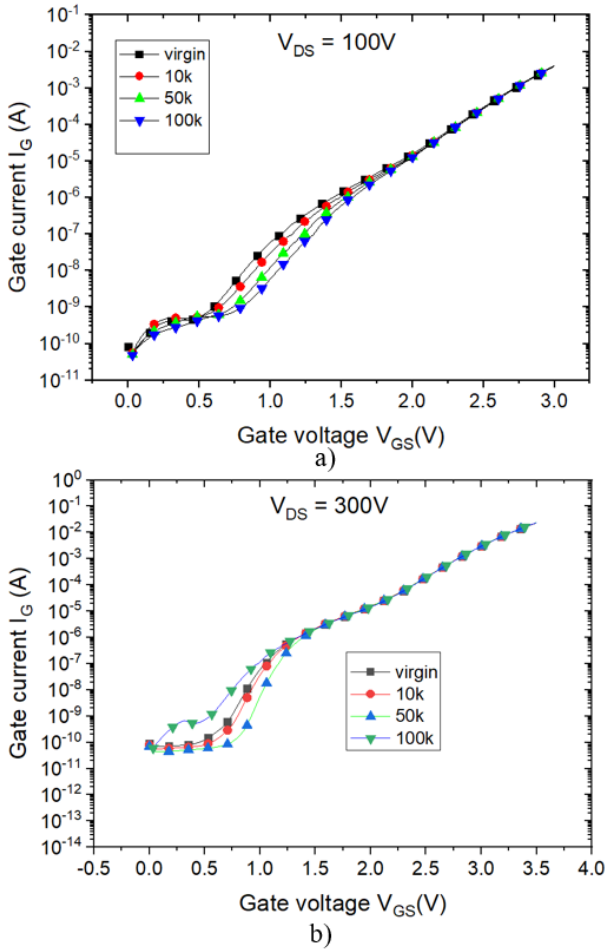

Fig. 7: Gate leakage current degradation. At 100V stress, there is an uniform trend, but more parameters are affected at 300V.

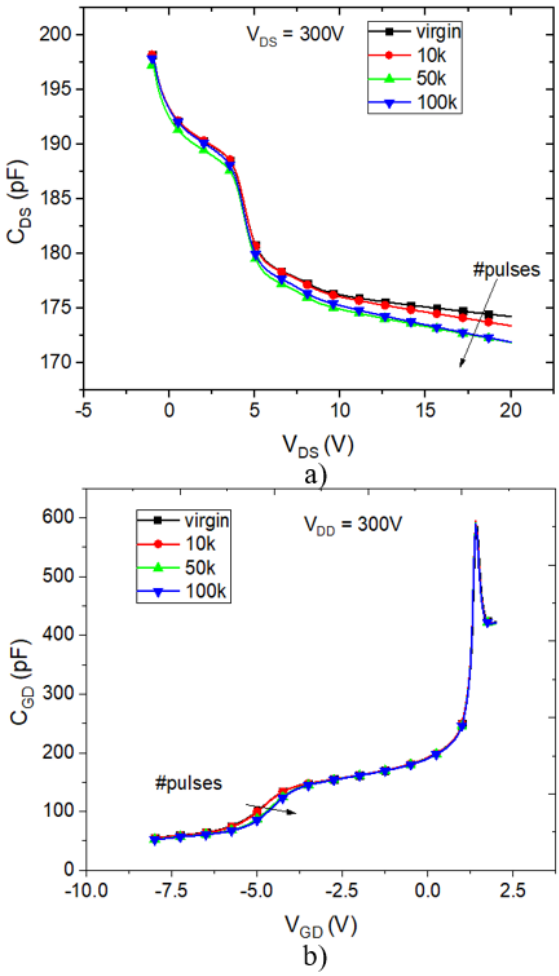

Fig. 8: Degradation of drain-to-source (C_{DS}) and gate-to-drain (C_{GD}) capacitances after 300V stress.

Gate leakage current $I_{G(LEAK)}$ degradation (Fig. 7) behaves in a similar manner as the transfer characteristics. At 100V stress voltage there is an decreasing trend of $I_{G(LEAK)}$ at gate voltages close to V_{TH}. However at V_{DS} = 300V there is no unequivocal trend, again suggesting different rate of degradation of at least two device parameters. Transistor capacitances were also ivestigated. The effect of 100V stress voltage on the capacitances was not significant. Degradation of drain-to-source (C_{DS}) and gate-to-drain (C_{GD}) capacitances after 300V stress are shown in Fig. 8. Both of them exhibit one-way shift, which is more pronounced in C_{DS} but only slightly visible in C_{GD}. Degradation of gate-to-source capacitance (V_{GS}) was negligible.

DLTS

To investigate possible generation of new traps, the DLTS spectra such as in Fig. 10 were measured on the virgin samples and compared to the spectra measured on the same samples after 10^5 SC stress cycles. First, several sets of measurements with various condition parameters were performed to map the distribution of the defects. The spectra were evaluated using the Fourier transform analysis by Direct auto Arrhenius Single and Multi-level evaluation and also by Tempscan maximum analysis [9].

Due to high complexity of obtained spectra it was difficult to evaluate parameters of all deep energy levels using the direct evaluation method. Therefore only traps that were verified by simulation and were present in most obtained spectra were evaluated. Positions of simulated DLTS peaks compared to measured spectra for both sets of measurement conditions are shown in Fig. 11. Parameters of 5 main evaluated traps are summarized in Table 1. Due to unknown active area of samples traps concentration was not evaluated. Analysis of possible origin of observed deep levels is still ongoing. Stated possible origins are first preliminary results. In Fig. 12 are shown DLTS spectra obtained on stressed samples for different stress conditions. First repetitive short circuit stress at 100 V was performed. Samples were exposed to 100k of stress pulses. Only small shift of DLTS spectra was observed, where small increase of signal for trap T1 dominated. Next gate stress was performed to analyse if shift of DLTS spectra is not induced by relatively high gate voltage present during stress pulses. From results it is clear that gate stress caused different shift of DLTS spectra. Signals of T1, T3 are decreased signalizing partial neutralization of this defects due to the stress.

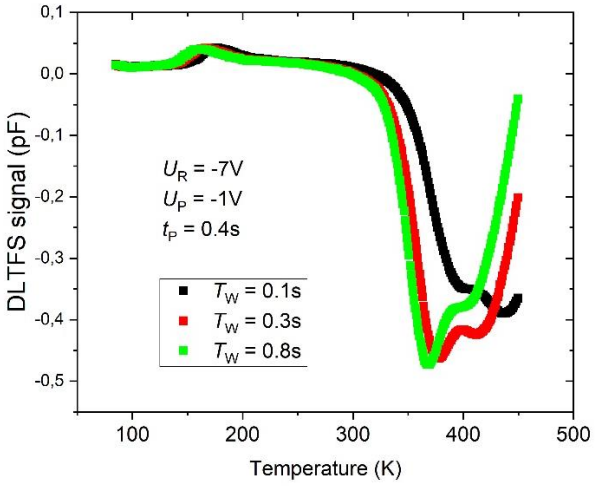

Fig. 10 Example of measured DLTS spectra of analysed sample of power HEMT before repetitive SC stress.

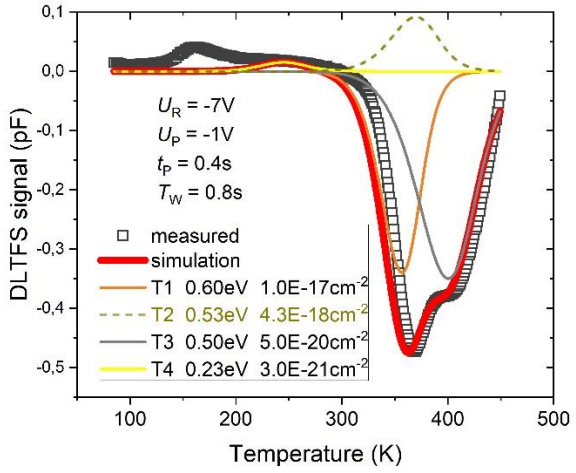

Fig. 11 Measured signals and simulated curves of DLTS defect states for selected measurement set.

Table 1: Parameters of observed deep levels

Trap	Activation energy ΔE_T (eV)	Capture cross section σ_T (cm^2)	Possible origin:
T1	0.6	1×10^{-17}	unknown
T2	Minority 0.53	4.3×10^{-18}	C_N deep acceptor states
T3	0.5	5×10^{-20}	Surface/interface states
T4	0.23	3×10^{-21}	Ga vacancy
T5	0.8	3.5×10^{-14}	GaN dislocations

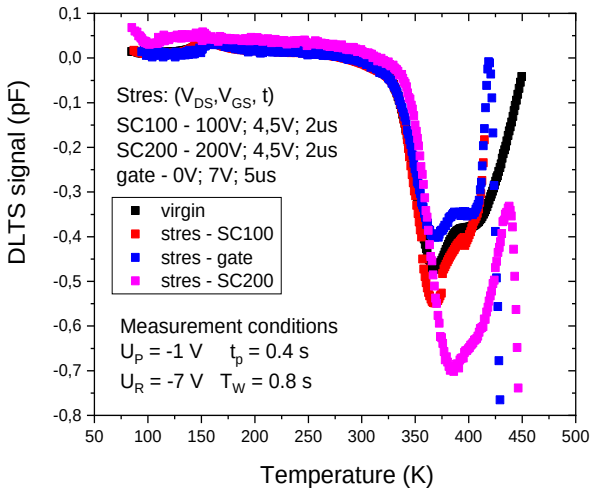

Fig. 12 Shift of DLTS spectra induced by different stress conditions

Finally, samples were exposed to repetitive SC stress at 200V. Significant shift of DLTS spectra was observed. Especially, signal of T1 and T2 traps was increased. Origin of trap T2 is believed to be C_N deep acceptor state (however, full analysis is still ongoing). These states are well known for their negative effects on dynamic on-resistance and current collapse phenomena [10]. Increase of T3, which origin may be in surface or interface states, may lead to decrease of carriers mobility in 2DEG and therefore has negative effect on device on-resistance and saturation current.

CONCLUSION

Gradual degradation of 600V GaN HEMT under repetitive SC stress was measured and analysed. Drain voltage above 300V (half of the nominal voltage) caused majority of tested devices to fail. At lower VDS measurable shift in device parameters and characteristics is observed. Higher stress voltage leads to higher degradation rate and more significant shifts of characteristics can be observed. However, particularly at higher stress voltage, shift of the characteristics does not have uniform character, pointing on at least three different mechanisms associated with generation of defects and trapping effects. The trapping was also analysed using DLTS. Due to high complexity of the spectra, only the traps verified by simulation were investigated. At 100V stress voltage, the shift in DLTS spectra was small, at 200V it was significant. The shift was verified not to originate from gate stress. Full analysis of possible origin of the observed deep levels is still ongoing.

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TCAD Simulation of the Bipolar Degradation in SiC MOSFET Power Devices

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Abstract

Reliability and performance of SiC high power devices are still limited by inherent SiC material defects despite tremendous progress made to reduce the density of these defects. The bipolar degradation remains a major challenge for developing high voltage SiC power devices. It is mainly due to the presence of Shockley-type stacking sequence faults (SFs) within the hexagonal SiC structure lattice, creating 3C-like SiC regions embedded within the main 4H-SiC structure. In this paper, we present a two dimensional numerical model of 4H-SiC power MOSFET device in which the drift region of the device is formed by a 4H-3C-4H heterojunction to account for the bipolar degradation. TCAD simulation results showed that the 3C- nano-layer creates a high resistive layer, effectively preventing the current flows across it, hence reducing the total active area of the device.

Keywords: Bipolar degradation, stacking faults, heterojunction, 3C- SiC.

INTRODUCTION

Reliability assessment of SiC power devices rely on a wide range of tests that have been developed and established during more than 30 years of experience on power packages with implemented Si device technology [1]. These tests are mostly performed to assess the chip quality such as High Temperature Reverse bias (HTRB) and High Temperature Gate bias (HTGB) stress tests, to assess the stability of the package in specified operating conditions and under external and internal temperature swings such as power cycling tests, and to assess the mechanical integrity of the package such as vibration tests. However, additional reliability tests have been specifically developed to account for SiC materials defects that direct impact the performance of power devices.

SiC material defects are broadly classified into two groups and they differently affect power devices performances: point defects and extended defects. The former are identified as a major carrier lifetime killer while the latter lead to excessive leakage current and significantly decrease the breakdown voltage of power devices if they include carrot/comet defects or triangular defects for instance [2]. On the other hand, basal plane defects, which are classified as extended defects, trigger the so-called bipolar degradation and are considered as the major defects hindering the commercial development of high power discrete devices rated above 1.7kV despite tremendous technological progresses achieved in SiC power devices fabrication and epitaxial growth to reduce these defects.

The bipolar degradation phenomenon has been observed for the first time during the research and development of SiC PiN diodes in the early 2000s [3]. Extensive experimental results have been published to explain this degradation mechanism in power devices operating in bipolar mode as PiN diodes, IGBTs and BJTs as well in unipolar SiC MOSFET power devices which are similarly affected by such degradation if their inherent body diode, working as a bipolar device, is intentionally or accidentally turned on [4, 5]. It has been reported that basal plane defects easily glide under stress because the critical resolved sheer stress is relatively low in SiC, leading to the formation of Shockley-type stacking sequence faults within the hexagonal SiC structure lattice and creating 3C-SiC- regions embedded within the main 4H-SiC structure [6-9]. In term of electrical parameters, the bipolar degradation manifests itself as the increase of the forward voltage of the power device due to poor conductivity modulation in the affected regions occupied by the SFs.

The motivation of this work is to understand the correlation between these bipolar degradations and the change of SiC MOSFET power devices characteristics through simulation models. Several papers have been published on SiC MOSFETs modelling methods that are mainly categorized as behavioural models, semiphysics models, physics-based models, seminumerical models or numerical models [10]. In this paper, 2-D device simulation models have been developed to investigate the bipolar degradation in SiC MOSFET. The paper is

organized as follows: section II presents a review of the bipolar degradation mechanism and explain how the defect is modelled within a 4H-SiC structure. In section III, the implementation of the power device in Silvaco-Atlas TCAD software is detailed and the main results are presented in section IV. A conclusion is given at the end of the paper.

REVIEW OF BIPOLAR DEGRADATION

Formation of partial dislocations

The cubic and hexagonal SiC structures known as 3C- and 4H- 6H- SiC are at present the main structures used for developing high power devices. However, deviation from their respective perfect stacking sequences is quite common during epitaxial growth processes as basal plane defects easily glide under stress because the critical resolved shear stress is relatively low in SiC at high temperature [2]. As a consequence, this deviation has been identified to create regions within the main structure that have the perfect stacking sequence of another polytype [6]. The structure is said to have stacking faults (SF) areas located between two partial dislocations (PD), namely the C-core and Si-core dislocation in which the latter is set into motion most likely due to electron-hole recombination enhanced dislocation glide (REDG) during the forward current conduction of bipolar devices as exemplified in figure 1 for the case of a 4H-SiC PiN diode.

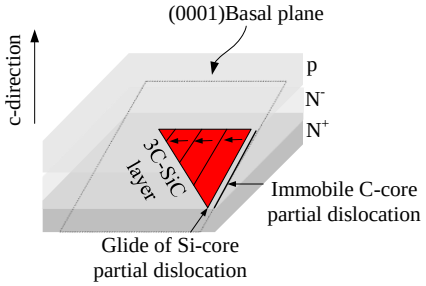

Figure 1. Schematic representation of Shockley stacking faults expansion within a *n-type* 4H-SiC PiN diode. A 3C-SiC layer area within the drift region is created by the glide of the Si-core partial dislocation while the C-core partial dislocation does not move.

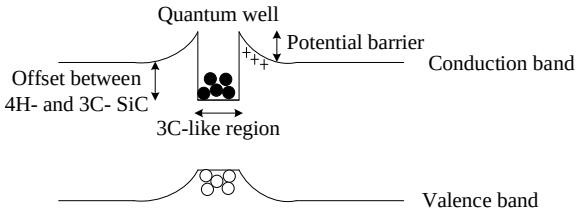

Figure 2. Conduction energy band split-off highlighting the inclusion of a 0.75nm 3C-SiC nano-layer into the 4H-SiC hexagonal structure which gives rise to a thin electron-attractive quantum well and creates a built-in potential barrier at both sides of the quantum well similar to a PN junction.

Electronic properties of SFs

The specification of the stacking patterns around stacking faults depend on the SiC polytype. We consider hereafter Shockley-type single SFs that are introduced by partial dislocations glide in the (0001) basal plane and are responsible for the so-called bipolar degradation in 4H-SiC power devices. In such structure, SFs in the neighbouring (0001) planes give rise to 3C-like cubic inclusion, i.e., a layer having a straight 3C-like stacking sequence [6]. Such structure's arrangement forms two heterojunctions of the type 4H-3C-4H SiC as schematically exemplified in figure 2. Experimental studies on *n-type* 4H-SiC samples, containing SFs regions, have indicated that this local thin planar 3C inclusion sequence is of the order of 0.75nm and lowers the conduction band by about 0.22eV - 0.31eV while the top of the valence band shows no such behaviour as illustrated in figure 2 [7]. For this reason, it was suggested that these SFs can be interpreted as a one-dimensional quantum well confinement effect with a strong electron localization in the c-direction (perpendicular to the (0001) basal plane, i.e., SF plane) [6-9]. Electrons trapped in the quantum well create a negative charge within the well and a positive charge within a depletion region from both sides of the well, until thermal equilibrium is established. As a consequence, a built-in electrostatic potential barrier appears in a similar way as in a PN junction. Under such condition, the overall energy properties of the 4H-SiC structure are fundamentally altered with the electron transport being practically obstructed in the c-direction whereas electrons are free to move in the SF plane [6].

MOSFET DEVICE MODELLING

To account for SFs effects in 4H-SiC MOSFET power devices, a thin 3C-SiC nano-layer is incorporated in the middle of the N^- drift layer of the device as shown in figure 3. Impact of such inclusion on the performance of the parasitic PiN body diode that initially triggers the bipolar degradation during the current conduction, and then the performance of the MOSFET in the first quadrant operation are examined using Silvaco-Atlas TCAD software.

The 2D cross-sectional view of the investigated 4H-SiC MOSFET structure is depicted in figure 3. Referring to literature data and design criteria for obtaining a threshold gate voltage between 4V and 6V [11], the doping and dimensions parameters are chosen as follows. A pitch cell of 8.5 µm has been considered throughout the analysis. The P^+ body region was designed with a thickness of 0.88 µm and an acceptor doping concentration of $1x10^{17}cm^{-3}$. The N^+ source region was designed with a thickness of 0.32 µm and a donor doping

concentration of $1x10^{19}$ cm^{-3}. The channel width was set to 1µm, and the thickness of the gate oxide was set to 50 nm giving an approximate threshold voltage of 5 V. The i-epilayer thickness was set to 12 µm to account for a breakdown voltage of 1.7kV. It was lightly doped with a uniform donor concentration profile of $1x10^{16}$ cm^{-3}. The N^- drain region was designed with a 2 µm thickness and a uniform doping concentration of $1x10^{19}$ cm^{-3}. A corrective factor was set within the algorithm to account for a MOSFET device with an approximate active area of $0.17cm^2$. It is worth noting that even though the design parameters may not be accurate with that of the commercial discrete power devices, it reflects the basic structure of the real device.

Note that the drain and the source electrodes were added to both sides of the structure. Shockley-type stacking faults regions are represented by the inclusion of a 3C-SiC nano-layer in the middle of the i-epilayer with a thickness of 0.75nm and a width varying between 25% and 100% of the total pitch cell width in order to get insights into the influence of the 3C-SiC inclusion on the carrier density and the I-V device characteristics. The simulated structure's parameters are summarized in Table I.

Material	Parameter	Value
4H-SiC	N^+ source doping concentration	1 x 10^{19} cm^{-3}
	P well doping concentration	1 x 10^{17} cm^{-3}
	N^- drift layer concentration	1 x 10^{16} cm^{-3}
	N^+ substrate doping concentration	1 x 10^{19} cm^{-3}
	Depth of N^+ source junction	0.32 µm
	Depth of P well junction	0.88 µm
	Thickness of the drift layer	12 µm
SiO2	Thickness of the gate	50 nm
3C-SiC	Inclusive thickness layer	0.75 nm

Table I. Summary of the simulated structure parameters

RESULTS AND DISCUSSION

Body diode degradation

The static I-V characteristics of the MOSFET body diode are depicted in figure 5 for different widths of the 3C-SiC nano-layer and at a temperature of 27°C and a gate voltage of -5V, assuring the MOSFET channel is fully pitched off (no synchronous rectification operation). Compared to the I-V characteristic of a healthy body diode, the maximum voltage shift ΔV_{max} due to the basal plane defect is estimated to be 0.7V at a current level of -3A. This represents the worst case scenario as it is assumed that the 3C- nano-layer, which is representative of the bipolar degradation, covers the whole width of the MOSFET pitch cell.

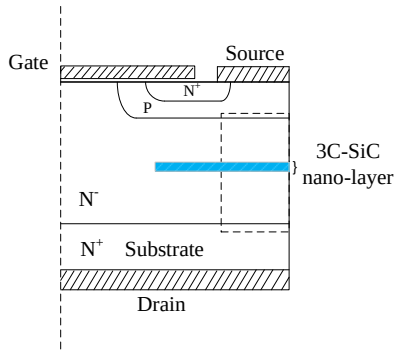

Figure 4. Cross-sectional view of the simulated 4H-SiC MOSFET power device with the inclusion of a 0.75nm 3C-SiC layer in the middle of the drift region.

However, the voltage shift does not drastically change with the 3C- nano layer width. This is due to the small active area the body diode occupies within the MOSFET pitch cell and hence it is suggested that SFs expansion will impact the performance of a MOSFET body diode at the early stage of the expansion.

In order to get insights into the behaviour of this drift configuration, the electrons and the holes carrier densities are presented in figure 6 at a voltage bias of -4V and a current of -3A. The electron/hole carrier densities within the defective 'i' region decrease when nearing the 3C-SiC nano-layer and a depletion layer of 0.1µm is formed at both sides of the 3C- layer. The density of the electrons is almost at its equilibrium value with a maximum excess carrier injection of only 1 x 10^{16} cm^{-3}. This is too low to assure high-level injection conditions. On the other hand, the minority carrier injection is approximately estimated to 4 x 10^{15} cm^{-3} which is still too low to assure the conductivity modulation effects necessary for PiN diodes to operate properly. The energy of the 4H-3C-4H- SiC structure at 27 °C is illustrated in figure 7. The energy gain due to the quantum well action of the 3C- nano-layer is estimated equal to $16mJ/m^2$ which exceeds the SFs energy formation γ of $14.7mJ/m^2$. This result is in accordance with the theoretical calculation obtained in [12] where it is predicted an energy gain of 15.5 mJ/m^2 with a doping concentration of 1 x 10^{16} cm^{-3} for the studied *n-type* 4H-SiC sample.

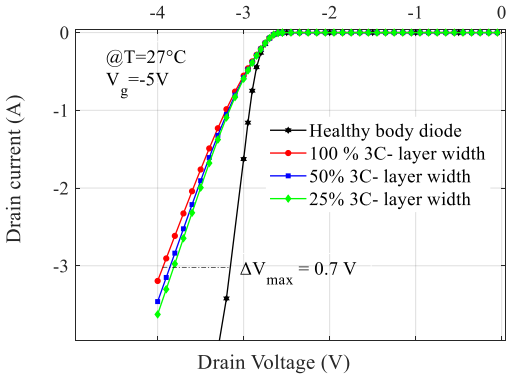

Figure 5. Static I-V characteristics of a healthy and a defective MOSFET body diodes where the width of the 3C-SiC nano-layer is varied between 25% and 100% of the total pitch cell width at a temperature of 27°C and a gate voltage of -5V.

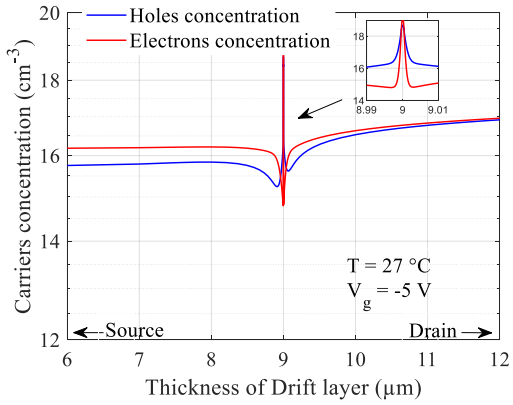

Figure 6. Defective MOSFET body diode Electrons/ holes carriers concentration. A depletion region is formed in the vicinity of the 3C-SiC nano-layer which causes the carriers concentration to lower.

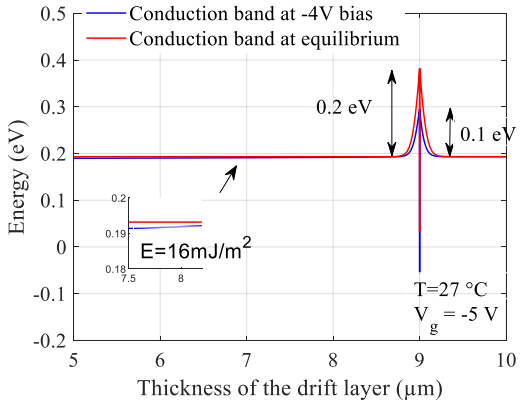

Figure 7. Defective MOSFET body diode energy at equilibrium (red) and at a bias voltage of -4V to illustrate the energy lowering due to the SFs. The energy formation is estimated equal to 16mJ/m^2.

MOSFET 1st quadrant operation

The unipolar MOSFET device operates under the majority carrier injection condition and as such, this mode of operation is not responsible for the expansion of the stacking faults (SFs). However, as previously mentioned, the voltage forward bias of the body diode triggers the basal plane dislocation glides, leading to the apparition of a 3C- polytype nano-layer within the 4H-SiC drift region. This obstructs as well the flow of the majority carriers.

Figure 8 shows the static I-V characteristics of the MOSFET operating in the 1st quadrant by varying the 3C-SiC layer width to cover 25%, 50% and 100% of the pitch cell, at a temperature of 27°C and a gate voltage of 20V. The voltage shift in this case is higher with a maximum voltage shift reaching 1 V at a current level of 4A. However, the size of the SFs had a more significant impact on the total active area of the device due to a larger depletion width appearing at both sides of the quantum well. At a voltage bias of 4V, the depletion width was estimated equal to 0.3 µm at 27°C, consuming space within the pitch cell and increasing the on-resistance by constricting the area through which the current can flow. The MOSFET on-resistance $R_{DS(on)}$ and its percentage variation with temperature are key performance indicators when considering the bipolar degradation and figure 9 illustrates the increase of the on-resistance of the simulated device at a temperature ranging from 300 K to 450 K. It is estimated an increase of 31% of the on-resistance at 300K. This suggests that the bipolar degradation is more detrimental to the operation of the MOSFET.

CONCLUSION

A two dimensional (2D) numerical model of a 4H-SiC power MOSFET device was build using Silvaco-Atlas simulator in order to gain insights into the performance degradation of the device when it is subject to a bipolar degradation due to the presence of stacking faults areas within the device. The defected area was represented by the inclusion of a 3C-layer in the middle of the drift layer of the device. This led to a heterojunction-like N^- region within the drift layer formed by a 4H-3C-4H- SiC arrangement. Regardless of the width of the 3C-SiC layer, it creates a high resistive area, preventing the current to flow through and hence reducing the total active area of the device. TCAD simulation results indicate that, during the operation of the MOSFET body diode, the electrons/holes carriers densities decrease within the vicinity of the 3C-SiC layer to a level that does not assure high level injection conditions for which the conductivity modulation is not possible. The forward voltage increase is due to the apparition of a depletion area at both sides of the 3C- nano-layer and is dependent on operating condition.

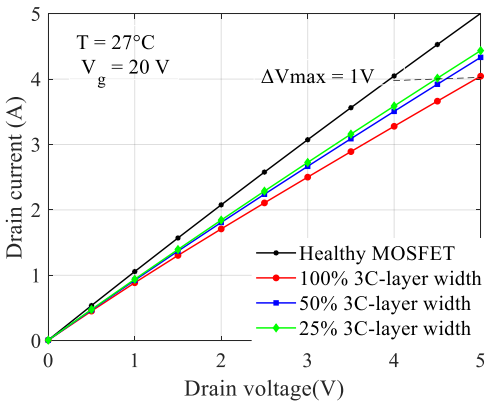

Fig 8. Static I-V characteristics of the MOSFET in the 1st quadrant obtained by varying the width of the 3C-SiC.

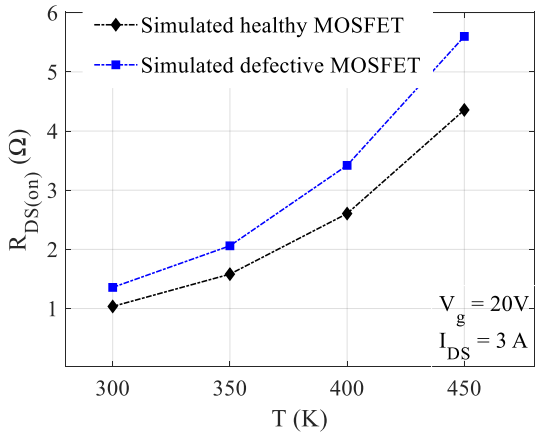

Figure 9. SiC MOSFET on-resistance variation in terms of the temperature. An increase of 31% is estimated at 300K.

Although the operation of the MOSFET in the 1st quadrant does not trigger any expansion of the stacking faults, it is still similarly affected by the presence of the 3C-SiC nano-layer.

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The influence of electrical stress on the distribution of electrically active defects in IGBT

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Abstract

This paper highlights electrically active defects investigation of the sixth generation 1200 V trench stop silicon-based Insulated Gate Bipolar Transistors by Deep Level Transient Fourier Spectroscopy. The focus is on the impact of electrical stress on defects distribution in the studied structures. Five electron-like deep energy levels ET1 (0.126 eV), ET2 (0.188 eV), ET3 (0.322 eV), ET4 (0.405 eV), and ET5 (0.514 eV), and nine hole-like deep energy levels HT1 (0.187 eV), HT2 (0.231 eV), HT3 (0.246 eV), HT4 (0.301 eV), HT5 (0.319 eV), HT6 (0.327 eV), HT7 (0.529 eV), HT8 (0.534 eV), and HT9 (0.750 eV) were identified. The presence of unintentional impurities like zinc, platinum, gold, etc. and emissions from structural imperfections was confirmed. A significant increase of the defect concentration after electrical stress in the temperature range of 120 to 225 K has been detected. Electrical stress did not affect the defect concentration above temperature 300 K.

Keywords: IGBT, deep energy levels, electrically active defects, the impact of electrical stress, Deep Level Transient Fourier Spectroscopy.

INTRODUCTION

The development of innovative silicon-based power semiconductors devices with increased power density and energy efficiency is a challenge for an advanced industry 4.0. These devices provide the performance of a large number of applications, with a focus on industry, mobility, grid and renewable energy [1]. Together, they will contribute to reducing carbon dioxide emissions despite the world's ever-increasing energy needs [2]. This is consistent with one of the objectives of the European Commission, which wants the EU to lead the clean energy transition. For this reason, the EU has committed to cut CO_2 emissions by at least 40% by 2030 [3].

Silicon-based power solutions are well known for decades [4]; however, the demand for the highest energy efficiencies are growing. Based on new materials, like gallium nitride, and silicon carbide [5], [6], the highest efficiencies have been shown recently, and production of those devices has started and will increase. Widely established silicon outcompetes upcoming new materials like GaN and SiC for power electronics because of its high reliability and excellent performance-price ratio (Figure 1).

IGBT power transistors have an irreplaceable role in power electronics circuits. The silicon-based IGBT has become widely accepted as the power device of choice for medium and high-power applications where the circuit operating voltages exceed 200 V [7]. It has enabled the development of highly efficient adjustable speed motor drives for industrial applications, compact fluorescent lamps for lighting, and an electronic ignition system for transportation [8]. During their operation, these components are exposed to extreme electrical stress, so it is desirable to ensure high stability of the distribution of electrically active defects for the correct operation of these components.

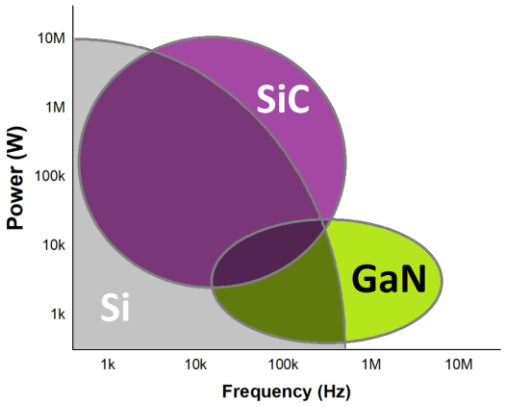


Figure 1: Comparison of technologies (inspired by [9])

The presence of electrically active defects in semiconductor devices can negatively impact the operation of these devices. These defects represent deep energy levels in the forbidden band of the semiconductor, which behave as capture or recombination centres. They are most of the time direct sources of material degradation, undesired electrical, optical or even structural properties. For example, after capturing the free carrier in such a capture centre, this localised charge carrier will no contribute to the current, and the carrier lifetime will be shortened. A carrier lifetime is a key physical property, which determines the on-state and switching characteristics of bipolar devices. It can cause slower switching during switching processes but also make the whole system inoperable. Even small concentrations of unwanted electrically active defects can significantly affect the performance and reliability of IGBTs. Defect identification and control has always been one of the essential tasks in the development of electronic devices and to optimise the fabrication process [10].

Deep Level Transient Spectroscopy (DLTS) is one of the essential methods of electrical active defect identification [11]. The values of the fundamental parameters governing thermal emission and capture on a deep energy level - activation energies ΔE_T and capture cross sections σ_T were calculated from an Arrhenius diagram [12]. It is a high-frequency capacitance transient thermal scanning method in which an electrical excitation pulse causes the capacitance transient effect in the potential barrier of the semiconductor. Although DLTS satisfies basic diagnostics requirements, e.g. non-destructivity and sensitivity, like other techniques, it has its limitations. The most challenging part of such investigation is the interpretation of experimental results [13]. Different factors are needed to be taken into account to establish a reliable evaluation procedure. On the one hand, we can have a comprehensive and reliable measurement result, although on the other, a non-evaluable experiment. In some cases, the opposite is true, deep energy level parameters (activation energy ΔE_T, capture cross-section σ_T and the trap concentration N_T) are obtained with high reliability, but structural and geometrical properties are indicating a questionable investigation.

The method's accuracy is mainly affected by complex situations in which different deep energy levels are interacting; therefore, the utilisation of different defect-recognition techniques and analytical approaches is a crucial factor of accuracy. We focus on one of the digital DLTS modifications, the DLTFS (Deep Level Fourier Transient Spectroscopy) method [14]. DLTFS is a digital system that records the whole capacitance transients and transfers the data into a computer system. Using a Fourier transformation and direct evaluation of the Fourier coefficients, the time constant and the transient amplitude can be evaluated for every transient measured at any temperature. Only one temperature cycle is necessary to measure the activation energy of a deep energy level. This modification was developed according to the increasing need for high sensitivity, reliability and accurate results.

This paper introduces the DLTFS study of electrically active defects in 1200 V silicon-based IGBT power transistors prepared by the sixth generation trench stop IGBT technology. This study was realised with the aim to contribute to investigate the impact of electrical stress on the distribution of defects in the measured structures.

EXPERIMENT

IGBT power transistors used in this DLTFS study are 1200 V silicon-based trench gate/field-stop IGBTs. This first 1200 V discrete IGBT in 300 mm was prepared by the sixth generation trench stop IGBT technology. It is optimised for low switching losses in hard switching and resonant topologies operating at switching frequencies above 15 kHz. Its typical structure is illustrated in Figure 2 left, and key performance parameters are listed in Table 1. The examined samples were exposed to electrical stress: pulse width 3 µs, drain voltage 600 V, the gate voltage 15 V, current 100 A and number of pulses 200 thousand. Three sets of DLTFS measurements were realised: before electrical stress (structure labelled no stress), after the stress (structure labelled stress 1) and after the repeated stress (structure labelled stress 2).

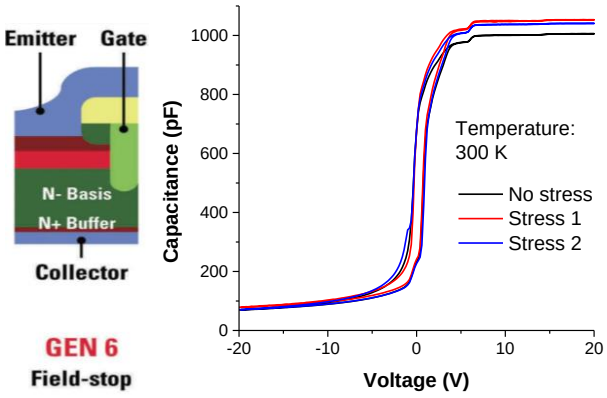


Figure 2: a) Silicon cross-section of a trench IGBT [15] and b) measured CV on the examined IGBT structures

Parameter	Symbol	Value
Collector-emitter voltage	V_{CE}	1200 V
DC collector current	I_C	15 A
Collector-emitter saturation voltage	V_{CEsat}	1.9 V
Operating junction temperature	T_{vj}	-40…+175°C

Table 1: Key performance parameters of the studied IGBT

Figure 2 right shows characteristic C-V measured on the examined IGBTs before and after electrical stress. The DLTFS measurements were carried out in the temperature range from 80 to 550 K using the BIORAD DL8000 measuring system equipped with Fourier transform analysis of the measured capacitance transients. The signal frequency for capacitance measurements is 1 MHz, and the magnitude of the applied differential voltage is 30 mV. During the measurements, the reverse bias was set at different voltages and periodically pulsed to the fill voltage to ensure trap filling. The voltages were applied between IGBT terminals Gate and Collector. DL8000 workplace displayed the majority charge defects as positive peaks and the minority charge defects as negative peaks [14]. The obtained DLTFS spectra were evaluated using the Fourier transform analysis with the "Direct Arrhenius evaluation" option.

RESULTS AND DISCUSSION

DLTFS experiments confirmed the presence of several emission and capture processes (Figure 3 - 8). Five electron-like deep energy levels and nine hole-like deep energy levels were identified. Defect parameters compared with parameters in references [16 – 23] are presented in Table 2. These identified defects most likely belong to the impurities of the chemical elements. Unintentional incorporation of impurities like zinc, gold, nickel, vanadium, silver, manganese and platinum are common contaminants in the growth systems typical for silicon-based devices. References for the identified defects presented in Table 2 are available in the defect catalogue/library at the DL8000 workplace. However, the origin of the identified defects may not correspond to the reference levels from the defect catalogue closest to the position. Due to the atypical behaviour of DLTFS spectra at temperatures lower than 250 K, it is possible to assume that the disturbances in DLTFS signal for defects ET1, ET2, HT1, and HT2 may correspond to the emission from structural imperfections like vacancies, resp. A – centre, corresponding to the vacancy-oxygen center [24].

Figures 3 depict measured DLTFS spectra under the different measurement conditions in all three types of examined structures with evaluated 5 electron-like deep energy levels with the activation energies and the positions in the DLTFS spectra. Defects ET1 (0.126 eV), ET2 (0.188 eV), and ET5 (0.514 eV) were identified in all three types structures. Defects ET3 (0.322 eV) and ET4 (0.405 eV) were identified only in structures after stress (stress 1 and stress 2).

Typical measured DLTFS spectra only for minority defects are shown in Figure 4. Nine hole-like deep energy levels HT1 (0.187 eV), HT2 (0.231 eV), HT3 (0.246 eV), HT4 (0.301 eV), HT5 (0.319 eV), HT6 (0.327 eV), HT7 (0.529 eV), HT8 (0.534 eV), and HT9

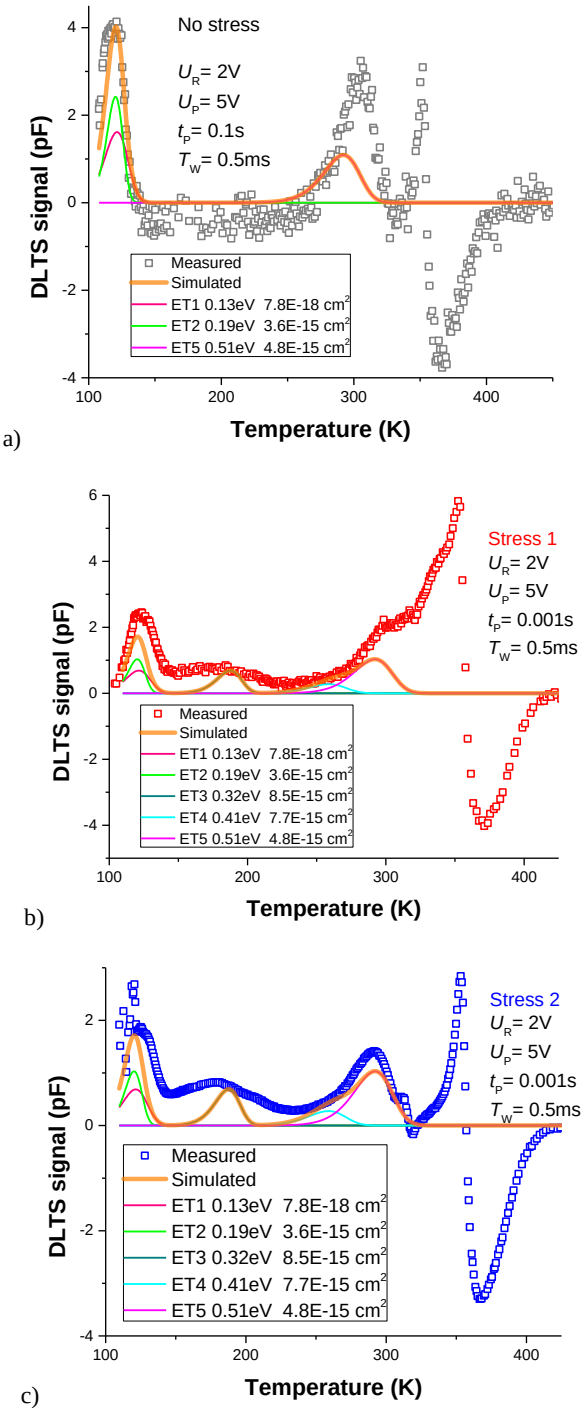
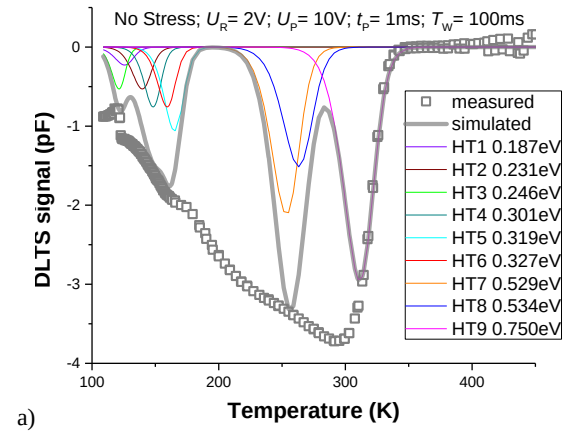


Figure 3: Identified electron-like defects, measured and simulated DLTFS spectra.

(0.750 eV) were identified in all three investigated structures. It is possible to observe significant changes in the peak heights of DLTFS signals corresponding to the identified defects.

The Arrhenius plots in the Figure. 5/ Figure 6 show all the evaluated electron-like/hole-like deep energy levels with their activation energies and reference deep energy levels with activation energies from the defect library for silicon. The effective mass of electrons and holes in silicon were respected in the DLTFS.



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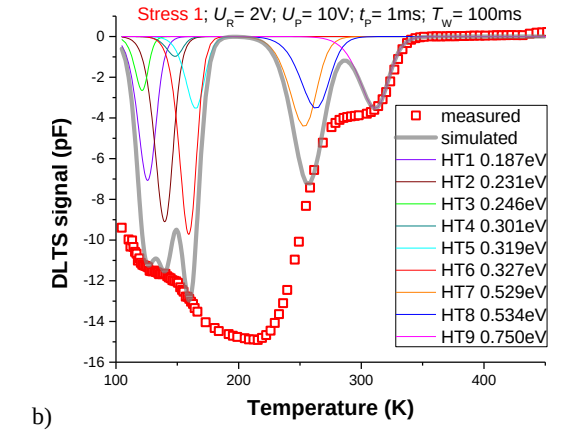

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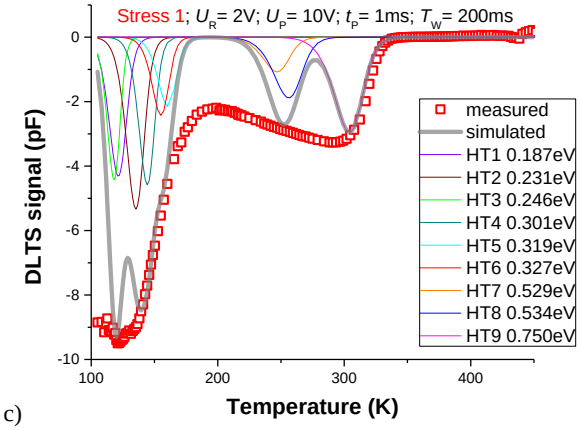

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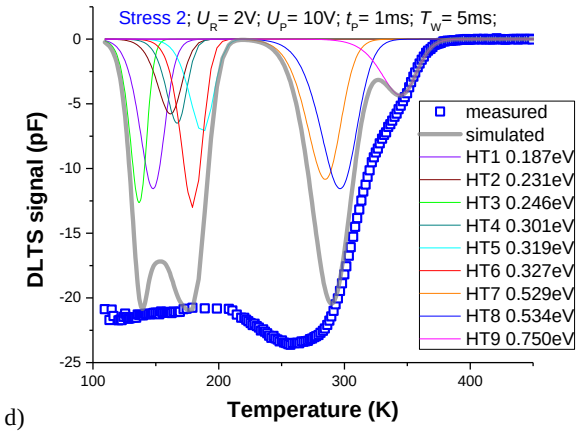

d)

Figure 4: Identified hole-like defects, measured and simulated DLTFS spectra

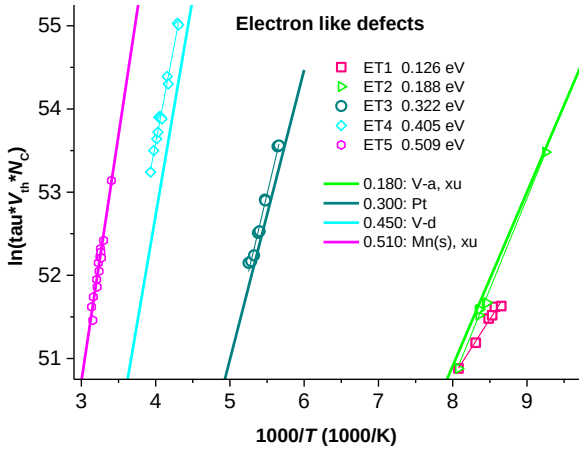

Figure 5: The Arrhenius plot of electron like defect

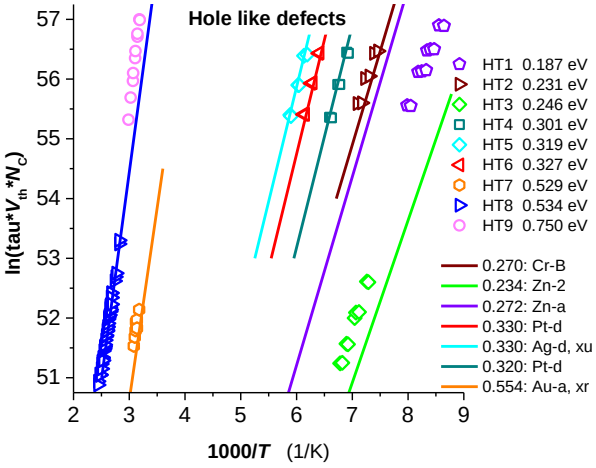

Figure 6: The Arrhenius plot of hole-like defect

During the DLTFS study of structure Stress 2, a significant effect of repeated measurements - thermal and electrical stress on the measured DLTFS signal - was observed (Figure 7). At the same time, the relaxation of the sample is confirmed. Figure 7 shows the DLTFS signal labelled Meas 1, and the DLTFS signal labelled Meas 3. These measured signals are almost identical. The time between the two measurements was 48 hours.

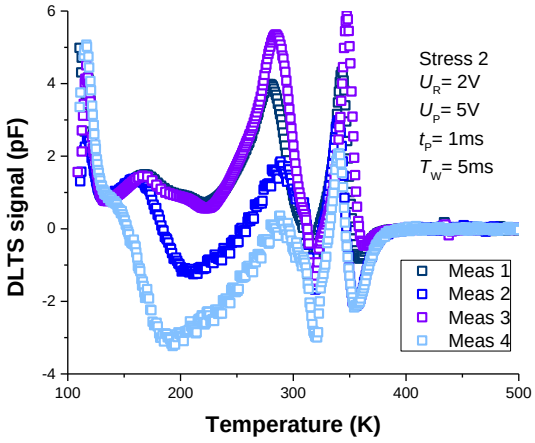

Figure 7: The impact of repetitive DLTFS measuring process measured Arrhenius plot of hole-like defect

Defect Name	Energy ΔE_T (eV)	Cross-section σ_T (cm^2)	Comparison; references
ET1	0.126	7.81×10^{-18}	0.18:VO [16]
ET2	0.188	3.55×10^{-15}	0.180:V-a [17]
ET3	0.322	8.52×10^{-15}	0.300:Pt [18]
ET4	0.405	7.72×10^{-16}	0.430:Ni-a [18]
ET5	0.509	4.79×10^{-15}	0.510:Ag-a [18] 0.510:Mn(s) [19]
HT1	0.187	2.48×10^{-17}	0.234:Zn, 0.272:Zn, [20]
HT2	0.231	1.39×10^{-16}	0.270: Cr-B [21]
HT3	0.246	9.84×10^{-14}	0.234: Zn [20]
HT4	0.301	7.81×10^{-15}	0.320:Pt-d [22]
HT5	0.319	2.55×10^{-15}	0.330: Ag-d, xu [23]
HT6	0.327	1.10×10^{-14}	0.330: Pt-d [22]
HT7	0.529	6.50×10^{-15}	0.554:Au-a, xr [21]
HT8	0.534	3.08×10^{-15}	0.599: Zn-aa [20]
HT9	0.750	1.81×10^{-13}	0.599: Zn-aa [20]

Table 2: Calculated defect parameters with possible referent data

Figures 8 depict compare of measured DLTFS signal of examined structures at the selected measuring conditions. The shape of the measured DLTFS signals shows that electrical stress affects the distribution of electrically active defects significantly below 300 K. This information is highly favourable, as most power devices such as the IGBT operate at room temperature and above. On the other hand, electrical stress significantly multiplies the concentration of defects around a temperature of 225 K and less. The value of the DLTFS signal capacitance increased from ~ -3 fF to ~ -12 fF (Figure 8 d), which means that at a temperature of 225 K, there was a fourfold increase in the concentration of defects after electrical stress.

However, the interaction between the majority and minority responses in the range from 300 to 350 K made it difficult to determine the defect parameters. If there are two defects in the same temperature range, one is electron-like and the second is hole-like, the emission process interacts with each other. When the voltage is reduced to reverse bias after applying the filling pulsed UP DLTFS signal passes from one type of defect to another type through zero (Figure 8 a) in DLTFS spectrum, which indicates interaction of these processes. The peak that we see in the DLTFS spectrum as a defect is the sum of these emissions at a given temperature, which distorts the parameters of the actual defect. Therefore, emission and capture processes at 350 K are a significant challenge for the DLTFS evaluation of measured spectra. Further research will be devoted to this problem.

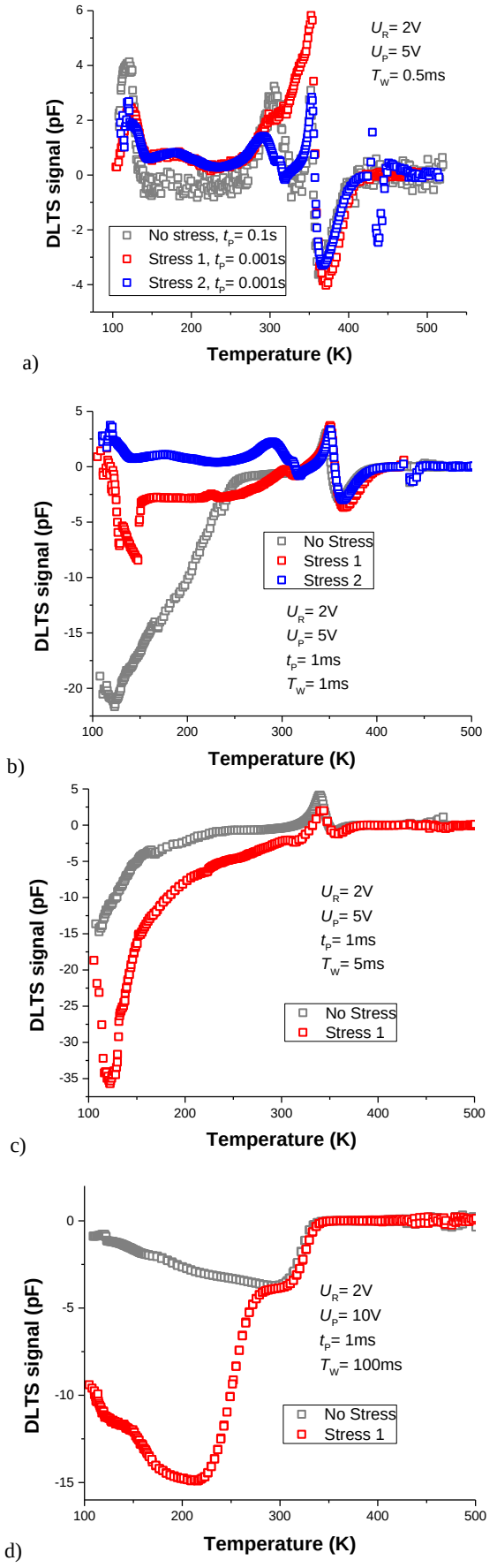

Figure 8: Compare of measured DLTFS signal of examined structures at the special measuring conditions

CONCLUSION

Power semiconductors are needed in all stages of energy conversion: generation, transmission, and use. More efficient silicon-based semiconductors devices applied in mobility, industry, and grid make a significant contribution towards reducing carbon dioxide emissions in spite of the world's growing energy needs. IGBT power transistors have an irreplaceable role in power electronics circuits.

This paper deals with the investigation of the distribution of electrically active defects in 1200 V silicon-based trench gate/field-stop IGBTs by the method of Fourier deep level transient spectroscopy. These power IGBTs were prepared by the sixth generation trench stop IGBT technology. These structures were exposed to electrical stress: pulse width 3 µs, drain voltage 600 V, the gate voltage 15 V, current 100 A and number of pulses 200 thousand. Attention is focused on the analysis of the influence of electrical stress on the distribution of defects in the investigated structures.

Five electron-like deep energy levels and nine hole-like deep energy levels were identified. The presence of unintentional impurities like zinc, platinum, gold, etc. and emissions from structural imperfections was confirmed. A significant increase of the defect concentration after electrical stress in the temperature range of 120 to 225 K has been detected. Electrical stress did not affect the defect concentration above temperature 300 K.

The investigated silicon-based IGBT shows exceptional quality. These are silicon-based power devices that are extremely well mapped, and at the same time, due to the precision of the production technology, silicon is extremely pure, as evidenced by capacitance values corresponding to the maxima of measured DLTFS signals. Very little influence of electrical stress on the distribution of electrically active defects in IGBTs in the area of working temperatures was confirmed.

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Parylene as Coating for Power Semiconductor Devices

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Abstract

The introduction of wide band gap semiconductor devices leads to smaller package sizes, higher power densities and higher switching frequencies, which is advantageous compared to the power electronics based on the conventional silicon devices. However, due to the small insulation distances and the limited temperature range of available package materials, it is not possible to exploit these advantages completely. In this study, the properties of Parylene coatings as passivation layers in power semiconductor devices is investigated. The material would be particularly advantageous for double-side cooled power modules because it can fill the small gaps between different conductive layers, which is not possible with conventional packaging technologies. Parylene is promising to provide an excellent insulation performance even in these areas and exhibits a good temperature stability. Furthermore, this polymer acts as a barrier for humidity, dirt and corrosive gasses. Two types of Parylene were tested using the High-Voltage, High Humidity, High Temperature Reverse Bias (HV-H³TRB) test on substrate level and the better Parylene type also on automotive three-phase modules. The results are encouraging, although the performance strongly depends on the Parylene type and although a sensitivity to the respecive surface condition to be coated became apparent.

Keywords: Parylene, Coating, Encapsulation, Packaging, Power Electronics, Double-sided cooling, Power Module, Environmental Stress, Humidity Testing, THB, H³TRB, HV-H³TRB, Reliability.

INTRODUCTION

Replacing the conventional silicon (Si) by wide band gap (WBG) power semiconductor devices is particularly useful in applications asking for high power densities (e.g. SiC in electric vehicles) and high switching frequencies (e.g. GaN in inductive charging). But the advantages of WBG over silicon cannot be fully exploited yet due to the limitations imposed by the device packaging. Available packaging materials are limiting the maximum usable temperature range considerably and, in this way, retarding rapid market acceptance [1, 2]. In general, there are two basic trends to increase the temperature performance. One approach is to improve the temperature ratings of the plastics and composites applied next to the semiconductor chips. However, the mechanical characteristics tend to deteriorate with maximum allowed temperature and compromise the devices' integrity.

Another approach is maximising the cooling by adapting the double-side cooling principle [2–5]. However, this requires a coating, which is able to enter the smallest crevices, like Parylene does, which is also used for medical instruments and implants [6–9]. Figure 1 shows a simplified structure of such a double-side cooled module. Each substrate consists of two copper layers (a) with a ceramic insulation (b) placed in between. The die (c) is connected to the copper layers of the substrates via the die attach on both sides (d).

However, miniaturised power electronics structures become more and more challenging in terms of insulation requirements. The gaps (e) in between the two substrates have to be filled entirely to avoid partial discharges or even sparkovers. In conventional silicon power device packaging, silicone gel is the agent of choice acting as surface insulation. Unfortunately, silicone cannot be applied in this case due to its relatively high viscosity. The material just does not fill out the space properly in standard processing.

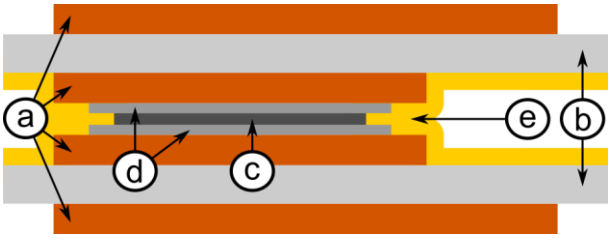

Fig. 1. Double-side cooled power module cf. [4]

In contrast, Parylene coatings provide excellent insulation properties [10] and the deposition process allows to fill the tightest gaps. Furthermore, a protective layer against dirt, humidity and corrosive gasses is provided [11]. As the diverse Parylene types offer these benefits to a different degree, two types were investigated in this work. Coated substrate samples were produced and tested under High Voltage, High Humidity, High Temperature Reverse Bias (HV-H³TRB) conditions.

Based on the results from the basic test, automotive three-phase modules, coated with the most performant Parylene variant were tested in HV-H³TRB, too.

TEST SET-UP

Based on the power module structure in figure 1, test samples were produced consisting of only an Active Metal Brazing (AMB) substrate and bond interconnects. The substrates have a size of 20 mm × 20 mm. The top-side structure consists of two copper areas with a gap of 1 mm in between, as shown in figure 2. Both areas were connected with bond wires to establish an electrical connection. Each sample is coated with Parylene. In this study, two different Parylene types were used. Parylene 1 has a maximum temperature, which is similar to silicone gel, while Parylene 2 can withstand significantly higher temperatures. The processing steps are the same for both types, but the chemical structure is different.

Prior to the Parylene deposition, an advanced cleaning process is needed to ensure a proper adhesion of the polymer on the substrate, which is a crucial factor to improve humidity robustness. The preconditioning of the surface was performed using a wet chemical cleaning process. The Fourier-Transform Infrared (FTIR) spectroscopy results, obtained with the FTIR microscope Bruker LUMOS, show the differences before and after the wet chemical treatment of the copper AMB substrates. A significant reduction of organic contaminations on the substrate surface could be verified by FTIR spectroscopy results shown in figure 3.

After the cleaning process, the samples were coated at an evaporation temperature between 100 and 150 °C and a deposition pressure below 10 Pa.

Seven samples of each test group were mounted on a PTFE test board and six of them were connected in parallel to increase the number of samples in the test. The seventh sample remains without any electrical connection and acts as a chamber reference. Figure 4 shows an overview sketch of these test boards.

The HV-H³TRB test was performed to evaluate the performance of the two Parylene types. The samples were exposed to the climate conditions of 85 °C and 85 % relative humidity for at least 3 h to reach a climatic equilibrium. Then, the test voltage of 1000 V was applied for the entire duration of the respective test cycle. If one of the samples connected in parallel carried a too high leakage current, the measurement channel for the whole test group was switched off automatically. After the cycle time elapsed, the voltage was switched off and the drying period started for at least 3 h at 50 °C and 10 % relative humidity. After each cycle, failed samples were removed from the board. Then, the next cycle continued including the remaining samples only. Figure 5 shows the test procedure for each cycle in detail.

(a) (b) (c)

Fig. 2. Samples: (a) before HV-H³TRB, (b) after HV-H³TRB without bias (slight discolouration), (c) catastrophic failure during HV-H³TRB

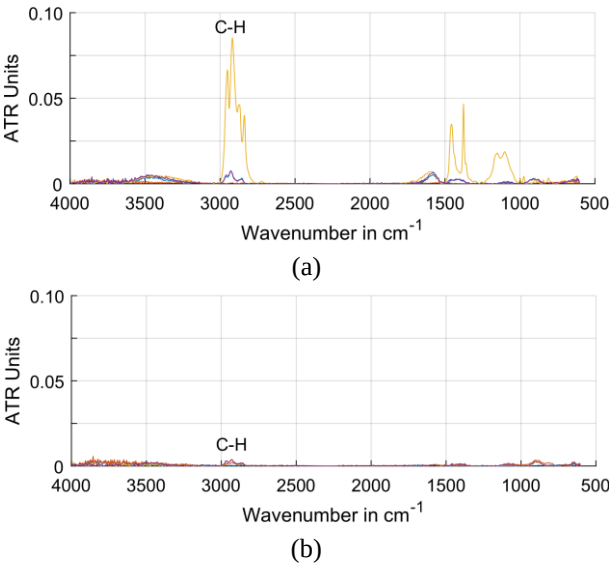

Fig. 3. FTIR results before (a) and after (b) the wet cleaning process at various positions

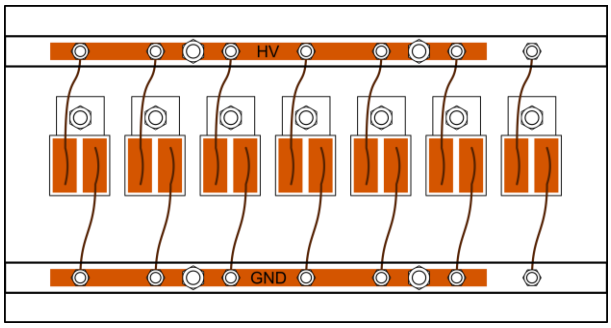

Fig. 4. Test board with six DUTs and an unbiased chamber reference (on the right).

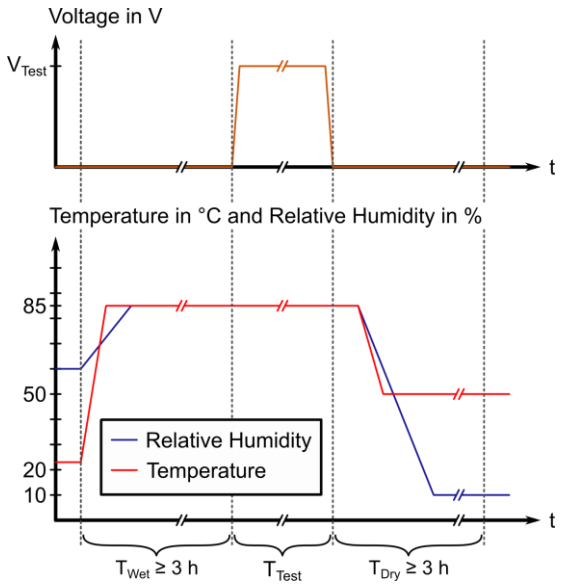

Fig. 5. Test procedure per cycle

RESULTS AND ANALYSIS

Due to the rather large number of samples per test split, the HV-H³TRB test on the substrate samples allows a statistical evaluation. The Weibull plot in figure 6 reveals the differences between the two Parylene types and the impact of the cleaning process. The most obvious result is the much tighter distributions, which the Parylene 1 splits exhibit. As shown in table 1, the lifetime (scale parameter) of Parylene 1 is also significantly higher compared to Parylene 2. While the impact of the cleaning process is negligible for Parylene 2, it leads to a significantly higher performance for Parylene 1. The shape factor for Parylene 2 is below one, indicating early failures. In contrast, the shape parameter is significantly higher than one for Parylene 1, pointing out that the failures are due to wear-out.

During the HV-H³TRB, the failures were detected by an increase of the leakage current. All failures (cf. figure 2 (c)), come along with burn marks between both electrode pads. Further analysis of the failed test objects revealed a dendritic growth below the Parylene layer, which finally leads to a short circuit between the two electrodes. Figure 7 shows a dendritic structure on the left side and a catastrophic failure on the right side. The growth of the dendrite starts at the electrode with the applied high potential (anode) and propagates towards the low or ground potential. The underlying electrochemical process is called “Anodic Migration Phenomenon” (AMP) and is described in [12, 13]. Consequently, migration products under the Parylene coating could be observed in the area of the anode (figure 8).

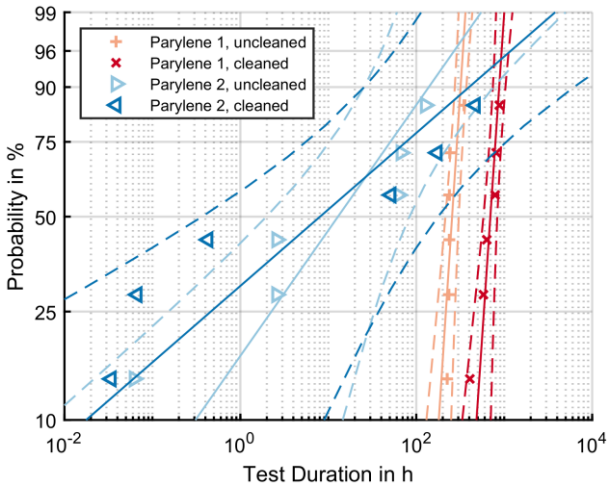

Fig. 6. Weibull plots of the substrate test campaign

Tab. 1 Weibull parameters for each test group

Name	Scale in h	Shape
Parylene 1, uncleaned	273	5.4
Parylene 1, cleaned	764	8.5
Parylene 2, uncleaned	26.6	0.5
Parylene 2, cleaned	26.5	0.3

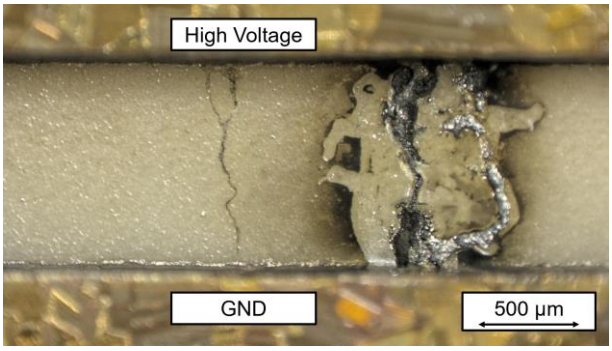

Fig. 7. Dendritic growth between the electrodes

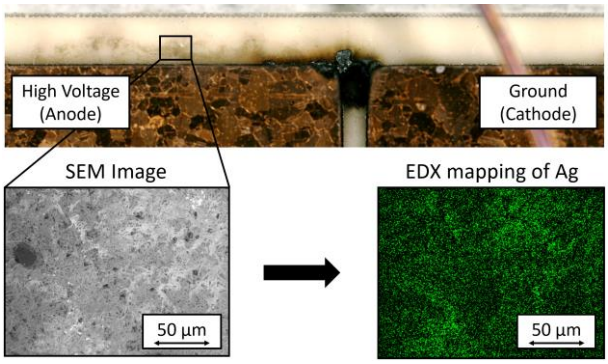

Fig. 8. EDX analysis of AMP residues

Since the copper area on the backside of the substrate is not connected, a capacitive voltage divider leads to a third potential in this test structure. The migration products of the AMP process can be observed on the edges of the substrate of the anode. The Parylene coating has been removed for the EDX analysis. The mapping of silver, as shown in figure 8, proves the migration products to be a chemical compound of silver, which originates from the AMB substrate.

One crucial factor during the AMP process is the delamination of the Parylene polymer from the surface. Using the Iodine Vapour Test (IVT) [14, 15], defects in the Parylene coating as well as adhesion weaknesses and delamination can be revealed optically. Delaminations as shown in figure 9, are visible after 4 h IVT at 80 °C. Mechanical stress, imposed e.g. by bent copper bond wires (see figure 9, left side) led to cracks and delamination. However, the delamination in this place is not a relevant failure mechanism. More important is the delamination visualised by the Iodine entrapped between the ceramic substrate and the Parylene layer. During the HV-H³TRB test, the delamination in this area leads to early failures due to the accumulation of water in the gaps and a faster degradation.

Fig. 9. Iodine Vapour Test results after 4 h at 80 °C

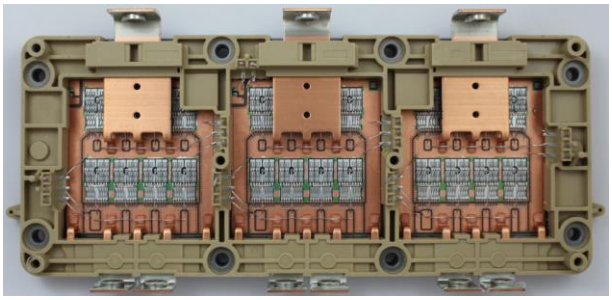

Fig. 10. 450 V three-phase automotive module coated with Parylene

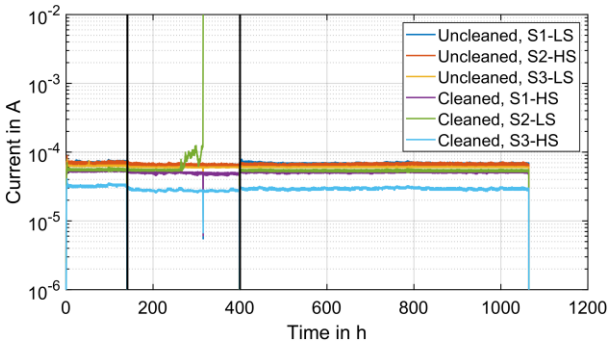

Fig. 11. Leakage logging during H³TRB Test of 450 V power modules at 85 °C, 85 % relative humidity and a test voltage of 405 V

CONFIRMATION ON POWER MODULE LEVEL

Based on the results of the substrate test, the Parylene 1 was selected to be tested on power modules for automotive applications. In this test, two three-phase modules were used. Each module consists of three half bridge systems and each half bridge has a high-side switch and a low-side switch. Every switch includes four IGBT chips and four diode chips. While one module remained uncleaned, the other module had been treated with the wet cleaning process. Both modules were coated with Parylene 1. Figure 10 shows a coated module before HV-H³TRB test. The voltage rating for these power modules is 450 V, although the chip voltage rating is higher. An HV-H³TRB test was carried out at 85 °C, 85 % relative humidity and 405 V, which is 90 % of the modules' voltage rating. The test duration was set to 1000 h according to AQG 324 [16].

Figure 11 shows the logging of the leakage currents of the respective switches under test. After 140 h and after 400 h the test was interrupted for intermediate measurements. During the whole test, only one semiconductor chip failed after 315 h in system 2, high side of the cleaned module. At the intermediate measurement after 400 h this DUT was inspected optically and the failed semiconductor has been disconnected from the other parts of the system. The blocking capability of the system regained the initial level. The same system was tested for the remaining test duration. The root cause of this failure is suspected to be an extrinsic defect, possibly due to processing the modules at different sites. No more failures occurred during the test of 1000 h.
The reason for the longer lifetime of the modules compared to the substrate samples is the much higher stress induced by the higher test voltage applied to the substrate samples.

SUMMARY AND OUTLOOK

In a first step, simplified structures of two copper pads with a distance of 1 mm on a ceramic substrate were produced and tested in HV-H³TRB. Each sample was coated with a layer of one of the two Parylene variants investigated. Some of the samples had been cleaned before the coating. During the HV-H³TRB test, the samples were exposed to 85 °C, 85 % relative humidity and 1000 V. Parylene 1 is clearly superior, showing a consistent wear-out behaviour, and cleaning the substrate before the coating increases its capability even further. The failure analysis indicated that the adhesion of the Parylene layer had been a crucial factor. Parylene 2 leads to an early-failure characteristic, with some very early failures due to delamination.
The superior Parylene 1 was then selected for a test on automotive power modules. In this second step of the investigation, two three-phase modules were tested in HV-H³TRB at 85 °C, 85 % relative humidity and 405 V for 1000 h. The three phases of the module were tested individually. There was one early failure, possibly due to an extrinsic root cause. Apart from that, the modules were completely stable.
These two experiments show that from a humidity capability point of view Parylene is indeed suited for standard power modules. The next step will be more challenging structures, e.g. required for double-side cooling, power cycling and thermal cycling experiments.

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Commercial Sweet Spots for GaN and CMOS Integration by Micro-Transfer-Printing

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Abstract

Several approaches for close integration of power switches with CMOS logic are subject of technical evaluations and academic discussions. This paper identifies the commercially relevant processing steps of different integration methods (HV and SOI CMOS, monolithic integration in SOI and in GaN, Direct Wafer Bonding, micro-Transfer-Printing of GaN on CMOS and CMOS on GaN) and compares them on simple cost per wafer and cost per chip models. Four examples of real ICs verify the simple costs per chip model. Commercially attractive high voltage to logic partitionings are identified for the different integration approaches.

Keywords: heterogeneous integration, monolithic integration

MOTIVATION

The need for better efficiencies of power supplies and inverters with smaller footprints can be met with Wide Band Gap (WBG) power devices like Gallium-Nitride (GaN) High Electron Mobility Transistors (HEMTs) with lower on-state and dynamic losses capable to switch at higher frequencies. Several approaches for close-by integration of GaN power switches together with silicon based CMOS driver and controller logic are on the market or subject of technical evaluations and academic discussions.

The package parasitics, namely the package lead inductance, bond wire length related inductances and resistances, as well as the PCB trace inductances are a serious obstacle to the high-speed switching, which is necessary in order to reduce the switching power losses or reduce the size of power converters [1], [2], [3], [4].

While academic research is and has to be done in all fields further industrial development can only occur within commercially promising areas. Therefore commercial boundary conditions impose economic limits to the usability of the different integration approaches depending heavily on the potential applications.

INTEGRATION APPROACHES AND RELATED COSTS

Partitioning

The addition of power switches to a CMOS logic can be realized in many different process technologies ranging from silicon based CMOS technologies to monolithically integrated GaN or silicon solutions. But for most solutions in general the costs for substrate, epitaxy, manufacturing and wafer test are per wafer. The costs per chip additionally include the number of good dies defined by the chip size and yield figures. Both cost figures are independent from the aerial usage of dedicated process steps. This so called partitioning problem is shown in Figure 1 for the example of a monolithic GaN integration into a silicon based CMOS logic technology. The full processing expenses e.g. for the GaN Metal Organic Chemical Vapour Deposition, MOCVD, are incurred independent if the IC contains only small or large GaN areas.

With a small GaN area all the GaN related costs are for a very small functional area, with a very high GaN area the costs per logic functionality get very high. Similar problems occur for dedicated high voltage or low voltage CMOS processing steps or mask layers which are used only in small parts or in only a few devices in the IC – but of course with much smaller values compared to GaN MOCVD epitaxy.

So when looking at costs per functionality, this implies acceptable costs structures for many integration approaches only for evenly distributed area usage but, very high costs levels e.g. in the mentioned example when integrating only one very small GaN high voltage switch.

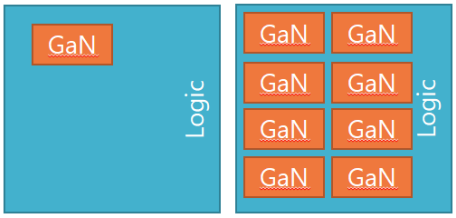

Figure 1: Partitioning problem for the example of monolithic GaN integration into a silicon CMOS chip, left: low GaN usage, right: low logic usage

Bulk CMOS

Already with standard CMOS technologies just by adding dedicated HV implants or gate oxides low side n- and p-channel enhancement and depletion transistors with operating voltages above 600V can be realized. With more specialized and dedicated CMOS or Bipolar CMOS DMOS (BCD) processes also high side configurations even above 600V can be manufactured.
Costs to be taken into account are the substrate material including the epitaxy and the processing costs depending on the complexity of the process. Both costs are area independent.

SOI CMOS

Replacing the bulk or epitaxial substrates by SOI wafers higher performance and high side capability can be achieved at the expense of higher wafer costs.
Costs to be taken into account are the SOI substrate material and the processing costs with both costs being area independent.

Monolithic integration in SOI

For the monolithic integration of GaN HEMTs on a silicon CMOS wafer several approaches have been discussed in the literature [5], [6], [7], [8]. A promising approach might be the use of Silicon-On-Insulator (SOI) wafers with (111) oriented handle wafer (the lower wafer in the SOI stack) with a (100) oriented upper device wafer. Etching a tub down to the handle wafer reveals an appropriate (111) oriented substrate for GaN epitaxial growth while the device wafer has the typical CMOS (100) crystal orientation, see Figure 2.

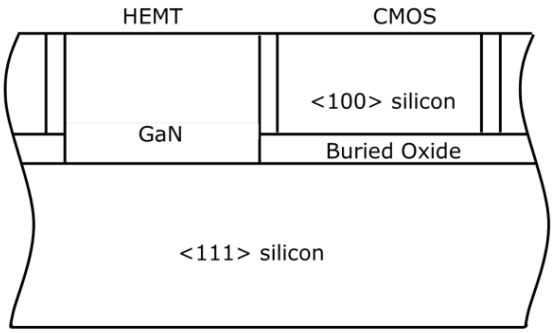

Figure 2: Schematic device cross section of the monolithic GaN in SOI approach [5]

Costs to be taken into account are for the SOI substrate material, the silicon and Buried Oxide (BOX) etch, the GaN MOCVD epitaxy and the CMOS and/or HEMT processing costs whereat not all processing layers allow for re-usage in the other domain.

Monolithic integration in GaN

In the GaN wafer process not only the single power switch can be manufactured, also further transistor(s) or diodes can be integrated to form e.g. a half bridge [9], [10]. With the integration of enhancement and depletion mode transistors NAND, NOR or NOT logic patterns can be built [11]. Just by design, mainly the gate to drain drift region spacing, transistors with different voltage rating can be realized e.g. for integrated gate drivers [12].
Today only n-channel devices are technically and commercially feasible while solutions for p-channel devices are complex and in an early state of research [13]. Additionally, the HV GaN devices will use photolithography nodes in the 180 nm to 1 µm range while for state of the art CMOS sub 180 nm geometry nodes are in use. So either the photolithography is not sufficient for CMOS logic or unnecessary small (and therefore expensive) for the GaN device. A CMOS like complexity won´t be achievable in GaN in foreseeable time.
A severe limitation of the monolithic integration in GaN will be the common silicon substrate. For operating voltages up to 200 V the common substrate is likely not an issue but it will negatively affect operation at higher voltages [14]. Overcoming this issue by the use of SOI substrates, consisting of a lower (100) handle wafer and a top (111) device or epi substrate wafer together with a trench isolation interrupting the (111) silicon substrate adds significantly to performance [15], [16], [17] but also to costs.
Costs to be taken into account are for the silicon (or SOI) substrate material, the MOCVD epitaxy and the processing including additional process step for e.g. trench etching and layers for additional devices.

Direct Wafer Bonding

Another potential integration method to combine GaN and silicon CMOS is wafer bonding [18], [19]. For the Direct Wafer Bonding, DWB, a demanding Chemical Mechanical Polishing, CMP, step is necessary to achieve the required planar surface with sub-1 nm surface topology [20], [21], [22]. The schematic complete flow is shown in Figure 3. Within a first wafer bonding step the GaN wafer is bonded to an oxidized temporary silicon carrier wafer and the (111) silicon substrate of the GaN wafer can be grinded away. After an oxide deposition onto the new surface the “GaN on temporary carrier wafer” is bonded in a second wafer bonding step onto the planarized CMOS wafer. Afterwards, the temporary carrier wafer is removed. Interconnects with sort of Through GaN Vias and a Re-Distribution Layer, RDL, connect the GaN HEMT with the CMOS.

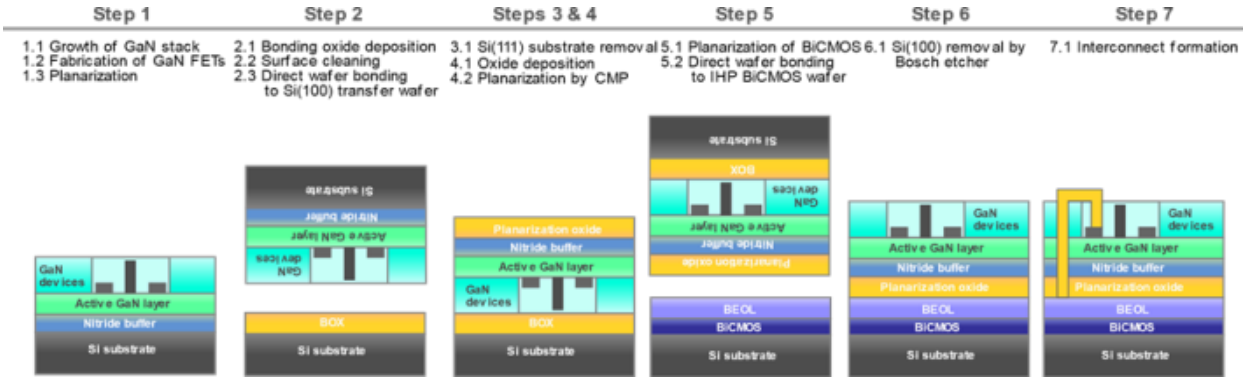

Figure 3: Schematic flow of the heterogeneous integration by Direct Wafer Bonding [20]

Costs to be taken into account are for the substrate materials, for CMOS and GaN MOCVD epitaxy, CMOS and GaN processing, additional processing layers for CMP planarization, two times the direct wafer bonding, grinding and the Through GaN Via and copper plating for the interconnects.

Micro-Transfer-Printing GaN on CMOS

For the micro-Transfer-Printing, µTP, [23] of GaN devices onto silicon CMOS the CMOS product wafer as well as the GaN source wafer are processed separately. Small GaN chiplets (e.g. consisting of a single HEMT or several HEMTs and diodes) or arrays of chiplets are picked from the source wafer with a stamp and printed on the product wafer. Final interconnect is done on wafer level by a thick RDL metal layer. This flow is shown in Figure 4. [24], [25], [26].

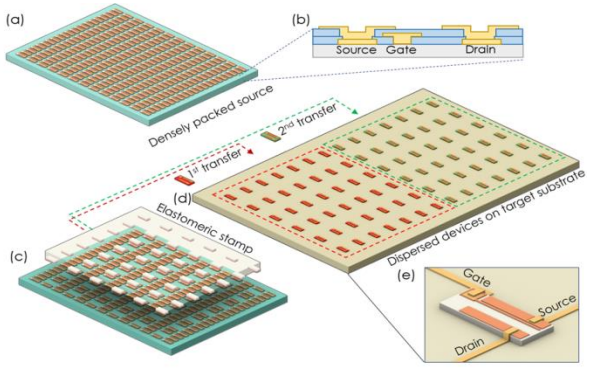

Figure 4: Schematic process flow of the micro-Transfer Printing [21]

Additional processing is needed for release, printing and interconnect. Schematic cross-sections to make the GaN HEMTs print-ready are shown in Figures 5a-c. A first trench etch step around the device removes the Inter-Metal-Dielectric, IMD, material in the Back End of Line, BEOL, layer stack. Silicon nitride is then deposited and patterned to form tethers connecting the HEMTs with an un-etched anchor region thus holding the chiplets in place when in a subsequent step the (111) silicon substrate is removed by an anisotropic wet etch. With help of an elastomeric stamp and velocity controlled adhesion the HEMTs are removed, tethers are broken, and an array of HEMTs is printed on a new substrate wafer and interconnected, Figure 5d.

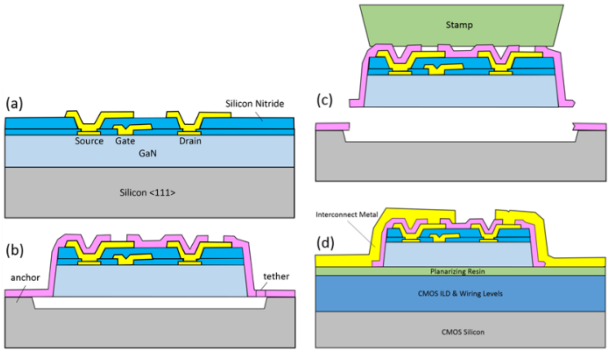

Figure 5. The process flow for heterogeneous integration of GaN HEMTs. (a) The transistors are fabricated on an <111> Si substrate. (b) The devices are isolated, passivated and then undercut. (c) The devices are retrieved with an elastomer stamp. (d) The devices are printed to a Si CMOS wafer and then interconnected using Cu RDL traces. [24]

Around the chiplets additional area is required in both x and y directions for the release trenches, typically these are designed with a width of 10microns. In one direction non under-etched area is used to form the anchor regions (Figure 5b). Figure 6 shows the dropping source wafer utilization rate at small chiplet sizes for anchor widths of 20 and 40microns versus standard 60microns scribe lane width. The wasted non-IC area is much larger for a standard scribe lane solution necessary for blade dicing than for the anchor and tether area of µTP

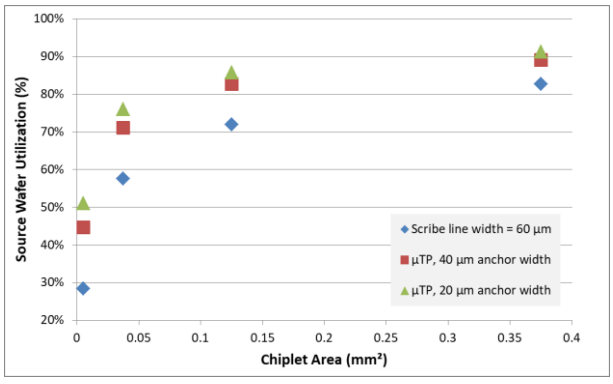

Figure 6: Source Wafer Utilization rate for scribe lane and anchor/tether chip separation

integration especially for small chip sizes.
Costs to be taken into account for the µTP process are the silicon substrates for CMOS and GaN epitaxy, the GaN MOCVD and likely CMOS epitaxy, CMOS and GaN processing, additional processing layers are required for release etch, tether formation, adhesive deposition and patterning. The costs for the micro-transfer printing are to be optimized between stamp size i.e. the number of required print steps to fully populate the product wafer and the source wafer utilization. The copper Re-Distribution Layer, RDL, needs a certain thickness to cross the chiplet height of some microns, this RDL layer potentially might substitute a CMOS via and metal layer – nevertheless full costs have been considered in the following.
A major costs advantage for micro-Transfer-Printing is that one source wafer is typically sufficient to populate several product wafers, thus the GaN source wafer costs are distributed on several product wafers and lower the costs per chip.

µTP CMOS on GaN

Using SOI technologies for the logic IC allows for release etching of CMOS chiplets, fabricated within the upper device wafer of the SOI material, vertically isolated by the BOX and laterally isolated by oxide filled trenches. The release requires a deep etch through the passivation and Inter-Metal-Dielectric, IMD, stacks as well as through the device wafer material. Either the BOX or the silicon handle wafer can then be etched away to release logic CMOS chiplets. Printing of these chiplets can be performed as shown above on top of large GaN HEMTs.
Costs to be taken into account are the silicon and SOI substrates, the GaN MOCVD epitaxy, CMOS and GaN processing, additional processing layers for release etch, adhesive deposition and patterning, the µTP and the RDL.

COST COMPARISON

An overview of the considered costs per integration approach is given in Figure 7. For all technologies 200mm wafer diameters are assumed. In detail the following costs are considered:
Silicon Substrate: Typical costs for 200mm polished substrates, (100) orientation for silicon epitaxy or (111) orientation for GaN MOCVD epitaxy.
SOI Substrate: Typical costs for bonded and etched back SOI wafer with a BOX thickness of about one micron and a device wafer layer several microns thick.
Silicon Epitaxy: Typical costs for about 10 microns thick silicon epitaxial layer.
CMOS process: A typical mask layer count of 20 layers was assumed for the basic CMOS process, additional layers for further metal layers and high voltage n- and p-channel devices are required, in total, processing costs for 30 mask layers were assumed.
GaN MOCVD: Assumed costs for a buffer and barrier GaN epitaxy suitable to manufacture HEMTs with operating voltages above 650V including p-GaN epitaxy for normally-on behaviour.
GaN process: Typical HEMT process with 15 mask layers including p-GaN gate patterning and several metal layers.
DWB: Costs for the planarization process(es), the substrate removal(s), the direct wafer bonding itself as well as the Through Silicon Via, TSV, process for interconnect via formations.
Through Silicon Via, TSV: Assumed processing costs for a sort of front side TSV process including deep di-electric and GaN etch, barrier deposition and copper plating.
µTP: Costs including the printing itself as well as costs for release steps and adhesive patterning
Copper RDL: Costs for a copper plating process, thick enough to cross the chiplet step height of several microns.
Figure 7 also mentions efforts for test and yield. In both heterogeneous integration methods (DWB and µTP) the yield of the CMOS wafer multiplies with the yield of the GaN wafer as well as with the yield of the integration process itself. For the µTP process also the

Yield loss	Yield loss	Yield loss	Yield loss	Yield loss³	Yield loss³	Yield loss³
Test	Test	Test	Test	Test	2x Test	2x Test
					Copper RDL	Copper RDL
					µ-Transfer-Printing	µ-Transfer-Printing
				TSV		
				Wafer Bonding		
			GaN Process	GaN Process	GaN Process	GaN Process
		GaN MOCVD	GaN MOCVD	GaN MOCVD	GaN MOCVD	GaN MOCVD
			Silicon Substrate	Silicon Substrate	Silicon Substrate	Silicon Substrate
CMOS process	CMOS process	CMOS process		CMOS process	CMOS process	CMOS process
Silicon Epitaxy				Silicon Epitaxy	Silicon Epitaxy	
	SOI Substrate	SOI Substrate				SOI Substrate
Silicon Substrate				Silicon Substrate	Silicon Substrate	
Bulk CMOS	SOI CMOS	Monolithic integration in SOI	Monolithic Integration in GaN	Direct Wafer Bonding	µTP GaN on CMOS	µTP CMOS on GaN

Figure 7: Cost components considered for different integration approaches

number of printed chiplets per IC needs to be taken into account since they lower the final yield.
Table 1 shows estimated final yield numbers for µTP of GaN chiplets onto CMOS ICs for typical chiplet and IC areas. The CMOS and GaN yield numbers Y were calculated using the simple Poisson model

$$Y=e^{(-A*D)}$$

defect density D assumed with 0.3 defects/cm² for the CMOS IC and 0.5 defects/cm² for the released GaN chiplet. Even with eight printed chiplets per IC and a low print yield of 90% as a worst case estimation, the calculated final yield numbers are still above 80%.

1 Chiplet / IC							
	GaN area [cm²]	0.0004	0.0008	0.0012	0.0016	0.002	
	GaN yield	99.98%	99.96%	99.94%	99.92%	99.90%	Print
CMOS area [cm²]	CMOS yield	Final yield					Yield
0.04	98.8%	97.8%	97.8%	97.8%	97.7%	97.7%	99%
0.08	97.6%	96.6%	96.6%	96.6%	96.6%	96.6%	99%
0.12	96.5%	95.5%	95.5%	95.4%	95.4%	95.4%	99%
0.16	95.3%	94.3%	94.3%	94.3%	94.3%	94.3%	99%
0.2	94.2%	93.2%	93.2%	93.2%	93.2%	93.1%	99%
0.24	93.1%	92.1%	92.1%	92.1%	92.0%	92.0%	99%
0.28	91.9%	91.0%	91.0%	91.0%	91.0%	90.9%	99%

8 chiplets / IC							
	GaN area [cm²]	0.0004	0.0008	0.0012	0.0016	0.002	
	Source GaN chiplet yield	99.98%	99.96%	99.94%	99.92%	99.90%	Print
CMOS area [cm²]	CMOS yield	Final yield					Yield
0.04	98.8%	88.8%	88.6%	88.5%	88.4%	88.2%	90%
0.08	97.6%	87.7%	87.6%	87.4%	87.3%	87.2%	90%
0.12	96.5%	86.7%	86.5%	86.4%	86.3%	86.1%	90%
0.16	95.3%	85.6%	85.5%	85.4%	85.2%	85.1%	90%
0.2	94.2%	84.6%	84.5%	84.4%	84.2%	84.1%	90%
0.24	93.1%	83.6%	83.5%	83.3%	83.2%	83.1%	90%
0.28	91.9%	82.6%	82.5%	82.4%	82.2%	82.1%	90%

Table 1: Final yield estimation for µTP of GaN chiplets on CMOS ICs for different areas, fixed print yields of 99% (top) and 90% (bottom) and one (top) or eight (bottom) chiplets per IC

The above described cost components with assumed values were then used for cost per wafer estimations of the different integration approaches for varied logic to HV or GaN switch area ratios, see Figure 8. For pure silicon solutions a hypothetical conservative factor of only ten in area was used to compare silicon and GaN high voltage transistors even when Baliga's figure of merit differs by three orders of magnitude between both materials [27], [28]. In this costs per wafer estimation only the µTP integration methods have an area ratio dependence.

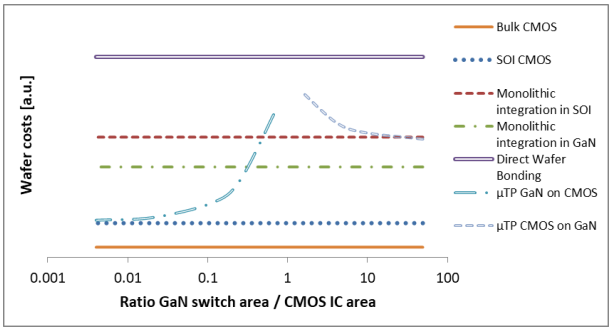

Figure 8: Different integration schemes and their costs per wafer versus area ratio CMOS IC / GaN Switch (equivalent Si HV area for bulk CMOS and SOI CMOS assumed)

Figure 9 gives the results of cost per chip estimations. Base of the estimation is a hypothetical IC with varied logic and HV or GaN switch areas. The standard CMOS solutions, SOI as well as bulk CMOS, reveal costs per chip which are growing significantly with higher switch area. The monolithic integrated solutions, in SOI as well as in GaN, have chip costs independent from the used area ratio. The integration by DWB has a cost minimum at a GaN to CMOS IC ratio of one. The µTP approaches have lightly growing costs per chip with larger GaN switch ratios.

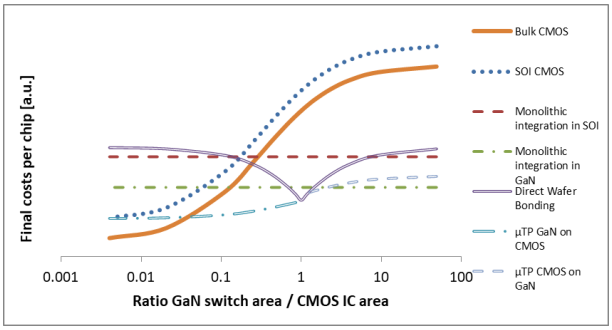

Figure 9: Different integration schemes and their costs per theoretical IC versus area ratio CMOS IC / GaN Switch

COMPARISON µTP – SOI CMOS

The commercial comparison done so far was on a pure cost per wafer base not taking functional requirements i.e. costs per performance and real application requirements, into account. To check the above cost estimation and to add also a functional comparison a cost estimation was done for different dedicated application examples requiring several high voltage switches. The replacement of (large) silicon power switches consuming a lot of IC area by (smaller) printed GaN switches with similar Rds(on) on top of the IC saves area and costs on the CMOS site but adds costs for the GaN device and the printing process.
The comparison, results are shown in Figure 10, was done for the following ICs:
A **30W DC-DC-converter.** This IC is manufactured in a 0.18µm high voltage SOI technology requiring a few 40V and 60V transistors with 0.01Ω and 0.1Ω respectively. The high voltage transistor area is more than 80% of the whole chip area in the silicon variant i.e. HV transistors and logic are placed next to each other, both requiring chip area. The printed GaN transistors on top of the logic lead to a huge chip size reduction with the GaN switches now on top of the logic. The printed switches now need 70% of a much smaller IC.
The cost adder for the release etch, printing and RDL interconnect adds about 50% additional costs. Final cost improvement is about 30%.
A **65W AC-DC-converter.** This IC is manufactured in the same 0.18µm HV SOI technology but it requires several 290V and 375V transistors with 1Ω each. The high voltage transistor area totals to about 35% of the

whole SOI chip area. The printed GaN switches consume only 5% of the IC area in the printed version. Taking into account the additional µTP and GaN costs versus the reduced HV SOI IC area the final cost reduction is almost 20%.

A **three phase Brush-Less DC (BLDC) motor driver**. This IC with on chip charge pump for floating supply generation was designed for a 1µm, 650V trench isolated SOI process. It contains six blocks of several 600V IGBTs and freewheeling diodes with a DC current capability of 4A. The 650V silicon devices to be replaced by printed GaN cover more than 50% of the total IC area in the original layout. Adding the IC area reduction to the additional µTP costs leads to a final costs reduction of more than 10%.

Eight channel controller IC. This IC was already designed for a 0.35µm bulk CMOS process with eight printed 100V, 1.1Ω HEMTs as power switches. The printed GaN needs only about 2% of the IC area. The µTP printing allows for high side configuration even on the bulk CMOS process. Replacing, theoretically, the printed HEMTs by silicon CMOS devices with similar voltage rating and on-resistance would increase the total chip area by only a few percent, cost improvement of the µTP variant is only about 2%. (But, it should be noted, high side capability as for the printed HEMT controller is not possible in this bulk CMOS technology).

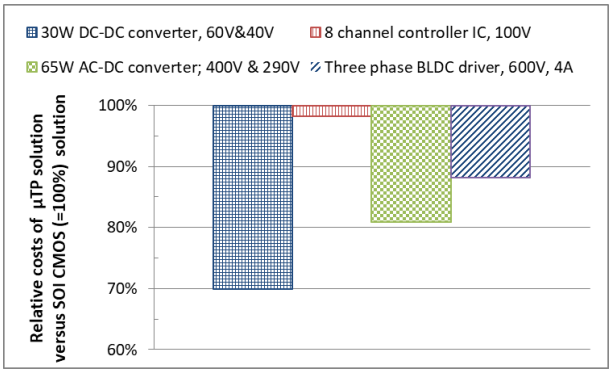

Figure 10: Costs comparison of micro-transfer-printed solution versus SOI CMOS (100%) approach

DISCUSSION

Several conclusions can be already drawn out of the more general costs estimations from Figures 8 and 9 without taking device or IC performance into account. The bulk and SOI silicon CMOS approaches have constant cost levels per wafer. On wafer level the processing effort is not affected by the ratio of high voltage switch to low voltage logic area. On chip level a large GaN switch to CMOS IC ratio as shown in Figure 9 leads to a very high area requirement for the silicon HV transistors (assumed factor of ten between GaN and silicon transistor Rdson) leading to very large IC areas and unfavourable costs when the switch area gets too large.

For both monolithic integration variants, GaN in silicon as well as logic integration in GaN, constant costs are observed per wafer as well as per chip. In both integration approaches costs are defined by substrate and processing costs and the total chip size. The difference in cost levels in Figures 8 and 9 is due to the difference of a factor of two in the assumed processing layers and the GaN MOCVD cost adder versus the SOI substrate. In both monolithic integration variants substrate and processing costs are independent from the ratio of GaN switch to CMOS IC leading to constant chip costs versus ratio in Figures 8 and 9.

Also with the Direct Wafer Bonding, DWB, constant costs can be observed when looking at pure wafer costs, i.e. the costs for two substrates and two times the processing. The costs per wafer appear very high when looking into costs per wafer. This situation changes when looking into costs per chip. Cost advantages for the DWB exist for an area ratio of about one i.e. logic IC and power switch area are about equal, due to the stacking the chip size is only half and material is used very efficiently.

The Micro-Transfer-Printing, µTP, of GaN on CMOS has its commercial sweet spot for low partitioning ratios i.e. the printed GaN switch is much smaller than the CMOS IC. Looking closer into the details it reveals that the main reason for the lower costs is due to the spreading of the quite large GaN MOCVD epitaxy costs of the source wafers over many product wafers. But for very small ratios a sort of saturation can be observed. This cost saturation is due to the required additional area for anchors in one direction and release trenches in both directions so that for very small chiplet edge lengths below 100microns the anchor and release trench area define the chiplet size, therefore the source wafer usage and therefore the costs for the printed chiplets do not further decrease.

Additionally, for small GaN chiplet areas the expected yield figures for the GaN and the release process are pretty high so that reasonable final yield numbers of above 80% can be achieved even when printing several chiplets per IC. The used defect density of 0.3 defect/cm² consider a mature CMOS process plus additional processing steps for the target wafer, the assumed defect density of 0.5 defects/cm² take into account a more complex epitaxial process, typically much less mask layers in the GaN process as well as the additional processing for the release of the chiplets. Based on these estimations potential applications and targets for further developments can be defined.

For µTP of CMOS on GaN a slight cost increase can be seen with higher GaN switch ratios. This is because here the (slightly) cheaper material is printed so that “only” the costs of the cheaper source wafer are distributed among several product wafers. Generally, µTP can lead to commercially attractive solutions when an expensive source wafer can be distributed over many cheaper product wafers.

The pure area related comparison described so far does not consider functional capabilities. Several performance limits like the poor logic functionality of

the monolithic GaN approach without complex digital logic or integrated NVM or the missing high side capability of a bulk CMOS technology might be misleading.
To check the cost per chip model four real IC designs were used to extend the basic costs per wafer and cost per chip comparison to more realistic application driven ICs. The results of these real examples can then be compared to the general cost per chip model, results are given in Figure 11.

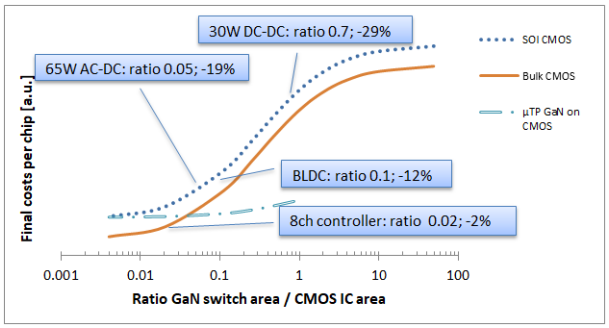

Figure 11: Adding the cost savings from Figure 11 into the expected cost model from Figure 9

The 30W DC-DC-converter is designed in a silicon SOI technology with very low ohmic 40V and 60V transistors. Due to the required low resistance the high voltage transistor area is therefore quite large and requires more than 80% of the whole chip area. Using GaN instead of the silicon HV devices reduces the HV area significantly leading to a printed GaN switch to CMOS IC area ratio of 0.7. The estimated costs savings of 30% fit very well into the general cost per chip model.
The 65W AC-DC-converter requires higher operating voltages (290V and 375V) but much smaller on-resistances and therefore a smaller area for the original silicon based HV transistors which need about 46% of the total IC area. Replacing the silicon HV transistors with printed GaN ones leads to a reduction of required HV GaN area to about 5%. The final cost reduction is almost 20% while the model also predicted cost savings lower than the previous DC-DC-converter.
The three phase Brush-Less DC (BLDC) motor driver originally needs 50% of the IC area for the HV IGBTs. In the printed GaN version the GaN transistors require only 10% of the chip area. With the estimated cost savings of 12% the real costs savings are slightly smaller than what the model would predict for a ratio of 0.1. Likely due to the better on-state resistance of the IGBT the area (and cost) saving effects of the replacement with GaN switches is slightly smaller in the real chip than what the model prediction.
The Eight channel controller IC was already designed for a bulk CMOS process with printed GaN power switches requiring only 2% of the IC area. The cost per chip model predicts a small cost increase of the µTP solution versus the bulk CMOS variant. The cost estimation of the real chip leads to a 2% cost saving. Both deviations from cost parity are rather small so that the model still gives the correct ball park number. Taking into account that all input costs are just estimations with a certain error the predicted behaviour fits very well to the real examples.

CONCLUSION

After having to a certain extend confirmed the rough cost per chip model with four examples one could use now Figure 9 to identify the commercial sweet spots for the considered integration technologies.
HV Bulk and SOI CMOS technologies are commercially competitive for small GaN switch areas. A GaN to IC area ratio of a few percent has to be "translated" into a few tens of tens of percent area ratio in these pure silicon processes which fits to the described partitioning problem.
Monolithic integration in SOI seems to be, from a pure estimated commercial point of view, less attractive. Of course technical performance or ease of handling might justify such a technology.
Especially for a large GaN area ratio **monolithic integration in GaN** has its benefits. So for applications requiring large driver areas with just some logic such a process is commercially attractive.
DWB has its commercial sweet spot for equal GaN and CMOS areas. For unequal chip sizes the unused and wasted area quickly leads to a big increase in costs.
µTP of GaN on CMOS is commercially attractive for small GaN area ratios. On the one hand side, for GaN chiplets getting too small the necessary area for anchors and tethers saturate the printable chiplet size. On the other hand the required underetch of the release process inhibits chiplet sizes getting too big.
µTP of CMOS on GaN is commercially comparable to a monolithic integration in GaN or slightly worse. The much better logic performance of a printed CMOS chiplet versus integrated GaN logic might be a big benefit.

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Singular Point Source MOS (S-MOS) Cell Concept

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Abstract

A Singular Point Source MOS (S-MOS) cell concept suitable for power semiconductor MOS based devices is presented. The S-MOS differs from a standard Planar or Trench MOS cell in the manner by which the total channel width per device area is determined. The S-MOS cell channel width is defined as the peripheral length of a line running approximately along the N++ source and P channel junction which is situated on a single gated trench side-wall. The length of the line can be established from a singular point source implant for forming the N++ source region which corresponds to the shape of the N++/P junction. The total channel width will therefore depend on the total number of gated trench side-walls per chip. Despite a relatively short channel width obtained on a single trench side-wall, narrow mesa dimensions between adjacent trenches will provide an adequate number of cells for adjusting the total channel width as required for a given device performance. The S-MOS can be realized by simple manufacturing processes and presents an alternative approach for MOS cell layouts by decoupling critical design parameters (e.g., channel width, trench dimension and NPN transistor area). This flexibility can lead to lower overall losses, lower gate charge levels, improved switching robustness and controllability for different MOS based devices.

Keywords: MOS devices, MOSFETs, Insulated gate bipolar transistors.

INTRODUCTION

MOS cell process/design platforms were developed over the years enabling advanced power devices such as the power MOSFET [1] and the Insulated Gate-Bipolar Transistor (IGBT) [2]. Both devices have been based on planar or trench MOS cells with a continuous development trend toward cell miniaturization which led to clear improvements in the overall performance over the years [3]. In particular, optimized trench gate designs target lower conduction losses and gate charge levels for optimum switching performance. Furthermore, special trench gate shielding features were also required for improving the device blocking, robustness and stability.

For IGBTs, modern structures employ Narrow Mesa trench designs for lowering the on-state losses. Typically, trench based IGBTs include non-active separation regions between active cells for lowering the channel width to achieve good short circuit capability [4][5]. However, trench IGBTs still require improvements in switching controllability especially for higher voltage devices [6][7].

On another development front with respect to wide bandgap semiconductors such as Silicon Carbide, the advances made on Silicon based MOS devices have provided a strong base for developing SiC power MOSFETs and IGBTs [8]. For SiC power MOSFETs, high cell packing densities are essential. In recent years, advanced 3D design concepts have been proposed [9] similar in a way to the low voltage lateral FINFET cell structure [10] as they rely on multi-dimensional channel width arrangements for increasing the cell density and reducing the on-state resistance R_{dson}.

In this paper, a new "Singular Point Source" MOS cell concept (S-MOS) is presented having improved design features for enabling higher performance levels when compared to standard MOS cell designs.

BACKGROUND AND NEW TECHNOLOGY

For a conventional CELLULAR type MOS cell layout design based on planar or trench gates, the channel width W_{ch} (also referred to as channel area) is defined as the total peripheral length along all the N++ source regions (or the total N++/P junction peripheral length). For LINEAR cell layouts as shown in FIG. 1 for both planar and trench MOS cells, W_{ch} is the longitudinal extension length of the N++ source in the third dimension [11]. For both cellular and linear designs, the total W_{ch} is defined by careful selection of certain mask dimensions when introducing the channel and source regions.

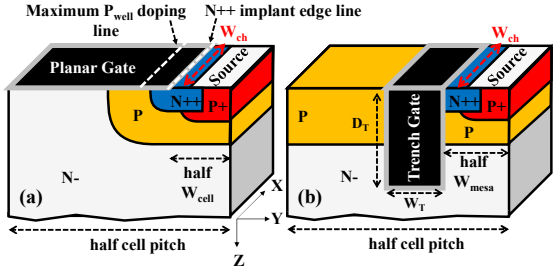

Fig. 1. Standard 3D linear Planar MOS cell (a) and Trench MOS cell (b).

It is important to note that the channel electrical characteristics are mainly defined at the highest P doping concentration positions in the P channel region. Therefore, W_{ch} is more accurately defined as the peripheral length in the P channel region where the P doping is at maximum. For linear designs, W_{ch} is defined by either the N++/P junction or the highest P doping longitudinal extension lengths since they are geometrically the same. The same rule applies for a Trench cellular layout due to the vertical channel (i.e., no lateral difference between N++/P junction and the highest P doping peripheral lengths). However, for a planar cellular layout with rounded edges (e.g., circular or hex), there is a difference since the highest P doping peripheral length is larger than the N++/P junction peripheral length.

Typically, the distance from the N++ source implant edge to the maximum P channel doping point can range from 0.3 µm to 1 µm. The S-MOS concept described in this paper is in principle based on this design feature which presents a new approach for the MOS cell design. The 3D S-MOS structure is depicted in FIG. 2 along with the critical cell dimensions. The S-MOS 2D cross section at the trench side-wall is shown in FIG. 3 along the cutline A-A` outlined in FIG. 2.

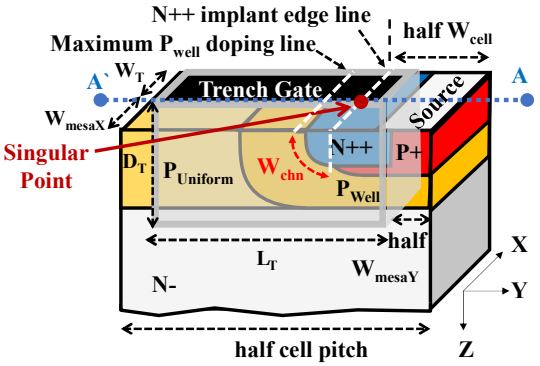

Fig. 2. Conceptional 3D S-MOS cell.

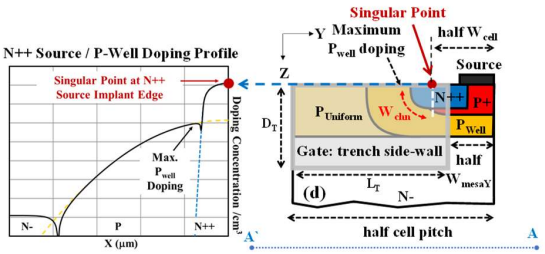

Fig. 3. S-MOS 2D cross section alone A-A` cutline in Fig.2 (at the trench side-wall) and doping concentration profile for the S-MOS P-Well version.

The key element for the S-MOS is the single unit channel width W_{chn} formed in the inversion layer of a gated trench side-wall. In this case, the channel width is not defined by a mask geometry (i.e., not an N++ extension line as in conventional designs), but is devised from a singular point source implant position which forms the N++ source and also the P-channel region (by implants through a mask and diffusion). The resulting doping profile will subsequently define W_{chn} on a single trench side-wall. The total device channel width W_{ch} becomes the sum of the W_{chn} formed on all trench side-walls. By implementing narrow mesa dimensions < 1 µm between active trench gates, the total W_{ch} is adequate for different power device design requirements.

There can be two types of P channel regions as shown in FIG. 2 and FIG. 3. This includes a P_{Well} profile similar to a P-type channel region employed in a planar design and a $P_{Uniform}$ profile similar to a P-type channel region employed in a trench design. Both P profiles can be formed by implantation and diffusion to resulting in gaussian profiles. While a P_{Well} forms a gaussian profile in both vertical and lateral dimensions from the singular point location, the $P_{Uniform}$ only forms a gaussian profile in the vertical dimension. For the later, a channel cannot form on the trench side-wall near the surface of the device as in the P_{Well} case. The S-MOS design also includes a key feature to prevent vertical trench channels from forming on the inner trench side-walls by extending the highly doped P+ base region under the N++ source. This ensures N++ protection during switching and potentially improved device robustness and stability. Furthermore, the length of the trench L_T can be adjusted to reduce the gate charge Q_G for improved switching behaviour and therefore, resulting a full or partial S-MOS trench design as described in the following section.

SIMULATION MODELS

The S-MOS concept was modelled using SILVACO 3D-TCAD software [12]. For the S-MOS proof of concept and to achieve efficient simulation time consumption, 150V MOSFET structures were modelled. On the other hand, for the reference planar and trench designs, 2D modelling was sufficient. We note that the 150V MOSFET investigation was not carried out to benchmark the structures with best-in-class equivalent devices, but as a qualitative exercise for comparing the new S-MOS with reference MOS cells concepts. For different type of MOS devices, the S-MOS will still require further optimization depending on the device type, rating and target performance.

Two S-MOS variants were investigated as shown in FIG. 4 having both a half-cell pitch of 5 µm. Design (A) employs a PARTIAL trench with a uniform type P channel doping region (L_T=1.5 µm) while Design (B) has a FULL extended trench and a P-well type channel region (L_T=4 µm). The total device thickness was 15 µm with a drift doping concentration of 1e15 /cm^3. The N++ drain had a maximum doping of 1e20 /cm^3 and depth of 1 µm. FIG. 5 shows the 3D S-MOS partial model doping concentration near the source from both sides of a half-cell unit with one trench side-wall. The P-channel region depth (main PN junction) was 3 µm deep while the

maximum doping concentration was adjusted to obtain approximately the same saturation current levels for all devices. The maximum doping concentration for the N++ source and P+ contact was set at 1e20 /cm^3 and 5e19 /cm^3 respectively. The 2D planar design has a cell opening W_{cell} of 2 µm while the 2D trench design had a W_{mesa} of 1 µm. The S-MOS has a trench mesa W_{mesaX} around 0.5 µm (between orthogonal trenches) and a trench mesa W_{mesaY} around 1 µm (i.e., the half-cell in X dimension = 0.75 µm). The S-MOS W_{cell} was set at 2 µm (distance between two singular points) while the P+ region extended laterally below the N++ source to ensure channels are only formed on the trench side-walls. All trenches had a width W_T of 1 µm and depth D_T of 5 µm.

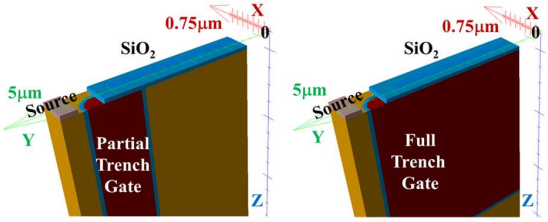

Fig. 4. 3D S-MOS models with partial (a) and full (b) trench.

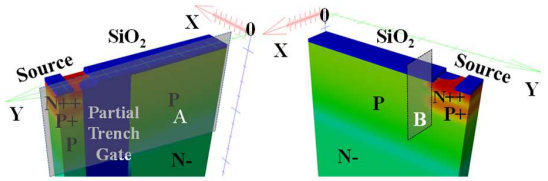

Fig. 5. 3D S-MOS Partial trench doping concentration (two sides of cell unit).

SIMULATION RESULTS AND DISCUSSION

For a 1 cm^2 scaled MOSFET, the linear planar and trench models had a total W_{ch} of 20 meters. For the S-MOS models, the W_{ch} per trench side-wall was approximately 0.75 µm leading to a similar total channel width W_{ch} per 1 cm^2 as for the reference devices. The channel parameters were adjusted to achieve similar saturation currents for all devices as shown in FIG. 6 for the IV output characteristics curves at 300K. At V_{gs}=10V. The S-MOS has an R_{dson} value similar to the trench device below 6 mohm/cm^2 when compared to the planar MOSFET which is around 8.6 mohm/cm^2. The full Trench S-MOS show the lowest levels below 5 mohm/cm^2. The S-MOS TCAD model for the patrial trench electron concentration at 2V is shown in FIG. 7. To better visualize the S-MOS during conduction, the cut planes A and B outlined in FIG. 5 are presented in FIG. 8 for the electron concentration. Cut A is at 0.5 µm in X direction (at the inversion layer of the trench side-wall) and cut B at 3.5 µm in Y direction (at the highest P channel doping). The figure show that the P+ base region placed under the N++ source region ensures no trench MOS channel is formed on the inner trench walls as explained earlier.

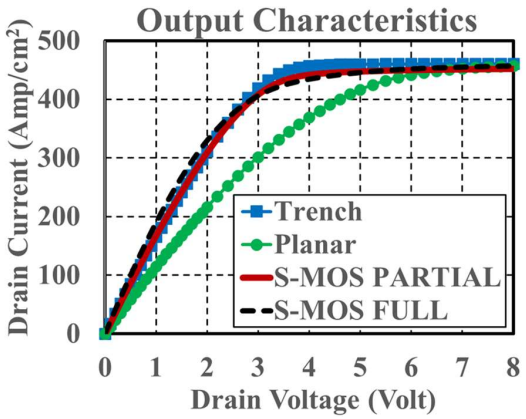

Fig. 6. 150V MOSFET IV output characteristics at 300K.

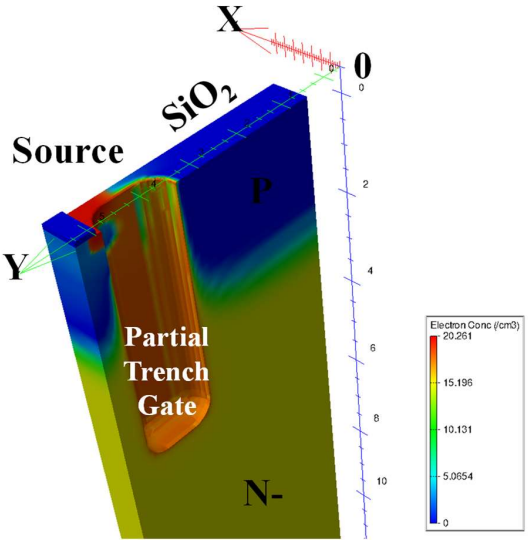

Fig. 7. 3D S-MOS partial trench electron concentration distribution at 2V, 300K.

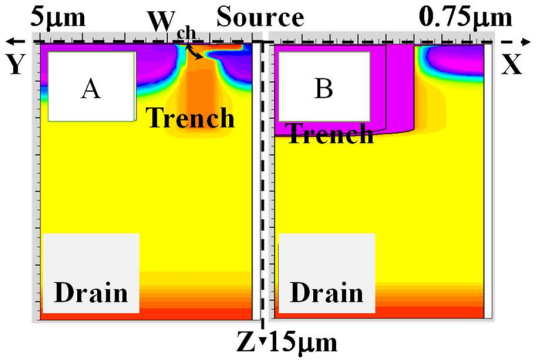

Fig. 8. S-MOS partial trench 2D cut sections cut A and B as shown in FIG. 5 for the electron concentration at 2V.

The IV transfer characteristics at 300K are shown in FIG. 9. All devices display normal behaviour with S-MOS devices exhibiting lower threshold voltage levels compared to reference devices due to higher current densities at the channel formed at trench gate oxide - planar gate oxide corner.

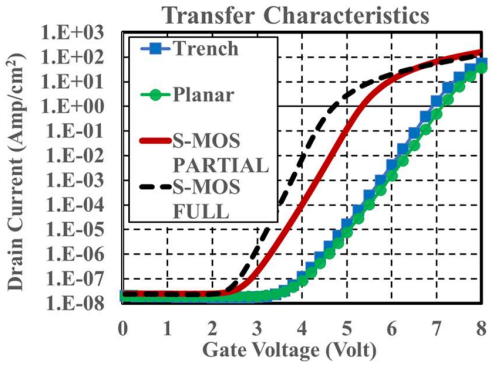

Fig. 9. 150V MOSFET IV transfer characteristics at 300K.

The IV blocking characteristics at 300K are shown in FIG. 10. The S-MOS shows higher blocking capability when compared to the trench MOSFET but still lower than the planar MOSFET. Trench devices typically show lower blocking due to the presence of the higher peak electric field associated with the trench bottom corner as shown in FIG. 11 for the Partial trench S-MOS at 150V.

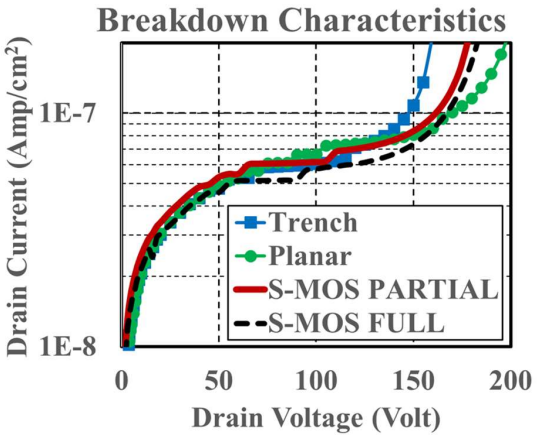

Fig. 10. 150V MOSFET IV breakdown characteristics at 300K.

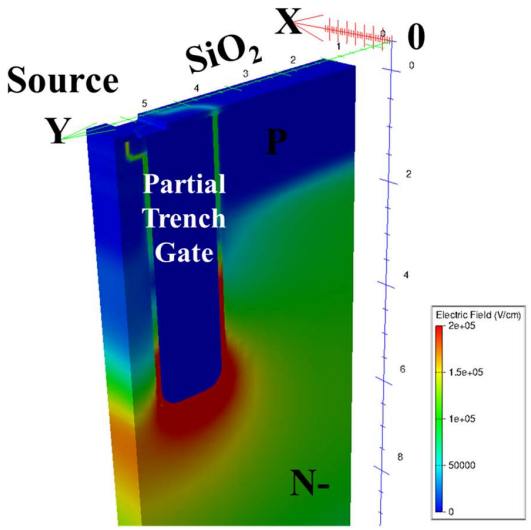

Fig. 11. 3D S-MOS partial trench electric field distribution at 150V, 300K.

Resistive switching results at 300K were obtained for all devices at V_{gs}=10V, DC voltage of 75V and a current of 100 A/cm^2. FIG. 12 and FIG. 13 show both the turn-off and turn-on current and voltage waveforms under such conditions respectively. For the same gate resistance R_G=1ohm, the devices show different switching behaviour which is dependent on the device input capacitance and gate charge levels. During turn-off, the much larger gate capacitance of the full trench S-MOS shows long delay times while the partial version matches that of the standard trench MOSFET. The planar device shows the shorter delay time as expected. During turn-on, the trench MOSFET deviates in the performance with slower di/dt and voltage fall times.

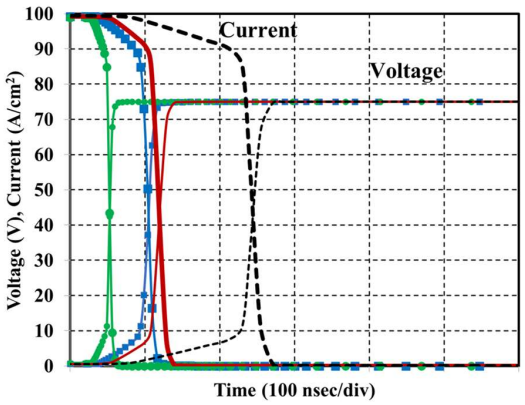

Fig. 12. 150V MOSFET turn-off resistive switching curves at 300K, 75V, 100A/cm^2 and R_G=1ohm.

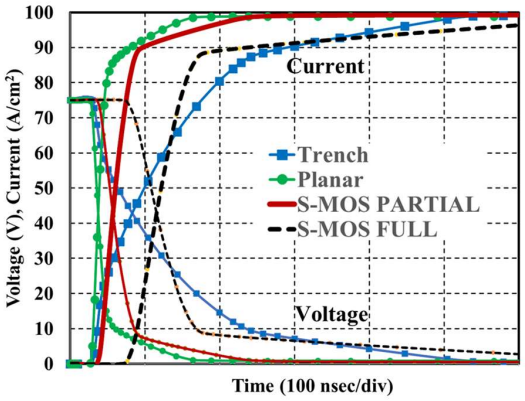

Fig. 13. 150V MOSFET turn-on resistive switching curves at 300K, 75V, 100A/cm^2 and R_G=1ohm.

To understand the switching behaviour obtained from the mixed mode simulations, the Gate Charge Q_G curves (V_{ge} versus Q_G) were extracted during the turn-on transient as shown in FIG. 14. The effect of L_T is clearly demonstrated showing that the S-MOS with partial trench can lead to low gate charge levels similar to those reach with trench gate designs. However, much lower turn-on losses can be achieved with the S-MOS concept due to the lower miller voltage plateau associated with this cell design as shown in FIG. 14.

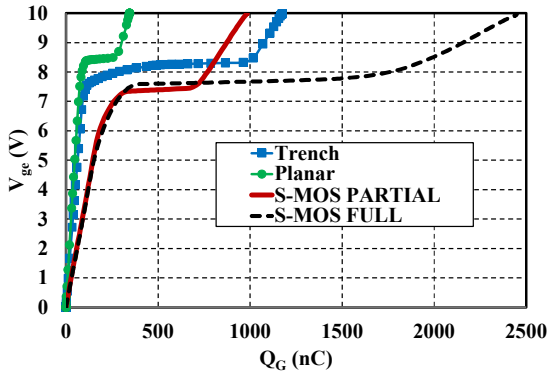

Fig. 14. 150V MOSFET turn-on resistvie switching associated Gate Charge curves at 300K.

A full summery of the static and dynamic parameters is provide in Table .1. It is clear that the switching losses of the partial S-MOS are much lower than the trench device while at the same time providing similar and low R_{dson} levels. Therefore, in principle, the S-MOS concept has the potential to provide benchmark performance after carful design optimisation and in relation to a given MOS based device concept.

Device	R_{dson}(ohm/cm^2)	V_{th}(V)	V_{bd}(V)	E_{on}(µJ)	E_{off}(µJ)	Q_G(nC)
Trench	0.00591	5.75	160	460	55	1175
Planar	0.00863	6	200	155	25	346
S-MOS PAR	0.00578	4.4	180	165	55	984
S-MOS FULL	0.00486	3.8	185	360	135	2308

Table 1. 150V MOSFET parameters under static and dynamic conditions at 300K (Switching: 75V, 100A/cm^2 and R_G=1ohm)
.

S-MOS OUTLOOK: Si IGBT and SIC MOSFET

To explore the potential of the S-MOS cell on high voltage devices, the new design was simulated for a 1200V IGBT 3D structure and compared to the latest Narrow Mesa Trench NM-IGBT designs having a W_{mesa} down to 1 µm [13]. For this case, the IGBT investigation provides an insight into the S-MOS behaviour for a bipolar device. A full and partial S-MOS trench design was implemented albeit with a P_{Well} doping profile as shown in FIG. 15. The S-MOS was capable of matching the NM-IGBT static performance in terms of conduction losses while also providing lower switching losses along with higher blocking capability. A full set of static and dynamic simulation results can be found in the referenced publication.

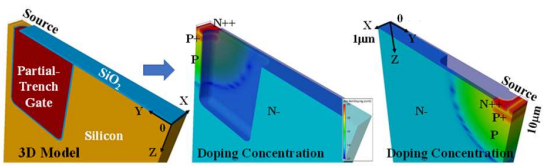

Fig. 15. 3D 1200V S-MOS IGBT model and net doping concentration.

The next step was to carry out the simulation study for a 1200V Silicon Carbide SiC MOSFET 3D structure as shown in FIG 17. Initial results show promising performance as shown in FIG. 18 for the IV output characteristics. The S-MOS is compared to a planar SiC MOSFET at 425K for a 1 cm^2 active area device. The S-MOS provides an R_{dson} around 3 mohm/ cm^2 compared to 5 mohm/cm^2 for the planar MOSFET. The full set of results will be published in a future article [14].

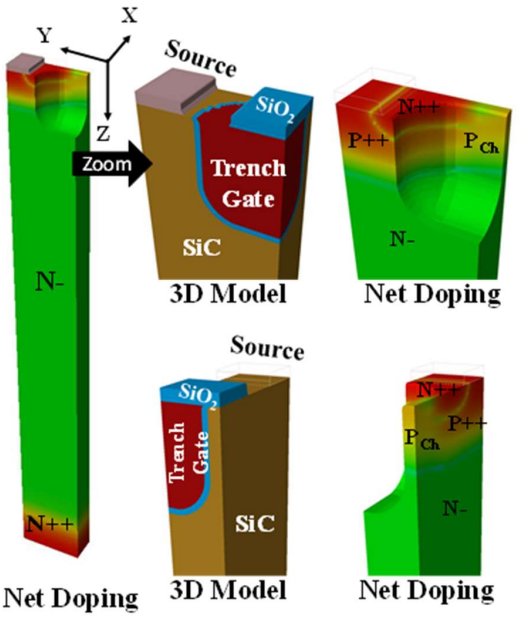

Fig. 17. 3D 1200V S-MOS SiC MOSFET model and net doping concentration.

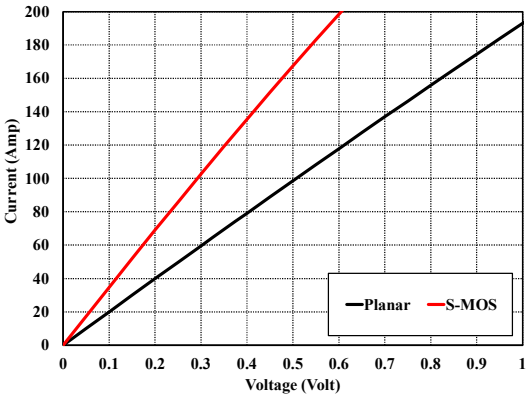

Fig. 18. 1200V SiC MOSFET IV output characteristics at 425K.

CONCLUSIONS

A new S-MOS cell concept was presented showing an alternative method to define and control the channel width in MOS based devices. The new approach can lead to simple manufacturing processes and improved overall performance. 3D simulation results confirm the

functionality of the S-MOS concept for a 150V power MOSFET compared to standard planar and trench devices. An outlook towards the implementation of the S-MOS platform for silicon IGBTs and Silicon Carbide MOSFETs was also provided.

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Scalable Vertical GaN FETs (SV- GaN FETs) for Low Voltage Applications

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Abstract

This is the first report on a novel multi-polarization channel applied to realize normally-off and high-performance vertical GaN device devices for low voltage applications. This structure is made with 2DHG introduced to realize the enhancement mode channel instead of p-GaN as in conventional vertical GaN MOSFETs. As the 2DHG depends upon growth conditions, p-type doping activation issues can be overcome. The Mg-doped layer is only used to reduce the short-channel effects, as the 2DHG layer is too thin. Two more 2DEG layers are formed through AlGaN/GaN/AlGaN/GaN polarization structure, which minimizes the on-state resistance. Simulation analysis shows that this proposed structure can provide a large drain current at ~ 500 mA/mm level. The calculation results show this novel vertical GaN MOSFET – termed as SV GaN FET - has the potential of breaking the GaN material limit in the trade-off between area-specific on-resistance ($R_{(on,sp)}$) and breakdown voltage at low voltages.

Keywords: 2DEG, 2DHG**,** Low Voltage, Scalable Vertical GaN FETs (SV- GaN FETs)

INTRODUCTION

Due to its capability for higher efficiency, Gallium Nitride (GaN) is widely considered as the next generation pervasive semiconductor that can help address global challenges of climate change, energy security, health, and connectivity. Replacing silicon with GaN has the potential to reduce power loss by 80%, chip size by 90% at 600V and meet the performance/cost parity demanded by Integrated Circuit (IC) industry. Moreover, GaN has great potential to reduce cost because GaN device can be fabricated on epitaxy grown substrate that is larger and less expensive than Silicon Carbide (SiC).

Polarization Super Junction (PSJ) technology has been recently introduced and applied on GaN HEMT devices. It breaks the trade-off between area-specific on-resistance ($R_{(on,sp)}$) and breakdown voltage in lateral formats [1, 2]. However, in most lateral GaN transistors, threshold voltage could not be increased to a high enough level (except through cascode approach) to satisfy the requirement of automotive applications [3]. For high-frequency applications, dynamic on-resistance in lateral GaN devices can degrade device/system efficiency due to increased conduction losses [4]. Besides, most lateral GaN devices are not as area-efficient as vertical GaN transistors since sufficient length between the gate and drain electrodes is necessary to achieve high blocking capability [5]. In vertical GaN MOSFET technology, p-type GaN is usually doped by magnesium (Mg) and the percentage activation of this impurity rarely exceeds 1%. Moreover, the fabrication and performance of high voltage GaN MOSFET structures are dependent on p-GaN doping techniques [6, 7]. To overcome such technical limitations, our innovative idea is to expand the PSJ concept to Scalable Vertical (SV) GaN FETs.

VERTICAL DEVICE STRUCTURE AND DEVICE SIMULATION

Silvaco TCAD is used for 2D device simulation of SV-GaN FETs. The models adopted for simulating I-V characteristics includes POLAR (spontaneous polarization), CALC.STRAIN (piezoelectric polarization) and FLDMOB (field-dependent mobility).

Fig. 1 shows a simplified SV- GaN FET with 10nm $-$ $Al_{0.05}Ga_{0.95}N$ / $5nm - GaN$ / 10nm $-$ $Al_{0.05}Ga_{0.95}N$ / $5nm - GaN$ channel. There are two 2DEG layers: the

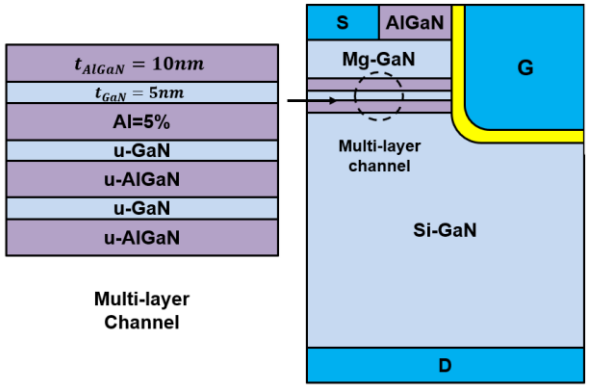

Fig. 1. Multi polarization channel vertical GaN device cross-section

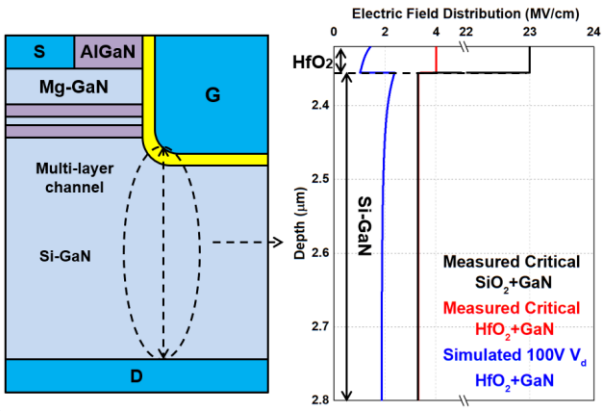

Fig. 2 Gate corner electric field distributions: simulated results vs. measurement material critical electric field [8, 9].

upper layer is connected to the source electrode while bottom 2DEG layer is connected to drain electrode. 2DHG presence in multi-layers is regarded as the channel with the function of realized normally off and controlled threshold voltage. 2DEG and 2DHG sheet carrier density can be controlled by adjusting AlGaN layer thickness and Al mole fraction.

The channel design of multi-layer stacks utilizes a charge compensation concept between the adjacent 2DEG and 2DHG layers to support voltage. The applied voltage is dropped across the stack as well as the Si-doped GaN drift region. BV can be scaled by increasing the number of multi-layer stacks or optimizing the thicknesses of the stacks. In trench gate vertical devices, corner design is an important issue that affects operation reliability. In this work, reported data of measured critical electric field strength of $\sim 4MV/cm$ $(23MV/cm)$ for HfO_2 (SiO_2) and $3.3MV/cm$ for Si-GaN is used as the reference values and U-shaped design is considered for the gate geometry to suppress corner effects [8, 9].

Fig. 2 shows that a SV- GaN FET device with $0.5\mu m$ Si-GaN drift region is simulated at 100V drain voltage, the peak electric field is the only 2/3rd of the reference value. Moreover, other techniques such as p-GaN underneath the gate can further electrically shield the gate corners. As shown in Fig. 3, an Mg-doped GaN region applied

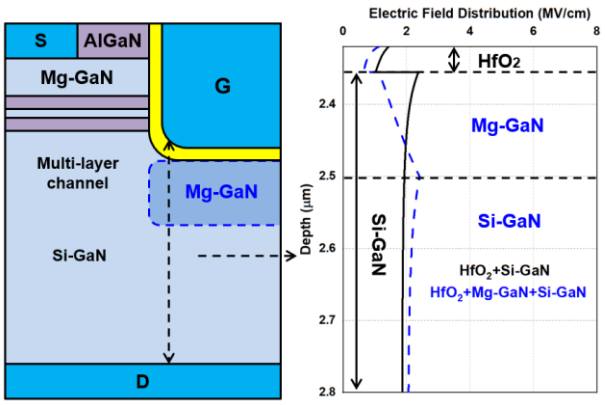

Fig. 3 Gate corner electric field distributions: Si-GaN vs. Mg-GaN+Si-GaN at $V_d = 100V$.

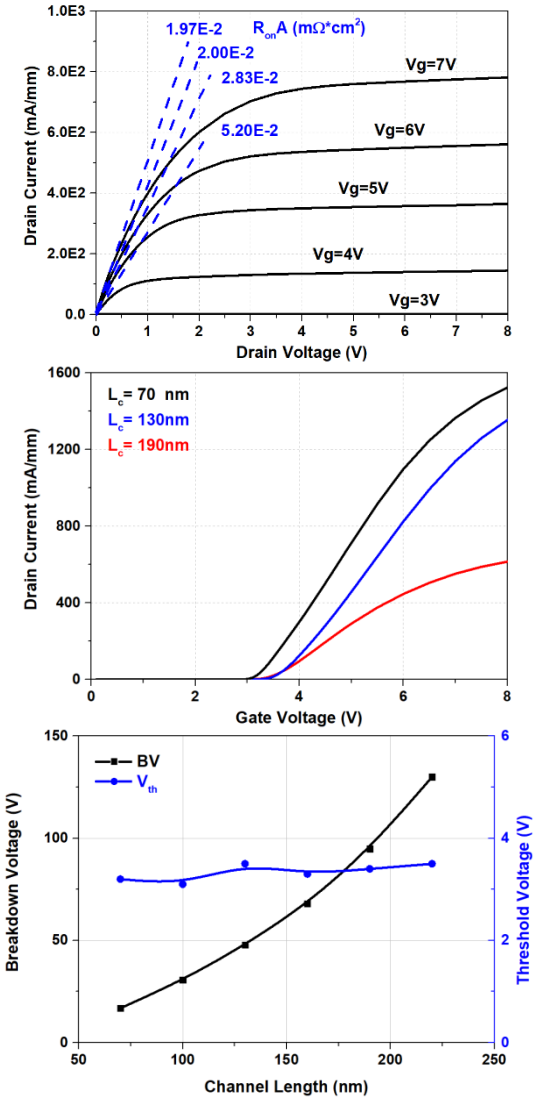

Fig. 4 Simulated (a) $160\mu m$ channel $I_d - V_d$ characteristics. (b) Transfer I-V characteristics. (c) Channel length vs BV and V_{th}

beneath the trench gate can further suppress the electric field crowding at the corner of the gate.

Fig. 4(a) shows the $I_d - V_d$ characteristics as a function of gate voltage. With the increasing number of multi-polarization junction stacks, device blocking capability can be improved without any significant increase in V_{th}, as shown in Fig. 4(c).

In Fig. 5, for comparison, 4H-SiC and GaN material theoretical limits are demonstrated as well as conventional GaN HEMT with $1\mu m$ channel length [10]. The calculation results show a performance beyond the material limit by assuming ideal channel mobility of 1000 cm^2/Vs. The simulation results for SV-GaN FETs predict significantly superior performance to conventional lateral GaN HEMT, albeit practical carrier mobility is utilized for calibration. Vertical GaN devices based on PSJ concept will be a promising candidate for the next generation of power electronics.

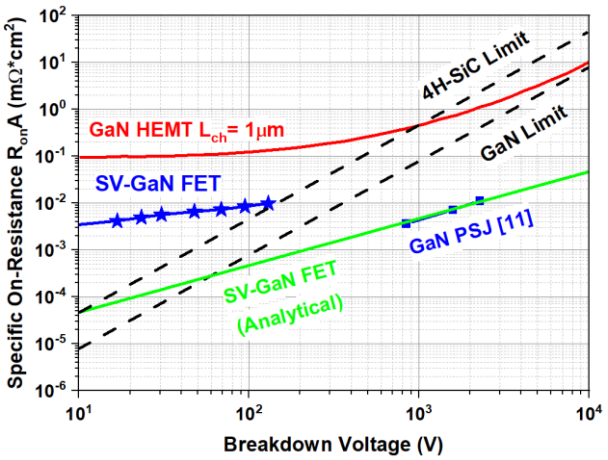

Fig. 5 Area-specific on-resistance vs. Breakdown trend in GaN and SiC; for reference vertical GaN PSJ technology [10] is shown as well as the predicted trend of SV-GaN FET.

CONCLUSIONS

A novel vertical GaN MOSFET technology, which can be scaled and suitable for low voltage applications, is presented herein. A 100V device can potentially achieve a $R_{(on,sp)}$ lower than $10^{-2} m\Omega \cdot cm^2$ as shown in this work. The device can be easily scaled, and the specific on-state resistance can be further optimized with more refined design rules. Based on the results presented, the multi-polarization channel vertical GaN device are predicted to offer immense potential in power electronic systems and high frequency integrated applications.

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Fast Short Circuit Type I Detection Method based on V_{GE}-Monitoring

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Abstract

In this paper, a Short Circuit type I detection method based on the monitoring of the gate voltage is investigated. The proposed detection principle relies on an existing method, which was realized as an integrated solution before. A modified discrete circuit solution is introduced, developed and tested. Moreover, measurements and investigations on different packaging concepts and test conditions are performed. The overview of the functionality, reliability, and restraints of this method, as well as aspects of a supposed dynamic self-adaption feature, are discussed.

Keywords: IGBT, Short Circuit Detection, Gate Drive Unit

INTRODUCTION

A low inductive Short Circuit type I (SC I) event, also known as Hard Switching Fault (HSF), appears when a power transistor is turned on to an already shorted load. It is a critical situation that should be detected and turned off as fast as possible, especially for transistors with reduced short circuit capability, such as on-state-optimized IGBTs [1] [2].

The failure detection based on the desaturation of the power transistor is a well-known and reliable solution but lacks a fast detection time due to the necessity of a blanking time. It also requires space for the circuitry because of the use of high voltage blocking diodes or ohmic-capacitive dividers [3].

Several alternative approaches based on the monitoring of different quantities were proposed. They either interpret one quantity solely, e.g. the load current slope di/dt [4], the Gate-Emitter voltage V_{GE} [5] [6], or more than one quantity in combination. A 2-D detection presented and described in [1] [2] [7] is based on the simultaneous monitoring of both the load-current transient di_C/dt and the gate voltage V_{GE}. In addition, a detection combining a V_{GE} and V_{CE} evaluation was published in [8].

This paper provides an overview of an SC I detection method which is based solely on the monitoring of the gate voltage of the transistor. The SC detection principle was first introduced in [5], where it was realized via an integrated circuit. In this paper, a modified discrete circuit solution is developed and tested. Moreover, investigations on different packaging concepts and test conditions are shown, to provide a more complete overview of the functionality, reliability, restraints, and features of this method.

FUNCTIONAL PRINCIPLE

The detection circuit, which monitors the course of the Gate-Emitter voltage V_{GE} during the turn-on transition of the IGBT, is depicted in the bottom part of Fig. 1. For a normal turn-on process, the Miller-plateau can be observed in the V_{GE} course caused by the decreased Collector-Emitter voltage V_{CE}, which will not take place due to the permanently high V_{CE} voltage under low inductive SC type I conditions. This effect was already discovered and used for detection schemes in [9] and [10]. However, for a high inductive SC type I, a Miller-plateau would be observed due to the transient decrease of V_{CE}. Therefore, the proposed method would not work reliably for the latter case.

V_1 and V_2 describe the voltage level of the capacitors C_1 and C_2, respectively. When the IGBT receives the turn-on signal, C_1 and C_2 are individually charged by the currents I_1 and I_2. I_1 is adjusted higher than I_2, which results in a higher charging speed of V_1 for $C_1 \approx C_2$. Two reference levels V_{Ref1} and V_{Ref2} are defined to stop the charging process of V_1 and V_2, respectively. V_{Ref1} is set below the Miller-plateau level V_{Miller}. Meanwhile, V_{Ref2} is fixed slightly lower than the steady-state value of the positive gate voltage. V_1 stops rising at time t_1 when V_{GE} reaches the value of V_{Ref1}. Similarly, V_2 stops to increase at t_2, when V_{GE} reaches the value of V_{Ref2}. The values of V_{GE} and the reference voltages V_{Ref1} and V_{Ref2} are halved to become processible by the comparators. For V_{GE} this is enabled via an ohmic voltage divider. V_1 and V_2 can be held across C_1 and C_2 by employing two Schottky diodes D1 and D2. At t_2, V_1 and V_2 are compared by Comp3.

The working principle is depicted in the schematic drawings in Fig. 2 and Fig. 3 for a faultless and an SC I turn-on process under consideration of idealistic courses

for V_1, V_2, and the Fault-Signal V_{Fault} as well as typical courses of V_{GE}.

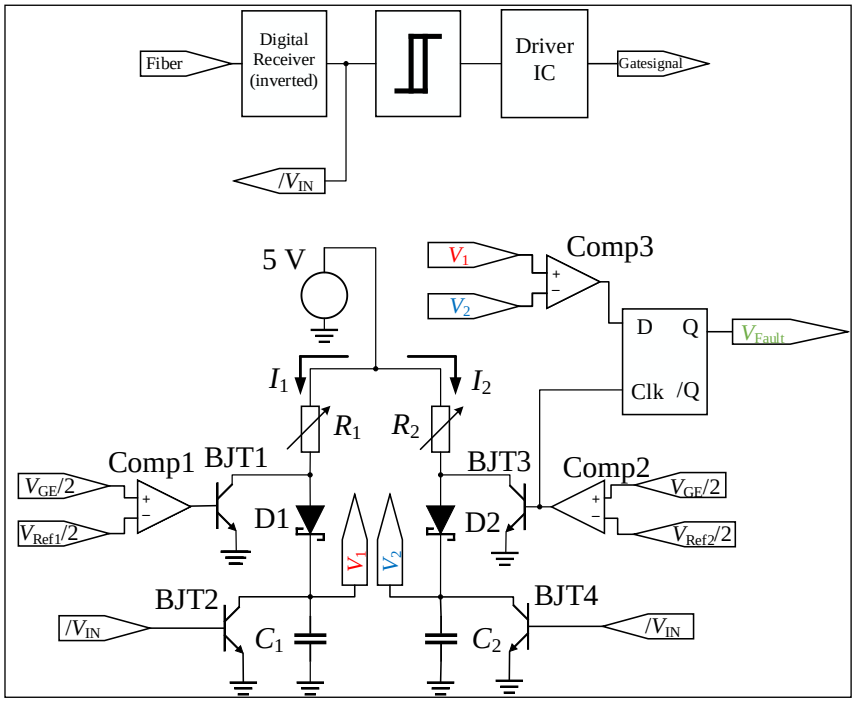

Fig. 1: Gate-signal-path (top) and detection circuit (bottom).

Under normal turn-on conditions, the relation (1) is applied due to a longer charging time t_2 of V_2, see Fig. 2:

$$V_1 < V_2 | t = t_2 \quad (1)$$

Therefore, (2) holds, see Fig. 3. This results in a fault signal V_{Fault} when the gate voltage reaches V_{Ref2}:

$$V_1 > V_2 | t = t_2 \quad (2)$$

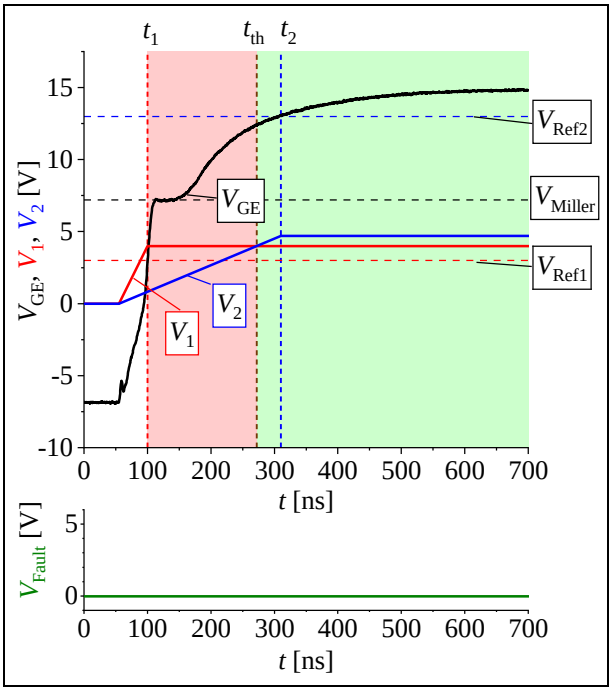

Fig. 2: Working principle with idealistic courses for V_1, V_2 (top), and V_{Fault} (bottom) under normal switching operation.

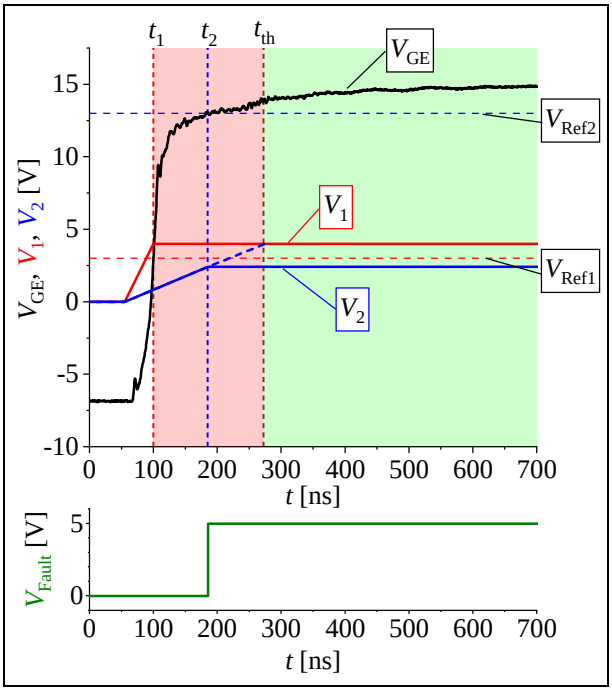

Fig. 3: Working principle with idealistic courses for V_1, V_2 (top), and V_{Fault} (bottom) under SC I turn-on conditions.

On the contrary, under SC conditions V_2 does not have enough time to reach the value of V_1, because the rise of V_{GE} is faster without the Miller-plateau.

The threshold time t_{th} is the time when V_2 exceeds V_1. Since t_{th} is dependent on the rise time t_1 of V_1, t_{th} should automatically be adjusted to a certain value according to the slope of the V_{GE}-course during turn-on. This potentially enables a self-adaption which will be discussed in a later section.

MEASUREMENT SETUP

To prove the detection method´s working principle, application-conform measurements representing normal and SC I turn-on transitions are performed. The load circuit is depicted in Fig. 4. The low-side switch being protected is subjected to a normal turn-on process during the double pulse test. In this case, the high-side consists of a load inductivity L_{Load} and an antiparallel freewheeling diode FWD. For the SC I test, the high-side is shorted before the turn on. The gate voltage is reduced to half by an ohmic voltage divider consisting of two resistors R_{div}, to prevent the comparator input voltage from exceeding the allowable range.

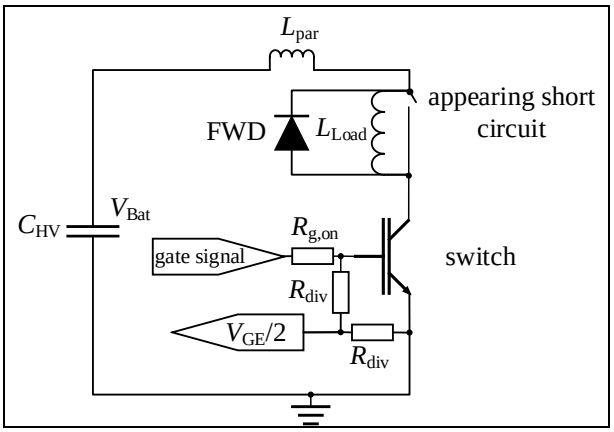

Fig. 4: Load circuit and parts of the gate signal loop for double pulse and SC I test.

The investigations have been carried out with IGBTs in TO-247-3 and EconoPACK-housing from Infineon. In Fig. 5, the proposed circuitry and the module are shown. The PCB on the lower left part of Fig. 5 represents the driver for the switch and its detection circuitry. It was used in this paper for testing IGBTs in both packages as mentioned before.

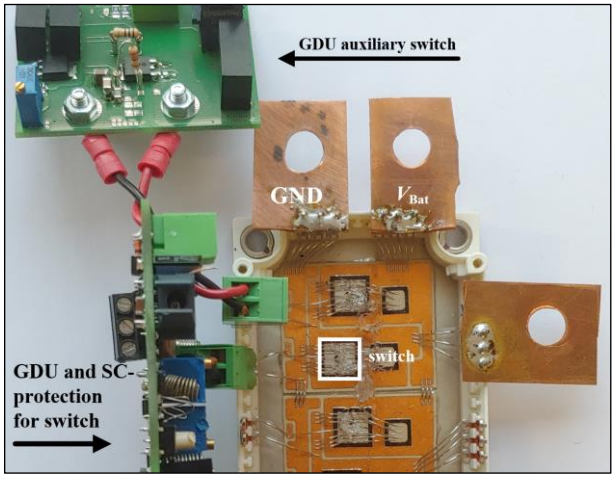

Fig. 5: Connection between EconoPACK-module with Gate Drive Unit (GDU) and detection circuit (bottom left).

MEASUREMENTS FOR GENERAL VALIDATION

In this section, the general working principle and detection accuracy of the method is demonstrated and proved. The following measurements have been generated using an IGBT-module FS75R17KE3 from Infineon in EconoPACK-housing under application-compliant conditions with reference voltages set to V_{Ref1} = 3.8 V and V_{Ref2} = 13.8 V.
For the non-fault case (1) see Fig. 6. There is no fault signal given.

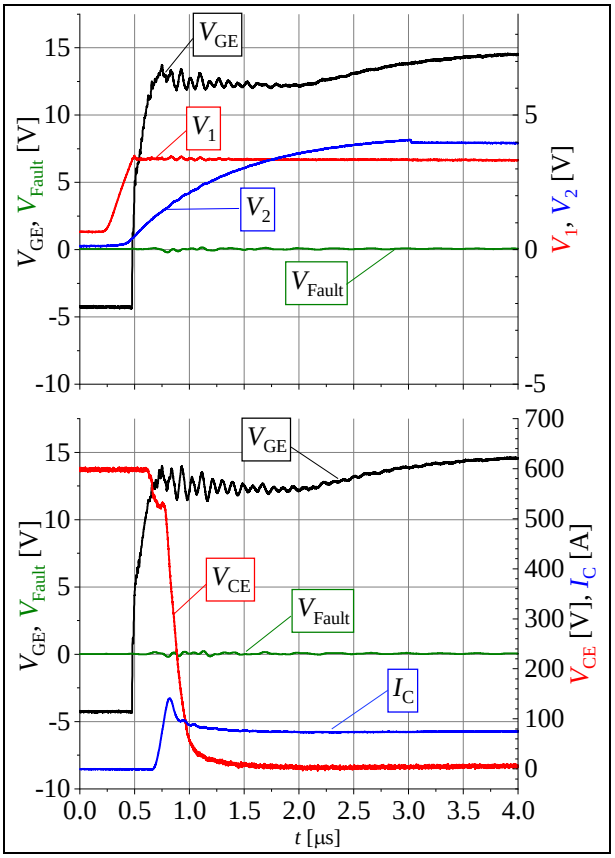

Fig. 6: Courses of detection circuit V_1, V_2 (top), load circuit V_{CE}, I_C (bottom), V_{GE}, and V_{Fault} during normal turn-on process. V_{Bat} = 600 V, I_C = 75 A, $R_{g,on}$ = 6.4 Ω, L_{Load} = 500 µH, L_{par} = 70 nH; EconoPACK-module.

For all the partial figures showing measurements, V_{GE} is always measured and depicted to demonstrate its relation to V_1 and V_2 or V_{CE} and I_C. V_{Fault} is always shown to prove its validity for each measurement.
At the beginning of the Miller-phase LC-oscillations are visible in the V_{GE} signal excited by the di_C/dt during the current rise and Reverse Recovery event of FWD. Regarding the stray inductance in the gate-loop, the connection between the GDU-detection board and the module is not realized ideally, as can be seen in Fig. 5. However, this does not affect the functionality of the detection circuit concerning the correct classification of a normal turn-on event. Nevertheless, an optimized gate loop design could mitigate this issue.

A successfully detected SC measurement under the same conditions as before is shown in Fig. 7. After turning on for around 300 ns, a short circuit is detected under given measurement conditions.

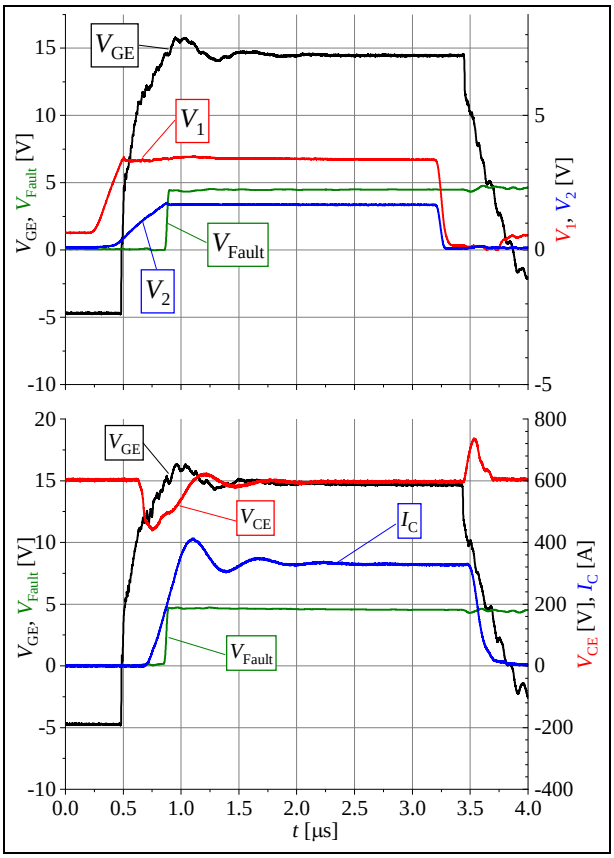

Fig. 7. Courses of V_1, V_2 of the detection circuit (top), V_{CE}, I_C of the load circuit (bottom), and V_{GE} and V_{Fault} during SC I. V_{Bat} = 600 V, I_C = 75 A, $R_{g,on}$ = 6.4 Ω, L_{Load} = 500 µH, L_{par} = 70 nH; EconoPACK-module.

The first measurements shown in Fig. 6 and Fig. 7 demonstrate that the proposed detection method can successfully distinguish between a normal and a failure turn-on. The detection offers a valid fault signal even before the static value of the positive gate voltage and short circuit current is attained. The detection mechanism can also be used within a 2-level turn-on procedure, where the full positive gate voltage is only released when no fault has been detected in the first turn-on step.

INVESTIGATION ON PACKAGES WITH AND WITHOUT A SENSE PIN

The evaluation of the behavior of the short circuit detection has not only been carried out on modules in EconoPACK-housing but also on devices in TO-247-3 package. Fig. 8 shows the behavior during a normal turn-on process using an IKW20N60T IGBT from Infineon under application relevant conditions. It is visible that, similarly to the EconoPACK-operation, oscillations occur from the appearance of the di_C/dt at turn on. Furthermore, the measured gate voltage V_{GE} is subjected to a transient increase at the beginning of the Miller-phase between 300 and 350 ns.
Although the current slope di_C/dt for the TO-package is lower compared with the module, a more pronounced V_{GE} overshoot during normal turn-on can still be observed.

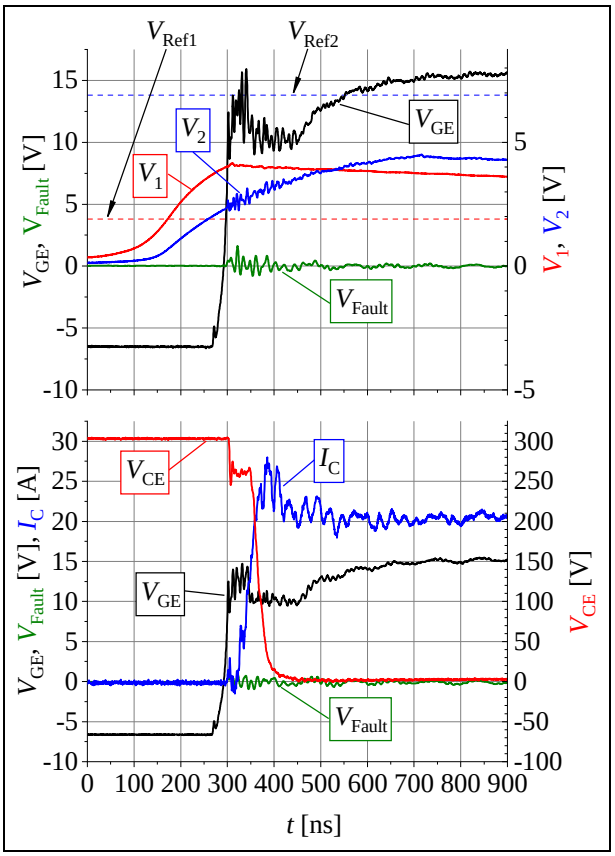

Fig. 8: Courses of V_1, V_2 of the detection circuit (top), V_{CE}, I_C of the load circuit (bottom), and V_{GE}, V_{Fault} during normal turn-on process. V_{Bat} = 300 V, I_C = 20 A, $R_{g,on}$ = 6.2 Ω, L_{Load} = 500 µH, L_{par} = 80 nH; TO-247-3-package.

The reason for this phenomenon can be found in the different structures of the two packages. Fig. 9 shows the gate loop of the module and how it is affected by a positive load current transient di_C/dt.

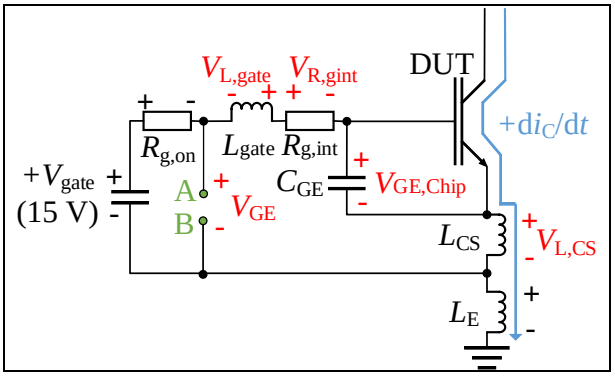

Fig. 9: Structure of the gate loop for a package or module offering a Kelvin sense contact.

The measured gate voltage V_{GE}, which also constitutes the voltage signal being monitored by the detection circuit before division, is picked off at terminals A and B.

During the occurrence of a collector current slope, V_{GE} does not correspond to the real chip-internal gate voltage $V_{GE,chip}$. Across the stray inductance in the gate loop L_{gate} and the common-source inductance L_{CS} affected by the gate current slope and the collector current slope respectively, additional voltages are induced:

$$V_{GE} = V_{R,gint} + V_{GE,chip} + V_{L,CS} - V_{L,gate}. \quad (3)$$

As

$$V_{L,CS} + V_{R,gint} > V_{L,gate} \quad (4)$$

applies, (5) holds.

$$V_{GE} > V_{GE,chip} \quad (5)$$

In contrast to the EconoPACK-module, a 3-pin TO-package is not provided with a separate Kelvin sense contact for the gate driver. For the TO-package, L_E in Fig. 9 is nonexistent, but there is a large L_{CS}. Hence, this measurement error produced by L_{CS} for a 3-pin TO-package becomes more pronounced compared to the used module offering a separate Kelvin sense connection.
Furthermore, the so-called self turn-on effect [11] can lead to a transient increase of V_{GE} additionally for both package concepts.
In the measurements shown in Fig. 8, V_{GE} exceeds the second reference V_{Ref2} before t_{th}, which normally would lead to a stopping of the charging process of C_2 and the end of the rise of V_2 accordingly, resulting in the output of a failure signal V_{Fault}. Since the ohmic voltage divider consisting of the two resistors R_{div}, dimensioned with each 2.7 kΩ, is not frequency compensated, $V_{GE}/2$ monitored by the detection logic is delayed to the original course of V_{GE}. To ensure fast and precise monitoring of the gate voltage, which this detection approach is aiming at, such a delay is generally considered as a disadvantage regarding the accuracy, especially for fast transitions. However, in the stated example this lack of precision turns into an advantage as it offers a certain level of robustness against the described transient gate voltage overshoot, oscillations, and noise. This results in a correctly detected normal turn-on process for the case depicted by Fig. 8. Nevertheless, when decreasing R_{div} to 1 kΩ, the divider proves fast enough to be sensitive to the disturbance resulting in the output of a fault signal constituting a wrongly detected SC I turn on (false positive). Due to this issue, a precise and reliable operation of the detection circuit cannot be ensured and proven under all conditions when applying this detection method to a package missing a Kelvin sense emitter. Instead, the usage of a device with a Kelvin sense emitter is required and recommended.

VARIATION OF TURN-ON RESISTANCE AND SELF-ADAPTION

Apart from the fast detection speed, the proposed method´s capability to dynamically self-adapt should also be given. Specifically, a change of the V_{GE} slope without any readjustment via R_1 or R_2 in Fig. 1 or the reference voltages is highlighted. A change of the switching speed may occur due to a change of the gate turn-on resistor or the input capacitance. The functionality of this V_{GE}-based detection method under an expanded condition set and its claimed self-adaption feature under different V_{GE} slopes shall be investigated in this section. For this purpose an evaluation under a variation of the $R_{g,on}$-values is performed.

Functional capability under a variation of $R_{g,on}$

As the differences of the gate voltage courses get smaller with an increase in switching speed, distinguishing between normal and failure turn-on processes is considered to be more critical for low $R_{g,on}$-values.

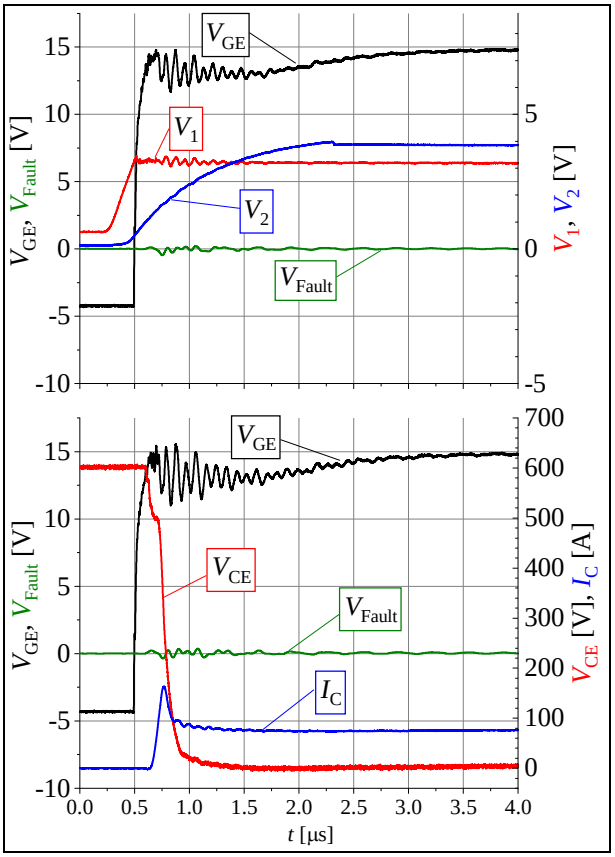

Fig. 10: Courses of detection circuit V_1, V_2 (top), load circuit V_{CE}, I_C (bottom), V_{GE}, V_{Fault} during normal turn-on process. V_{Bat} = 600 V, I_C = 75 A, $R_{g,on}$ = 1.7 Ω, L_{Load} = 500 µH, L_{par} = 70 nH; EconoPACK-module.

According to the aforementioned results shown in Fig. 6 and Fig. 7, where a datasheet-$R_{g,on}$ of 6.4 Ω is used, measurements with an $R_{g,on}$ of 1.7 Ω and 3.5 Ω, respectively have been carried out. For both values, the separation of normal and failure cases is working reliably.

Fig. 10 and Fig. 11 show the measurement results for $R_{g,on}$ = 1,7 Ω representatively.

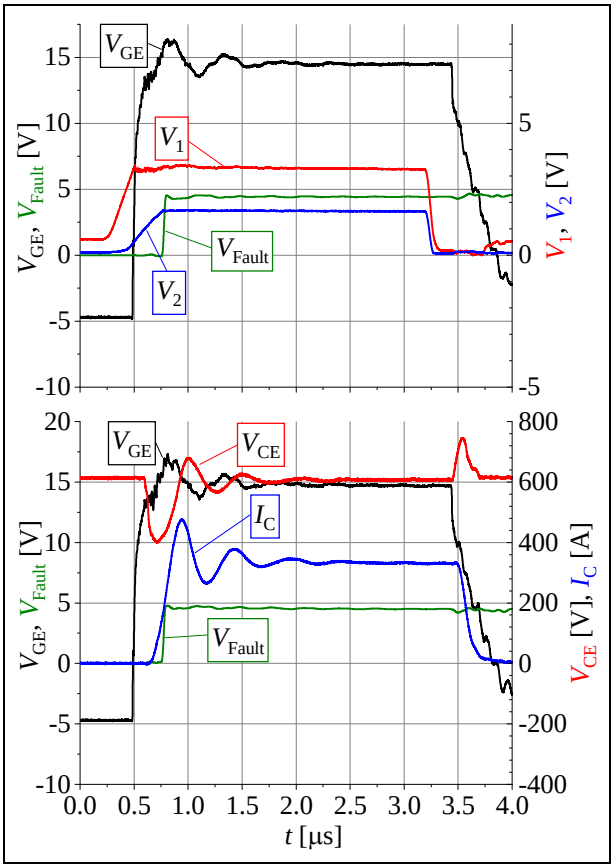

Fig. 11: Courses of V_1, V_2 of the detection circuit (top), V_{CE}, I_C of the load circuit (bottom) and V_{GE}, V_{Fault} during SC I. V_{Bat} = 600 V, I_C = 75 A, $R_{g,on}$ = 1.7 Ω, L_{Load} = 500 µH, L_{par} = 70 nH; EconoPACK-module.

Investigation on self-adaptive behavior

Conventional gate voltage-based SC I detections rely on attaining one reference voltage level within a certain time to detect a potential short. A big advantage of the proposed detection method is claimed to be the utilization of two reference voltages [5]. In theory, this allows the detection circuitry to dynamically self-adapt to different V_{GE} slopes, as the time t_{th} will automatically shift to certain values when t_1 is changed due to flatter or steeper V_{GE} slopes.

For a conventional gate voltage-based SC I detection the top of Fig. 12 depicts the V_{GE}-courses of normal and failure turn-on processes for a variety of V_{GE} slopes schematically. t_{th} is fixed to a constant value, represented by the constant V_1. V_2 is, similarly to the method discussed in this paper, used to assess the turn-on speed and to distinguish between a normal and a failure turn-on (see Fig. 12 bottom). As a result, the conventional approach would classify both a fast normal turn-on (Fig. 12: steep slope, normal), as well as a slow failure turn-on (Fig. 12: flat slope, SC I) incorrectly. Only the case for medium slopes is assessed correctly, as t_{th} fits to the proper separation of normal and SC I turn on.

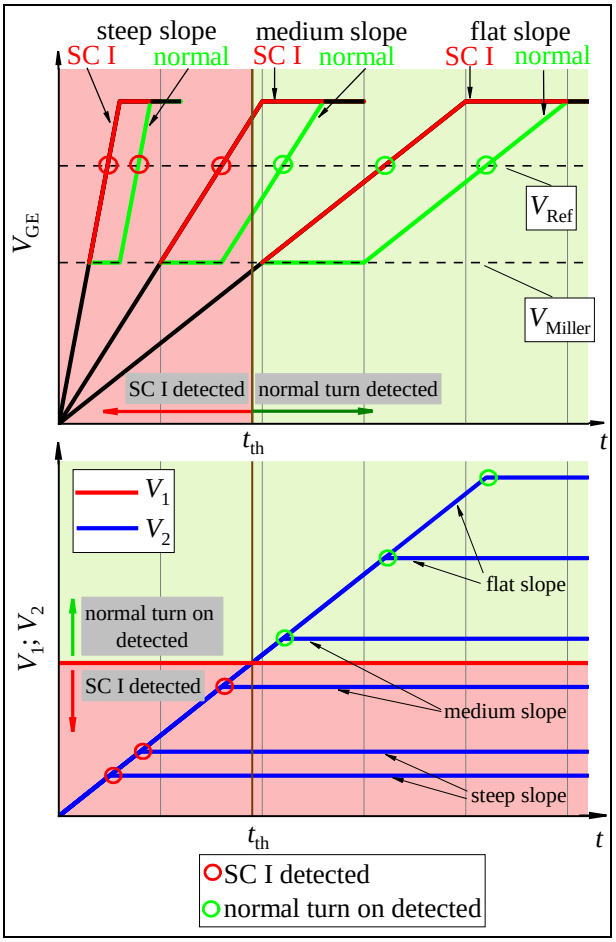

Fig. 12: Simplified schematic courses of V_{GE} for three different slopes under normal and low inductive SC I turn-on conditions for conventional gate voltage based method (top). Courses of the detection circuitry with only one voltage reference (V_{Ref}, top, represented by V_1, bottom). To provide comparability with the approach presented in this paper, V_1 is set to a constant value, representing the fixed threshold time t_{th} (see also [5]).

In contrast, the proposed principle relying on two voltage reference levels should categorize all switching events correctly. This can be achieved because t_{th} is correlated to the variable value of t_1. Therefore, t_1, describing the time within which V_{Ref1} is attained, acts as a determining factor and is used to adjust t_{th} and set it to a certain value according to the switching speed being present in the interval for $V_{GE} < V_{Ref1}$. Given this mechanism, also schematically depicted in Fig. 13 for the steep and flat slope case, a self-adaption to different switching speeds shall be enabled without the necessity to readjust the circuitry. The appropriate schematic courses of V_1 and V_2 are drawn in the lower part of Fig. 13.

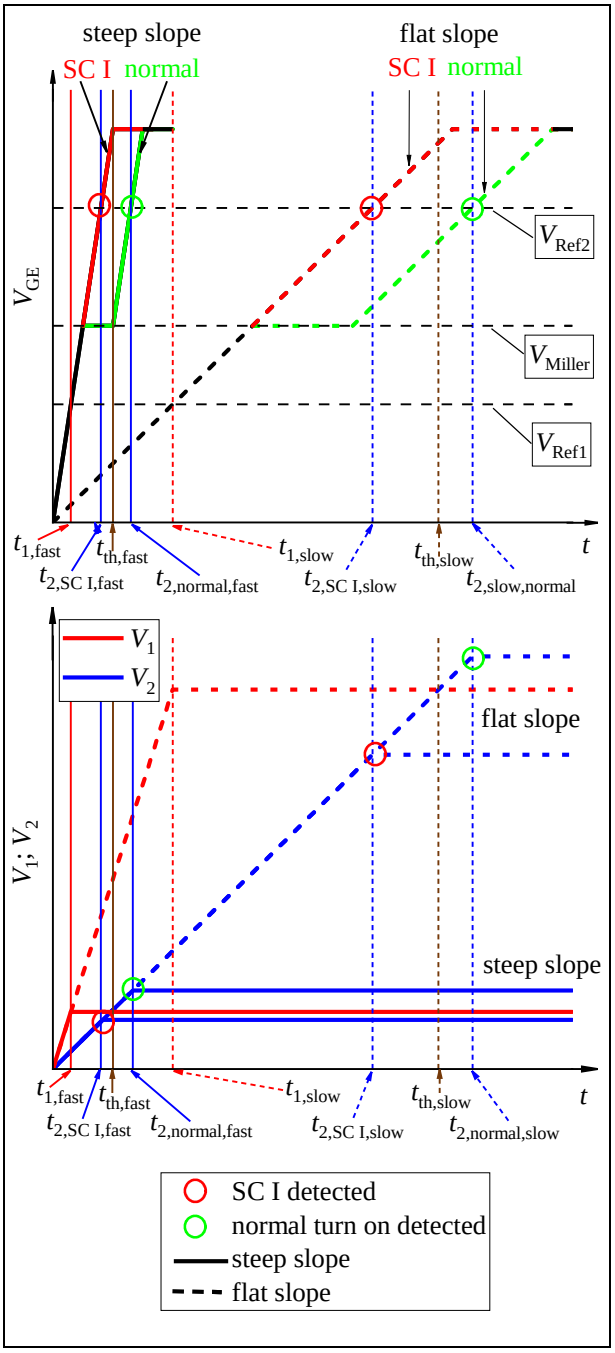

Fig. 13: Simplified schematic courses of V_{GE} for the steep and flat slope cases of Fig. 12 under normal turn-on and SC I conditions (top). Courses of the proposed detection circuitry using two voltage reference levels (bottom). t_{th} is set dynamically according to t_1, which adapts to the slope of V_{GE} (see also [5]).

Regarding the measurements shown in this paper for the EconoPACK-housing, the correct classification of the switching events for different $R_{g,on}$-values between 1.7 Ω and 6.4 Ω, shown in Fig. 6, Fig. 7, Fig. 10 and Fig. 11, could be obtained without a readjustment of the detection circuitry. Nevertheless, this achievement does not rely on dynamic self-adapting behavior. Fig. 14 displays the comparison of the V_{GE}-courses for the fastest normal turn-on at $R_{g,on}$ = 1.7 Ω and the slowest SC I turn-on at $R_{g,on}$ = 6.4 Ω.

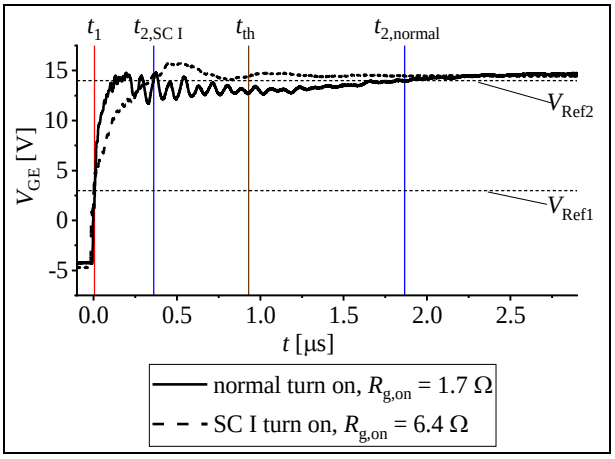

Fig. 14: V_{GE} for the fastest normal turn on at $R_{g,on}$ = 1.7 Ω and the slowest SC I turn on at $R_{g,on}$ = 6.4 Ω.

The slight exceedance of V_{Ref2} at the beginning of the Miller-phase is not taken into consideration by the detection circuitry because of the already explained smoothing behavior of the ohmic voltage divider. Despite the smaller $R_{g,on}$ = 1.7 Ω, the normal turn-on process is still slower than the SC I turn on at higher $R_{g,on}$ (6.4 Ω) regarding the surpassing of the second reference V_{Ref2}. The correct categorization of both the cases shown in Fig. 14 without any readjustment is based on this fact instead of a dynamic self-adaption.

In contrast to the theoretic considerations of Fig. 12 (top) and Fig. 13 (top), the crossing of the first reference V_{Ref1} does not change significantly with a variation of $R_{g,on}$ within a certain range. As a result, a dynamic self-adaption would not happen in this case. The weak dependence of t_1 on $R_{g,on}$ is also due to the relatively high internal gate resistance $R_{g,int}$ = 8.5 Ω present in the DUT, which attenuates changes of the external gate resistance.

The self-adaptive behavior can only be proven, when the SC I turn-on is slower than the normal turn-on across the entire V_{GE}-course (see Fig. 13). In this case, a conventional gate voltage-based detection method would fail (see Fig. 12). Furthermore, a self-adaption could potentially only take place if the surpassing of V_{Ref1} occurred at considerably different times t_1 for both cases so that an adjustment of t_{th} could take place.

CONCLUSION

A discrete gate voltage-based SC I detection introduced in [5] has been presented and tested. The results show that the proposed method can detect a low inductive SC type I failure in a very fast and reliable way. The failure will be detected when V_{GE} attains the second voltage reference level. For the used 75 A EconoPACK-module, the SC I was detected 270 ns and 300 ns after turn-on for external gate turn-on resistances of 1.7 Ω and 6.4 Ω, respectively. Subsequently, for different gate resistors and input capacitances, the detection speed varies.

Furthermore, the reliability of the method highly depends on the package form of the DUT.

The reliability and functionality are applied for a package offering a sense emitter contact with a low L_{CS} design. The packages, which are not provided with a Kelvin sense, such as 3-pin TO-247 devices, as tested in this paper, are not recommended. Special attention should be paid to an operation at high load currents or turn-on transitions with low gate turn-on resistances since the voltage level of the Miller plateau depends on the level of load current and IRRM. This aspect can affect the detection method´s functionality when an overload current or a high IRRM is observed.
The expected self-adaptation of the detection for a varied V_{GE} slope highly depends on the DUT´s chip design, such as internal gate resistance and input capacitance C_{iss} (current rating).
However, the detection method demonstrated in this paper appears to be suitable also for bigger modules such as IHM (IGBT High Power Module), since the internal gate resistance is usually small and the common-source inductance L_{CS} is significantly optimized. Moreover, the high $C_{iss,}$ due to a large number of chips in parallel, enables a wide detection time window for the varied V_{GE} slope. Finally, in comparison to the conventional V_{CE}-monitoring, the gate driver board is not exposed to high voltage, which provides more safety for the control unit and the driver itself.

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Development of an HBM-ESD tester for power semiconductor devices

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Abstract

Recently, the human body model - electrostatic discharge (HBM-ESD) test capability for power diodes was introduced among the requirements in the field of automotive include for a superior reliability. During the HBM-ESD test, the DUT works in avalanche conditions and it is still not well understood the failure modality occurring in power diodes. The available commercial HBM-ESD testers only give information about the maximum voltage rate, without any specific measurement of electrical waveforms. In this work we present a HBM - ESD tester for the characterization of power semiconductor devices up to 6 kV. In the proposed tester both the voltage and current DUT waveforms are measured, for a further gain of the failure analysis in power diodes.

Keywords: Human-Body-Model Electrostatic Discharge (HBM-ESD), Avalanche Breakdown, Power Diode

INTRODUCTION

The power semiconductor devices market is demanding for power semiconductor devices with a superior reliability in out of safe operating area (SOA), with a specific emphasis on the avalanche capability. Usually, the avalanche capability of a power diode is measured through the unclamped inductive switch (UIS) test [1], that is the maximum energy that the DUT can stand in avalanche conditions (A sketch of the UIS test schematic is reported in Fig. 1a). However, the last requirements in the field of automotive concern about the reliability in terms of HBM-ESD [2] (A sketch of the UIS test schematic is reported in Fig. 1b). This model approximates the electrostatic discharge that may occur when a person handles a device. Typically, the HBMESD event is not considered detrimental for power diodes. However, recent studies highlight as power diodes may fail under electrostatic discharge [2], unexpectedly. The HBM-ESD capability concerns the reliability in handling procedures for mounting discrete power diodes is automotive applications, such as DC-DC converters or inverters. As for UIS, the HBM-ESD test forces the DUT to operate in avalanche conditions. Since the HBM-ESD test energy is at least one order of magnitude lower than the one of the UIS test, different current density dynamics are expected to occur during the test. Numerical results in highlight as the higher di/dt occurring during the HBM-ESD test leads to the occurrence of failures different from that of UIS. As reported in [2], unexpected effects as current filamentation may occur during the ESD test, leading to premature failure. Typically, the current filamentation leads to a strong variation of the Cathode voltage. Therefore, the measurement of the current and voltage

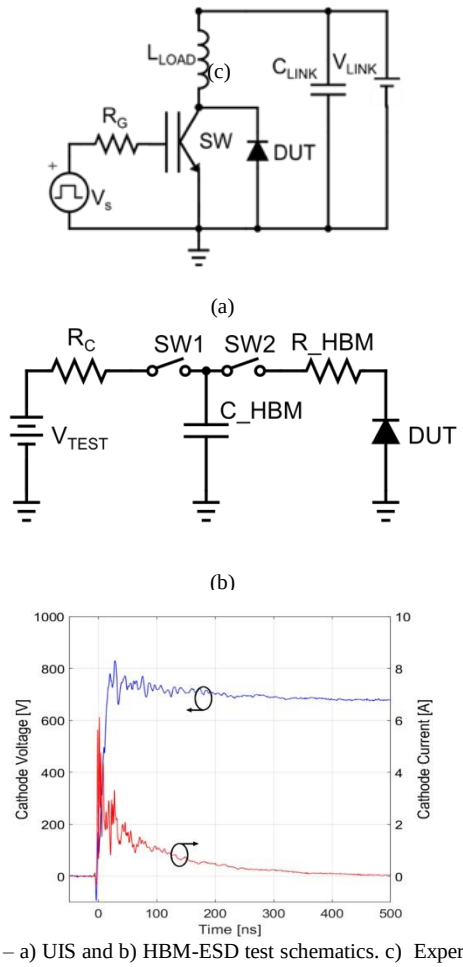

Figure 1 – a) UIS and b) HBM-ESD test schematics. c) Experimental device [4] HBM-ESD test waveforms.

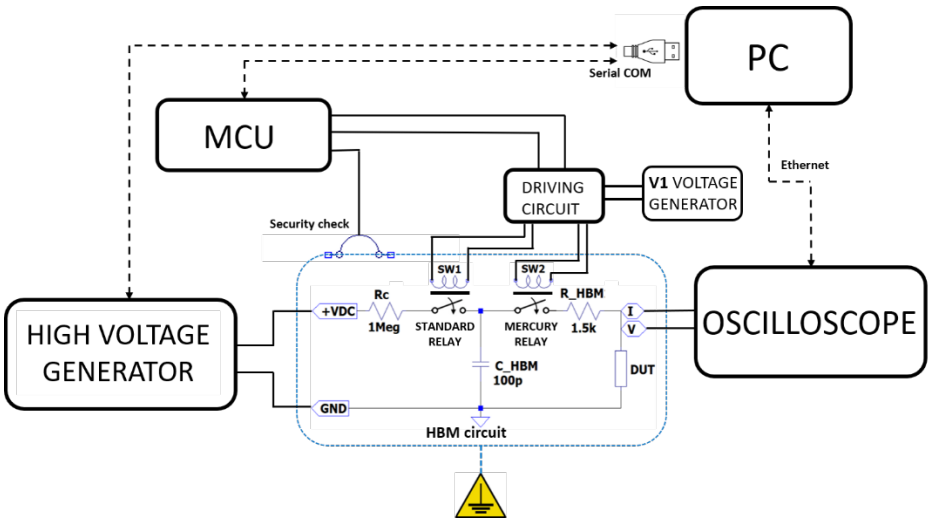

Figure 2 – A sketch of the developed HB-ESD tester.

waveforms at the DUT terminals during the ESD test gives further elements for the investigation of failure, supported by TCAD simulations. The main disadvantage of the commercial ESD tester is the impossibility to measure the current and voltage waveforms occurring at the terminals of the DUT during the test. Results in [2] show as the cathode voltage waveform during the HB-ESD test gives important information about the current distribution over the time. In this work we present an HBM-ESD tester capable to measure the electrical waveforms, with a consequent gain in the comprehension of the failure events. Therefore, in a first section the experimental setup in presented. In a second section some experimental data are reported and commented.

THE DEVELOPED HBM-ESD TESTER

The reference standard for the HBM - ESD tester is reported in [3] and in Fig. 1b the circuit of principle is reported. C_HBM=100 pF, R_HBM = 1.5 kΩ and R_C = 1 MegΩ. Basically, the C_HBM capacitance in a first step is charged at the V_{TEST} voltage through SW1 that is a short circuit. In this phase SW2 is an open. When the voltage drop at the C_HBM terminals achieves the target value, SW1 becomes open and after a suitable delay time SW2 turns to the short-circuit condition. At this point, since the DUT voltage is zero, a current equal to V_{TEST}/R_HBM flows into the DUT and forces it into the avalanche condition. Therefore, once the DUT voltage achieves the breakdown voltage (BV) the voltage clamps and the current exponentially drops with a time constant equal to $\tau = R\_HBM \cdot (C\_HBM + C_{DUT})$, where C_{DUT} is the DUT capacitance. This time constant is the main difference between the UIS and the HBM-ESD tests. For the former test the current falls down with a slope equal to $di/dt = -(BV - V_{LINK})/L_{LOAD}$ and typically it is at least one order of magnitude higher than that of a HBM-ESD test. As an example, the HBM-ESD waveforms of device [4] are reported in Fig. 1c. However, the implementation of the setup involves the design of the different parts that compose the test, as sketched in Fig. 2. The most critical component of the tester is SW2, a

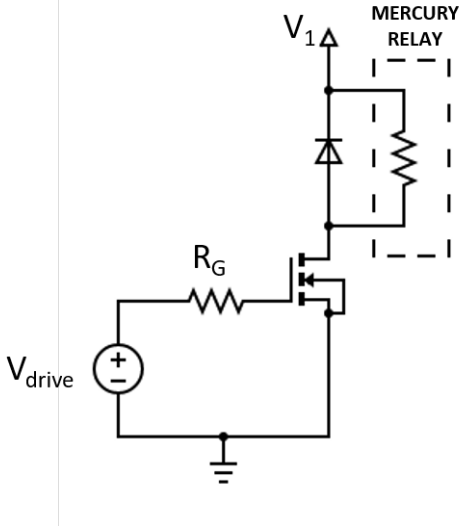

Figure 3 – The Relays driving circuit schematic.

relay that uses mercury as a switching technology. This is mandatory to achieve the requirements of the [3] standard. The SW2 switch must become instantaneously a short circuit to replicate the exact testing conditions. Moreover, a V_{TEST} up to 7kV is applicable to the terminals of both SW1 and SW2. This is not compatible with most of the semiconductor or vacuum tubes switches. A standard relay is not usable, since it exhibits contact bounces that interrupt the C_HBM discharge and this is not suitable for an HBM-ESD tester. In Fig. 3 the driving circuit of both the switches SW1 and SW2 is reported. Basically, the relay coil is the load of a power MOSFET in common emitter configuration. V_{drive} in Fig. 3 comes from the driver IC MCP1404, supplied at 15 V by the voltage generator V1, that has as the input a digital output of the STM32F401RE Nucleo-64 board. The same board checks that the circuit box is closed, to assure a safety measurement. If it is open, the MCU does allow to run the test. Finally, through a Matlab© graphical user interface the PC in connected to the high voltage generator, the oscilloscope and the STM32F401RE Nucleo-64 board. A multi-purpose sock is used to

quickly connect up to three terminals power devices (TO220 like), as well as two general purpose terminals. The current flowing through the DUT is measured by a current transformer.
Finally, the high voltage supply is given by the SRS PS375 generator [5], that has a maximum voltage capability of 20kV. The limitation to 7 kV is related to the maximum measurable voltage of the voltage probe of the oscilloscope.

RESULTS AND COMMENTS

Different families of devices were tested to validate the setup and to evaluate their HB-ESD capability. Recalling results in Fig. 1c, the voltage and current waveform is reported for the commercial device [4] for V_{TEST} = 3.2 kV. When the SW2 gets close, the current suddenly achieves its peak and after 20 ns the cathode voltage achieves the breakdown voltage (BV) of the device, that is in the order of 700V. Some cathode voltage oscillations are visible, but their variation lays in the range of 50 V. These oscillations are mainly related to the parasitic elements of the circuit. Therefore, the setup board design was carried out with very low parasitic capacitance and inductance. However, the DUT itself may be the origin of the oscillations and their evolution may give information about the current distribution into DUT, as reported in [2]. In Fig. 4 the electrical waveforms are reported for the device [6] with V_{TEST} = 3 kV. As for the previous device, after 20 ns the cathode voltage achieves a BV voltage in the range of 1000 V, even if the voltage rate of the device is 650 V. Moreover, when the cathode current becomes negligible, the cathode voltage rises up to 1200V. At the same time the cathode current exponentially goes down. Differently from data reported in Fig. 1c, the voltage oscillations have a lower and irregular frequency. This a complex behavior and it is a typical experimental evidence that highlights the presence of a strong current filamentation in the device [2], [7]. The current filamentation is due to the presence of a negative differential resistance (NDR) in the reverse I-V curve of the DUT and it becomes more relevant when the conduction carriers concentration becomes comparable to the doping concentration of the Drift layer [8]. The more the oscillations are large, the more the current density is higher into the filaments, with the consequent voltage variation. In these conditions the high instability of the impact ionization phenomenon becomes dominant and the current crowding becomes the stable condition. When the current filamentation occurs, the cathode voltage drops down to a voltage that is typically up to 200 V lower than the BV at low current levels. However, as soon as the total current flowing in the device achieves a value where the I-V blocking curve has a positive differential resistance, the current spreads and becomes constant over the area of the device. When this occurs, the cathode voltage goes back to the BV voltage for low current densities, that is typically higher. This kind of dynamic occurs if the current filamentation does not leads to a premature destruction of the device.

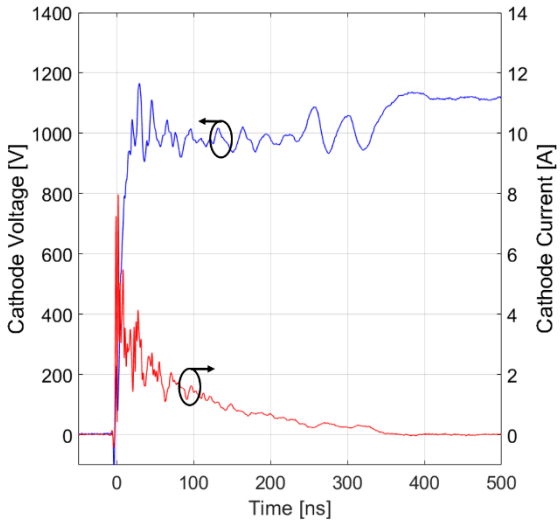

Figure 4 – Experimental device [6] HBM-ESD test waveforms.

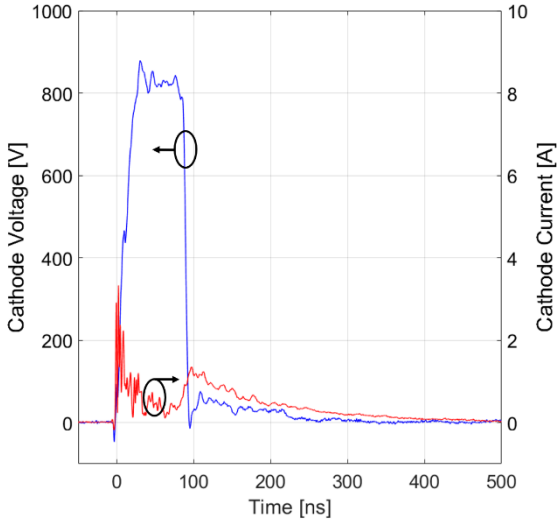

Figure 5 – Experimental device [9] HBM-ESD test waveforms.

As an example, in Fig. 5 the electrical waveforms are reported for device [9] that fails for V_{TEST}=1.5kV. Standard HB-ESD testers only give the maximum test voltage, while the developed tester allows an accurate characterization of the device even when it fails.

CONCLUSION

In this work, the development and validation of a custom HBM-ESD tester has been presented, for a test voltage up to 7 kV. The main advantage of the developed setup in the possibility to measure the electrical waveforms during the test, giving a further insight into the investigation of the failures. Some measurements are presented to show the capability of the setup.

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Measuring Transient *I*/*V* Turn-On Behavior of a Power MOSFET without a Current Sensor

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Abstract

Double pulse test (DPT) is usually used to characterize and verify turn-on/turn-off operation of power switches. Yet, new high frequency switching devices based on SiC and GaN technologies require much more elaborate DPT circuitry and sensing nodes compared to the established Si devices. Especially, suitable current sensors are challenging to realize and always limit the bandwidth.
We propose a Transmission Line Pulsing (TLP)-based technique, which we call sensor gap TLP (sgTLP) and which is capable to monitor the transient currents and voltages during the turn-on sequence of a power MOSFET, without the need of a current sensor. The proposed sgTLP approach is compared to established TLP methods in two applications: the passive switching of a fast transient voltage suppression diode and the active switching of a Si power MOSFET. The novel sgTLP shows the same or better characteristics than both of the standard methods, but needs only one measurement, where standard TLP would need two separate methods. Especially, sgTLP detected rise times of 54 ps of a current and 52 ps of a voltage signal using a pulse duration of 100 ns. The measured characteristics of the MOSFET turnon reveals several inductive and capacitive coupling mechanisms that are not analyzable by the established TLP methods but become visible applying sgTLP.

Keywords: Device characterization, Time-Domain Analysis, Power MOSFET, Transmission Line, Pulsing, sensor gap TLP (sgTLP)

I. INTRODUCTION

Electronic switches based on gallium-nitride (GaN) and silicon-carbide (SiC) materials are capable of turn-on times in the single digit nanosecond domain; some manufacturers even advertise devices with sub nanosecond rise times.[1] The circuit design and simulation with such fast devices relies on adequate large signal models [1]. Here, model validation or parameter extraction becomes increasingly challenging, as the simultaneous detection of the voltage (few volts and several hundreds of volts) and current (tenths and several tenths of amperes) waveforms at the terminals during the nanosecond switching process is hardly feasible. Therefore, state of the art characterization includes different kinds of measurement setups for different sets of parameters. Ranging from pulsed techniques [2] to frequency-based methods [3-5] every technique needs different setups and operational requirements.
The gold standard method that comes closest to the conditions the switches are exposed to in the field is the double pulse test (DPT). Here, the terminal quantities are monitored during the dynamic turn-on/ turn-off cycle. Yet, the DPT cycle is not only dependent on the device under test (DUT), but also on the DPT circuitry the DUT is embedded into and the type and position of the sensing nodes. Especially the current sensors have the most intricate realization requirements for characterization of SiC and GaN devices: high bandwidth, very low loading effect and high current ratings.
To reduce the number of different setups and to overcome the DPT restrictions we introduce first steps towards a characterizing technique that does not rely on a current sensor limiting the performance w.r.t. the above-mentioned aspects.
The presented transmission line pulsing (TLP) [6]-based setup can characterize the turning on sequence of a power MOSFET, while maintaining the exact synchronization of the acquired voltage and current waveforms at both transistor ports simultaneously.
Section II describes the novel approach and contextualize it into several established TLP techniques. Key aspects are validated using a fast transient voltage suppression (TVS) diode.
The turn-on transients of a silicon (Si) power MOSFET extracted with the proposed approach are described in Section III. A comparison with a similar technique utilizing a dedicated current sensor shows good correlation. Lastly, Section IV summarizes the results.

[1] i.e., IMW120R350M1H Infineon Technologies

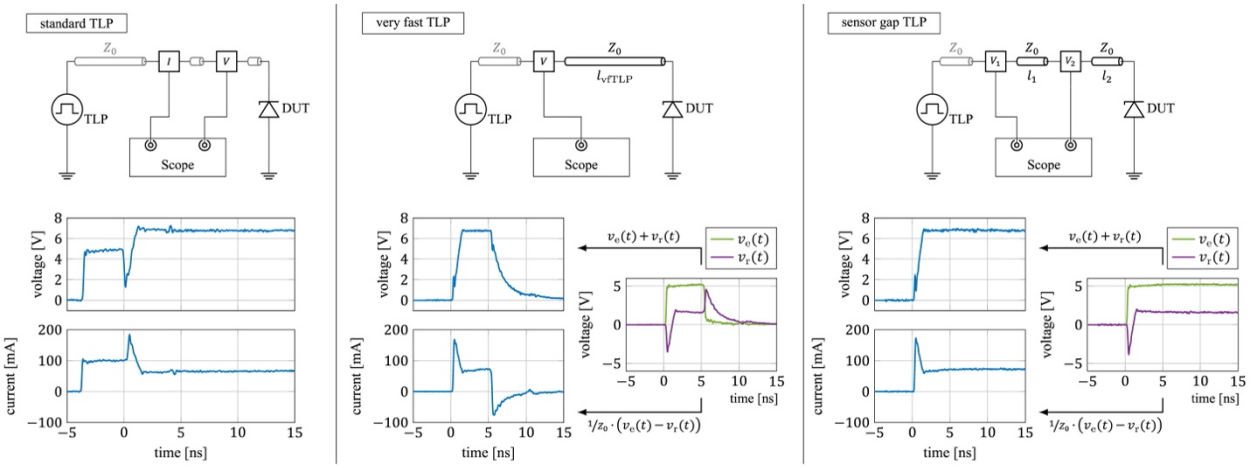

Figure 1: Three different TLP setups with the same TVS diode as DUT[2]: standard TLP, very fast TLP and sensor gap TLP. Each of the three sub-images illustrates the setup and the resulting current and voltage waveforms. Additionally, for very fast TLP and sensor gap TLP the acquired and synchronized excitation $v_e(t)$, the DUT response $v_r(t)$ and the mathematical operations to compute the current and the voltage are depicted.

II. TRANSMISSION LINE PULSING

Many different forms of the TLP method evolved out of the initial method introduced by Maloney and Khurana in 1965 [7], which was the first description of a TLP method to characterize semiconductor devices in the fast ESD regime. This evolution was driven by requirements of signal resolution and new application fields [8]. Even so, all of them have a common feature: the pulse generator (or pulser) and waveguide (cable) with a constant impedance Z_0 connecting the pulser to the DUT.
The pulser produces a very replicable short, constant voltage pulse $v_e(t)$ with a fast-rising edge, which then travels along the cable to the DUT. There, in response to this excitation, the DUT generates a transient voltage waveform $v_r(t)$, which in turn travels into the opposite direction along the cable. According to the transmission line theory the superposition of the excitation and the response at the terminals yields the current and waveforms at the DUT.
The process of sensing the signals present in the system distinguishes the different TLP methods. For the analysis in this paper, the following three are important: standard TLP, very fast TLP and sensor gap TLP.
To illustrate the relevance and limitations of each method to the topic of transistor characterization, the applicable measurements setups and the prevalent signal waveforms are depicted in figure 1. A fast TVS diode as DUT[2] shows pivotal effects: turn-on time in single nanosecond range with subsequent clamping of the voltage.

Standard TLP

The method in figure 1a is referred to as "standard" TLP or TLP (with any epithet) and is very similar to its primal origin. Here, current and voltage sensors are located near the DUT.
To understand the structure of the resulting standard TLP waveforms the following details must be considered:

(1.) The sensors are placed as close as possible to the terminals of the DUT. Even so, there are unavoidable cable pieces between the sensors themselves and between the last sensor and the DUT. Deliberately, these must be as short as possible. Additionally, as the excitation $v_e(t)$ and the DUT response $v_r(t)$ are travelling in opposite directions, small misalignments result at the measuring points of the sensors.
(2.) Both sensors generate a voltage signal proportional to the current or voltage present at their location. However, they utilize different measurement principles (current: transformer principle, voltage: resistive pickoff). This implies different transient responses, especially at the beginning of the sensor waveforms.

Moving from left (-5 ns) to right (15 ns) in figure 1a, the standard TLP voltage and current waveforms can be explained as follows:
The first part (-5 to 0 ns) of the signals is just the incoming excitation $v_e(t)$ from the pulse generator, which is a constant voltage pulse with a fast-rising edge. Both voltage and current signals are not aligned (see explanation given in (1.) above) and there is no proper way to align them, as the $v_e(t)$ and $v_r(t)$ are travelling in opposite directions. In addition, the transient responses of the sensors are clearly different at the onset of the plateaus, which is due to remark (2.).
From 0 ns onward the actual signal from the TVS DUT establishes. The voltage sensor registers a sudden drop followed by a rising edge with a small overshoot until the voltage settles to the clamping value of around 7 volts with an additional small voltage ringing in the plateau at

[2] TVS Diode: „ESD5V3S1U-02LRH" Infineon Technologies

about 4 ns (which will turn out to be an artefact). The current waveform shows a peak around 0 ns (during the voltage rise) with a drop to approx. 65 mA afterwards and a similar ringing at about 4 ns.
The TVS DUT turns on during the first nanosecond (0 to 1 ns). At that time, the voltage and current are determined by the charging process intrinsic capacitance of the diode until it switches to the conduction mode, where current and voltage are set by its DC characteristic.
The sensor signals do not represent this reactive turn-on behavior properly, as the misalignments (1.) and unequal sensor specific influences (2.) do disturb the first 10 ns in this measurement setup. Therefore, in standard TLP the data is usually extracted only after some nanoseconds, i.e. in the non-reactive part at the end of the pulse. Thus, the waveforms deduced by the standard TLP resemble the quasi-static DUT characteristics without second order effects like i.e., self-heating.

Very Fast TLP

If more information about the reactive DUT behavior at the beginning of the excitation is needed, the temporal resolution can be increased using very fast TLP (vfTLP). The core idea driving this method is that as soon as the exact waveforms of the excitation $v_\mathrm{e}(t)$ and the DUT response $v_\mathrm{r}(t)$ are known, both current and voltage transients can be calculated by superimposing the signals. Therefore, the main goal is to extract the excitation signal $v_\mathrm{e}(t)$ and response $v_\mathrm{r}(t)$ of the DUT separately.
To do so, vfTLP uses only one voltage sensor and a long cable between the sensor and the DUT. The cable length l_vfTLP is chosen long enough to ensure that $v_\mathrm{e}(t)$ and $v_\mathrm{r}(t)$ do not overlap at the location of the sensor. Since the current information is redundant in this setup and current sensors usually tend to have lower bandwidth ratings, the current sensor is omitted.
The figure 1b shows the vfTLP setup with the resulting voltage and current waveforms at the DUT for the same TVS diode[2] as before. Also shown are the synchronized waveforms of the excitation $v_\mathrm{e}(t)$ and the DUT response $v_\mathrm{r}(t)$, from which the voltage and the current are calculated.
Using vfTLP, the turn-on process of the TVS diode is determinable in more detail: a capacitive signal at the beginning is followed by the clamping behavior. The current rise time is determined as 145 ps, corresponding to the TLP pulse onset. Additionally, the resolution is sufficient to unveil a small inductive voltage peak during the rising current edge due to the conductors to the DUT. Moreover, the small voltage overshoot and the ringing in the plateaus (see at 2 ns and 4 ns in standard TLP waveforms) is not present.
The principal limitations of vfTLP are the cable length (l_vfTLP) between the sensor and the DUT needed to separate $v_\mathrm{e}(t)$ and $v_\mathrm{r}(t)$, which depends on the pulse duration. With common cable delays of about 4 ns/m, several meters of cable are needed for pulses longer than about 10 ns. Since long cables distort high bandwidth signals, state of the art vfTLP methods produces useful results only with pulse durations in the range of a single digit nanosecond regime.

Sensor Gap TLP

The sensor gap TLP method (sgTLP) was developed to overcome the pulse duration restriction of vfTLP, while keeping its high temporal resolution. As depicted in figure 1c, sgTLP uses two voltage sensors, separated by a well-known cable with a length of less than a meter. The cable connecting the DUT can be even shorter, so that the total cable length corresponds to delays of about 5 ns, but the method allows considerably longer pulse widths (e.g. 100 ns and more).
A sophisticated algorithm [10] combines both voltage signals to separate the excitation $v_\mathrm{e}(t)$ from the DUT response $v_\mathrm{r}(t)$, even if they overlap at the locations of the sensors. Thus, with the sgTLP method, useful pulse durations are independent of the cable lengths. The basic algorithm is described in the appendix.
The graphs below the sgTLP setup in figure 1c show the extracted pulses of the excitation $v_\mathrm{e}(t)$ and the DUT answer $v_\mathrm{r}(t)$, as well as the resulting current and voltage transients.
The voltage and currents are almost identical to the vfTLP waveforms during the duration of the vfTLP pulse, showing the quality of the sgTLP algorithm. The current rise time amounts to 153 ps, corresponding to the vfTLP value within less than one sampling period (12.5 ps) and again representing the pulse onset. Moreover, like in vfTLP, the ringing observed in standard TLP data is not present and the inductive voltage peak is visible in sgTLP, too.
But while the vfTLP pulse ends after 5 ns, much longer pulses can be used in the novel sgTLP method. Figure 1c shows only the first 15 ns of a 100 ns pulse for clarity, longer transients are discussed below.
As the sgTLP method does not rely on a bandwidth limiting current probe and employs shorter cables, the overall bandwidth of the setup can be higher in comparison to both standard TLP and vfTLP.

In conclusion, this study shows that sgTLP is superior to both standard TLP and vfTLP, as it combines the advantages of either world: very fast transients and long pulses. The sgTLP waveforms show the TVS' fast turn-on characteristics, also present in vfTLP, together with the quasi-static characteristics prevalent in the standard TLP data. The current rise times measured in this TVS experiment by vfTLP and sgTLP match within one sampling point and represent the excitation pulse rise time of 150 ps. In the standard TLP data, the rising edges are not accessible due to the described artefacts.
Nonetheless, the extraction algorithm for sgTLP with its required calibration increases the level of complexity.

III. USING TLP TO TURN-ON A POWER MOSFET

In a double pulse test (DPT) the initial condition of the DUT drain voltage is set in a predefined manner prior to

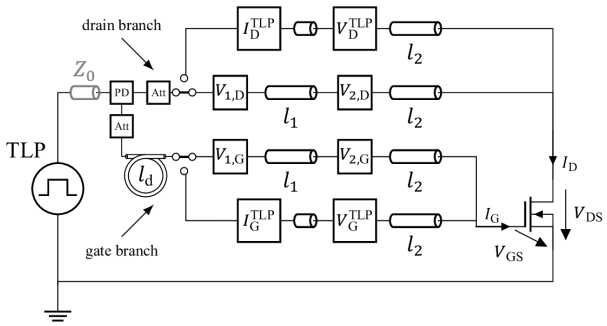

Figure 2: Measurement setup for the turn-on experiment with standard TLP and sgTLP methods.

starting of the turn-on sequence. How the device behaves during a fast ramp up for that condition is not accessible by measurement but can be very valuable for the characterization [9]. The TLP methods can be used to monitor both sequences: the settling of the drain voltage and the subsequent turning on of the device.
The following section describes the measurement setup for the turn-on of a Si power MOSFET[3] with standard TLP and sgTLP methods. This experiment inter alia directly compares the current waveforms acquired with a dedicated current sensor (standard TLP) and by the indirect current measurement (sgTLP).

Measurement Setup

As the desired turn-on sequences have durations of few nanoseconds, the following prerequisites are important:

A. Each transistor port needs a separate excitation with different amplitudes.
B. The excitation of the gate branch must be delayed with respect to the drain excitation, so there is enough time to set the drain voltage before the gate excitation initiates the turn-on process.

Figure 2 depicts the setup for the turn-on experiment with standard TLP and sgTLP setup separated by switches, so both experiments can be performed in succession. A TLP pulser system produces a single excitation with a high amplitude. This pulse is then split into two branches by a set of a power divider (PD) and attenuators (Att) to meet the first experiment prerequisite (see A.); the maximum voltages that can be acquired in the drain and gate branch are 200 V and 30 V, respectively. The attenuators have a second purpose besides setting of the amplitudes: without them there would be disruptive crosstalk between the drain and the gate branch.
In each branch there are two sensors; two voltage sensors for the sgTLP setup and a close-by current and voltage sensor combination for the standard TLP method.

[3] Si Power MOSFET: „IRFSL4127PbF" Infineon Technologies

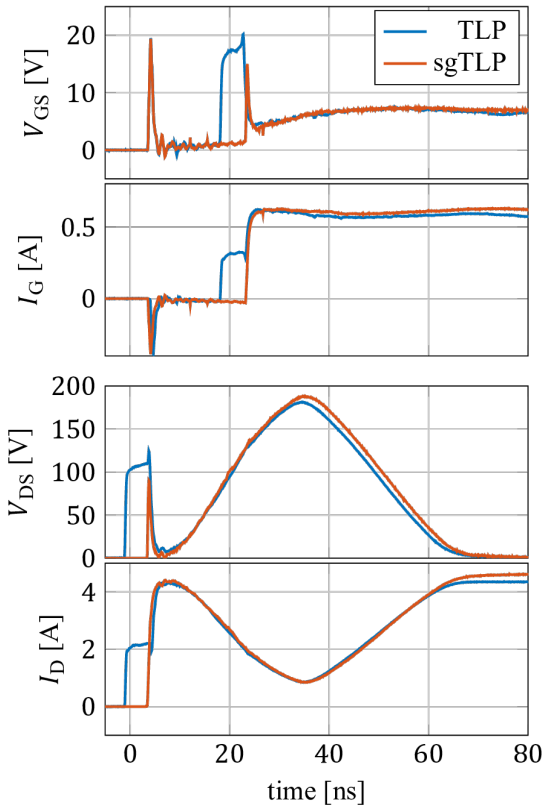

Figure 3: Transient current and voltage waveforms at the gate port (top) and the drain port (bottom) of a power MOSFET[3] during the turn-on experiment.

The second experiment prerequisite (see B.) is ensured by the additional delay line l_d in the gate branch that introduces a time difference of about 20 ns between the drain and gate excitations. Each port of the MOSFET is connected with RF needles (pitch of 0.5 mm and 40 GHz bandwidth) guaranteeing proper pulse polarities and grounding. The DUT packaged in a D²Pak is soldered onto a PCB with about 1.5 cm copper lines.

Experimental Results

Figure 3 illustrates the average (50 pulses) transient evolution of the terminal voltages and currents during the turn-on experiments for the standard TLP and sgTLP setups. For standard TLP, the incoming pulses again occur as artefacts in the drain and gate signals at about 0 ns and 20 ns, respectively. Those artefacts mask features that are clearly visible in the sgTLP data.
The pulse enters the drain path of the DUT at $t \approx 4$ ns, starting the charging of the output capacitance until $t \approx 38$ ns. Around that time, the delayed gate pulse (starting at $t \approx 23$ ns) has charged the gate to the threshold voltage and the transistors turns on during about 22 ns.
Taking a closer look, additional more or less subtle features are evident. Starting at $t = 0$ ns the sgTLP waveforms clearly show a voltage peak in V_{GS} and V_{DS} around

$t \approx 3$ ns. The cause of this peak is the rising current edge at the drain terminals up to 4 A in around 0.2 ns. Due to the inductance of the PCB lines and bonding wires in the drain path, the current rise is limited and an inductive voltage peak manifests in V_{DS}.
At the same time, the gate electrode exhibits a positive voltage and a negative current peak. As there is no incoming signal at the gate terminals, this gate waveform can be interpreted as magnetic coupling from the drain-source current loop to the gate-source loop.
From here onwards, the V_{DS} and I_{D} curves show the described capacitive charging behavior of the output capacitance towards about 200 V. Simultaneously, the gate electrode exhibits an increase in voltage due to the capacitive voltage divider between the miller capacitance and the gate source capacitance. Having a positive voltage at the gate terminal and no external excitation at the gate source port, a negative current flows into the Z_0 impedance cable.
At around 23 ns the gate excitation arrives at the gate port. An inductive voltage peak is evident that can be used to analyze the gate path inductance. As this voltage peak at the gate port subsides, the excitation of 30 V together with the $Z_0 = 50\ \Omega$ impedance of the cable acts as a constant 0.6 A current source for the gate. This current is charging the input capacitance until $t \approx 38$ ns, where the threshold voltage of around 5 V is reached and the turn-on sequence starts. Due to the relatively small gate current the V_{GS} remains at the miller plateau for another 20 ns while V_{DS} decreases and I_{D} rises to the values given by the transfer characteristics of the transistor.

Comparison of TLP and sgTLP Waveforms

As the V_{GS} curves in Figure 3 (top) show, the gate delay is slightly longer in the sgTLP setup. This leads to a delayed turn-on instant and, thus, to a higher maximum drain-source voltage. The difference in the gate branch delays is caused by laboratory restrictions for the cables and adaptors and is below one nanosecond.
Additionally, starting with the turn-on of the transistor, both gate and source currents become slightly higher in sgTLP than in standard TLP. A similar difference can be observed for the TVS diode described above (not shown), where the currents from sgTLP match those from vfTLP, but the standard TLP currents are slightly lower. Those discrepancies are still under investigation but seem to stem from the differences of the setups' components.
In summary, the waveforms produced by both methods match very well during the entire turn-on sequence. The inductive crosstalk to the gate loop is observable in both TLP signals, but the primary effects during the excitations' rising edges are masked in the standard TLP data, as the unavoidable distances in the setup generate artefacts just at exact this time.
For standard TLP, further attention must be paid when aligning currents and voltages in a signal path, because incoming and reflected pulses have different timings in the voltage and current sensor, respectively.

In contrast, sgTLP avoids those disadvantages by design, as the mentioned artefacts are not present in the sgTLP waveforms. Temporal resolution is increased and reveals additional information i.e., inductive and capacitive signals and crosstalk. Also, the synchronization of voltage and current in each path is more accurate, due to the manner the sgTLP waveforms are generated.
Utilizing the mentioned crosstalk, the very first peak of I_{G} and V_{GS} reveals the rise time characteristics of the respective sensor itself, undisturbed by the reflections in standard TLP. The rise times of the negative current peak are 75 ps for standard TLP and 54 ps for sgTLP, the rise time of the voltage peak is 52 ps for both methods.
The data clearly show the reduced bandwidth of the current probe in standard TLP. In sgTLP, however, the current detection rise time matches the value of the voltage measurement (in both setups) and reaches the scope limit of 50 ps, impressively showing the potential of the new method.

IV. SUMMARY

We proposed a novel Transmission Line Pulsing (TLP) based method, the so-called "sensor gap TLP" (sgTLP) that is able to monitor voltage and current transients, e.g. during the turn-on sequence of a power MOSFET, for sufficiently long times and with very high temporal resolution of 54 ps or less, for both voltage and current detection.
Instead of using a dedicated current sensor, two spatially separated voltage sensors are utilized to extract voltage and current transients at the terminals of the DUT.
Using a fast TVS diode as DUT, the proposed approach could be directly compared to established TLP methods and its very good performance could be shown for fast transients as well as for long pulses.
These findings could be further confirmed by analyzing the turn-on sequence of a Si power MOSEFT with sgTLP and a current-sensor-utilizing standard TLP setup. Applying two unequal and shifted excitations to the drain and gate terminals, the transient evolution of voltages and currents during the establishing biasing process and the subsequent turning on of the transistor could be recorded. Both approaches (with and without current probe) showed the expected general turn-on behavior. However, only sgTLP showed additional details that were masked in the current-sensor-based approach.
Thus, the noval "sensor gap TLP" (sgTLP) combines both the ability to apply "long" pulses of 100 ns or more and a very high temporal resolution of 54 ps or less. This is a promising approach, especially for the analysis of present-day fast power semiconductor devices or modules.

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APPENDIX: BASIC ALGORITHM FOR SGTLP

Figure A.1 (top) shows the measurement setup for sensor gap TLP (sgTLP) and the corresponding voltage waveforms of sensors V_1 and V_2. To illustrate the core idea of the separation algorithm clearer, the load is an inductance followed by a resistor with value of the systems characteristic impedance Z_0.
The sensor signals represent overlapping pulser excitation $v_e(t)$ and DUT answer $v_r(t)$, but the cables ensure different time shifts. The time shifts are determined as follows:

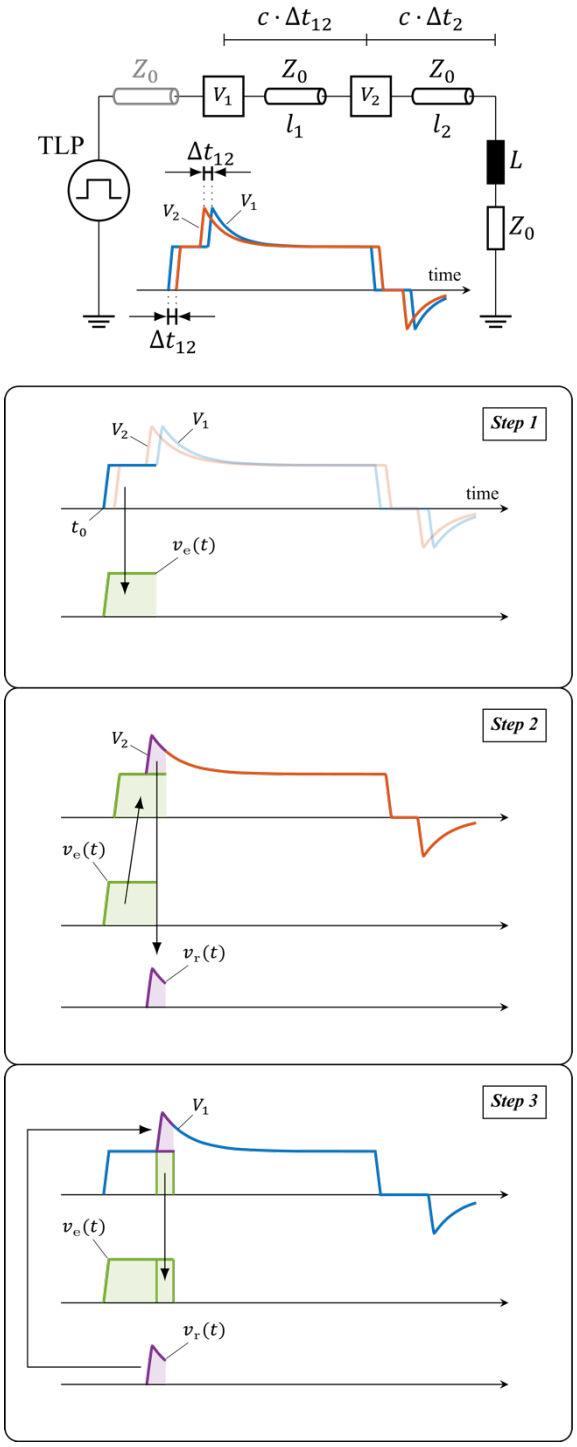

Figure A.1: Basic principle of sgTLP algorithm to separate $v_e(t)$ and $v_r(t)$.
Top: sgTLP setup with suitable DUT ($L + Z_0$) and the corresponding voltage waveforms of each voltage sensor V_1 and V_2.
Bottom: the first three steps of the sgTLP algorithm.

- The time delay between excitation $v_e(t)$ and DUT answer $v_r(t)$ of the sensors is
    - the double of time delay of cable 2 (l_2) for sensor V_2 and is denoted as $2 \cdot \Delta t_2$,
    - the double of combined time delay of cable 1 (l_1) and cable 2 (l_2) for sensor V_1 and is denoted as $2(\Delta t_{12} + \Delta t_2)$.
- The time shift between the sensor signals amounts to the single delay time of cable 1 (l_1) denoted as Δt_{12}.

This means that sensor V_1 "sees" $2 \cdot \Delta t_{12}$ more of the prevalent excitation $v_e(t)$ compared to sensor V_2 before the waveform is overlapped by the DUT answer $v_r(t)$. To understand how that additional information is useful to separate the overlapping signals, consider first three steps of the iterative algorithm [10], which are depicted in figure A.1.

Step 1: t_0 to $t_0 + 2(\Delta t_{12} + \Delta t_2)$ of sensor V_1's waveform is identified as the beginning of the excitation $v_e(t)$.

Step 2: This known beginning of $v_e(t)$ is first shifted by Δt_{12} to the right and then overlapped with the waveform of sensor V_2. Subtraction of both signals reveals the beginning of the DUT answer $v_r(t)$.

Step 3: The new part of $v_r(t)$ is shifted Δt_{12} to the right and overlapped with the waveform of the sensor V_1. Subsequent subtraction unveils an excitation waveform that is $2 \cdot \Delta t_{12}$ times longer than the waveform from step 1.

Steps 2 and 3 are then repeated until $v_e(t)$ and $v_r(t)$ are separated entirely. Having both separated waveforms, the current and voltage results from the usual vfTLP calculation (see figure 1).

New method for Si-wafer resistivity determination

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Abstract

Wafer resistivity is one of the most important parameters in production of Power Semiconductor Devices (PSD). This parameter is mainly responsible for achieving required breakdown voltage and other electric parameters. Proposal article describes principles and details of newly designed resonant method and new equipment according patent [1] and compares it with commonly known 4point method. This new method is based on resonant measurement of capacity and following calculation. New method exhibits comparable accuracy with 4point method and brings additional advantages.

Keywords: resistivity, pn junction, *C-V* curve, capacity, resonance.

INTRODUCTION

Silicon wafers are still used in production of PSD. Typical bulk resistivity varies from the order 10 Ωcm (e.g. welding diodes) up to 300 Ωcm (e.g. 7 kV rectifier diodes). Typical tolerance of commercially offered wafers is about 10 %. Better tolerance and sorting on demand (banding) is charged. Sometimes, suppliers don't want to do banding despite additional tax [2]. The 10 % wide band is too wide and unusable for some applications. Sometimes it is necessary to check the resistivity during or at the end of the production process when it is necessary to reveal the cause of the production defect (e.g. low blocking voltage achieved). For this purpose, a new method is useful that can examine the resistance on pn junction wafers. Such device can be already polarized by external voltage bias.

DESCTRIPTION OF RESONANT METHODE

Standard method of impedance measurement

Measurement of voltage dependence of capacity seems to be a trivial issue. Capacity can be measured by common RLC analyzer; voltage bias can be provided by laboratory high-voltage source with output current several hundred of μA. In real practice, this approach is not usable. The main limitation is the impossibility to provide reliable separation between RLC analyzer and high voltage circuit. Each fast transient effect in the high voltage part (e.g. spike) is itself transferred to the measuring circuit. In the worst case, the transient is transferred at full voltage level. Voltage breakdown or jump on measured sample will cause overvoltage on the input of RLC analyzer. When measurement is performed with bias voltage in the order of hundreds volts, this overvoltage will certainly damage the used RLC analyzer.
Further, noise generated by measured sample or high voltage source will cause measurement error and increase the uncertainty of measurement. Therefore, new resonant equipment for measuring capacity of biased pn junction with safe separation and reliable measurement has been developed.

Resonant method

The equipment described in document no. 305210 [1] as industrial design PV 2014-327 serves primary for the measurement of electric capacity of biased pn junction. This capacity is voltage dependent and mostly is decreasing with the square root of applied voltage. Basic principles of equipment are illustrated in the Fig. 1 bellow.

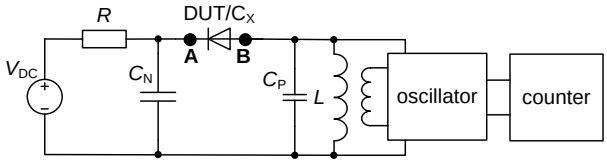

Figure 1: Principles of resonant measurement of capacity.

Measured pn junction (voltage dependent capacity C_X resp. DUT) is connected into resonant circuit which is made by the fixed capacity C_N (vacuum or ceramic capacitor) and by the inductance L. Inductance is represented as a parallel combination of ideal coil L and parasitic capacity C_P of winding. Such circuit has its own self resonance frequency given by well-known relation

$$f_r = \frac{1}{2\pi\sqrt{L\left(\frac{C_N\, C_X}{C_N + C_X} + C_P\right)}}. \quad (1)$$

The self-resonant frequency f_r depends mainly on the capacity of measured junction C_X. This capacity C_X can be significantly changed by connecting external voltage bias V_{DC} through coupling impedance R. The applied external DC voltage (bias) does not create any voltage drop across the inductance L. Therefore, the polarization voltage on measured sample (DUT) will be exactly the same as on the voltage source V_{DC}. The inductance L is connected directly to the control circuit of the Meissner oscillator. Oscillator serves for initiating whole circuit into self-resonance. The inductance L has a very low DC resistance and is not loaded by DC polarization voltage. At the same time, it effectively separates the high voltage part of circuit and oscillator by high frequency transformer.

The transformer helps to reduce penetration of energy of avalanche breakdown and other dynamic effects from the high-voltage part of the circuit into evaluating circuit with the oscillator. The resonant circuit also serves as a high efficient band-pass filter and protects the oscillator against overvoltage and other kinds of noise coming from high voltage circuit.

An active device in the oscillator is vacuum tube. This device is more resistant to surges or electronic shocks than semiconductor components. Vacuum tube operates at a higher level of input voltage, so that the effect of noise coming from the measured samples is reduced. The electron-coupled oscillator is made of a pentode, a resonant circuit, a grid resistor and a capacitor. The pentode is equipped by feedback from the second grid. The high-frequency transformer together with the pentode creates a so-called three-point Meissner oscillator. The inductance itself and capacitor in the resonant circuit are designed to be resistant to damage by high-voltage peaks.

The output of the oscillator is indicated on the built-in counter. The actual resonant frequency f_r is than shown immediately for current capacity C_X of the measured sample. From equation (1), then the capacity of measured sample C_X can be simply derived

$$C_X = \frac{1}{\frac{1}{4\pi^2 f_r^2 L - C_P} - \frac{1}{C_N}}. \quad (2)$$

Knowledge of both main circuit variables C_N, L and parasitic capacity C_P is a necessary condition of the calculation. Parasitic capacity C_P is in the same order as measured C_X. Both of them are in the order of hundreds or thousands of picofarads. Therefore, our task is to find out three unknown circuit variables. Fortunately, three independent equations can be written to describe a circuit in three different states as follows:

Disconnected measured sample DUT

When the terminals **A**-**B** are disconnected, the resonant circuit is made only of the inductance L and its own parasitic capacity C_P. For such simple circuit we can get the equation 3:

$$C_P = \frac{1}{4\pi^2 f^2 L}. \quad (3)$$

Typical resonant frequency of this unloaded circuit is about 1 MHz. The parasitic capacity C_P of winding for air-cored coil is of the order of 100 pF. Inductors suitable for most of PSDs have an inductance in the order 100 μH.

Short-circuit measurement of the DUT

When the terminals **A**-**B** are shorted, we basically measure the almost infinite capacity C_X. The resonant frequency of such circuit is then given by formula

$$f_r = \frac{1}{2\pi\sqrt{L(C_N + C_P)}}. \quad (4)$$

The typical resonant frequency of such a circuit will be about 100 kHz; using a C_N capacitor of nanofarad units. The C_N capacity should be in the same order (or better higher) then the capacity of measured sample. The capacity C_N cannot be affected by applied polarization voltage; i.e. it must be voltage independent. Therefore, high voltage ceramic disc capacitors designed for output stages of RF transmitters are suitable. Vacuum capacitors usually have a significantly lower capacity, typically in the order of hundreds of picofarads.

General reactance of DUT

In the general case, the resonant frequency of the circuit is given only by formula (1). Besides semiconductor samples, we can used as the DUT whichever capacity or reactance that will be without losses or losses will be less than 1 %. For the determination of main circuit variables, it is useful to use the etalon of capacity (e.g. vacuum capacitor). Such a device has a stable capacity which can be measured by an RLC-bridge with sufficient accuracy.

The described procedure leads to the set of three independent equations with three unknown variables. Such a task can be simply solved with the numerical Solver tools in MS Excel. When more than one etalon with a known capacity is used, we can obtain a larger set of equations that are in mutual dependence. Such a task has a lot of solutions, but with some inaccuracy. There is no analytical solution. The described procedure allows us to verify all parameters of the main circuit before the measurement itself. We can also observe time and temperature shift of these circuit variables. When knowing all parameters of the circuit, we can provide the measurement of C_X according formula (1).

C-V CURVES, RESISTIVITY CALCULATION

Description of C-V curves

When we know the capacity of biased pn junction (mostly at the current DC voltage) we can study the scattering of the electric field in the Space Charge Region (SCR). Finally, we can calculate the initial resistivity of the bulk/Si-wafer. The theoretical background is described in detail e.g. in [3] and can be (with some simplification) shown in the Fig. 2.

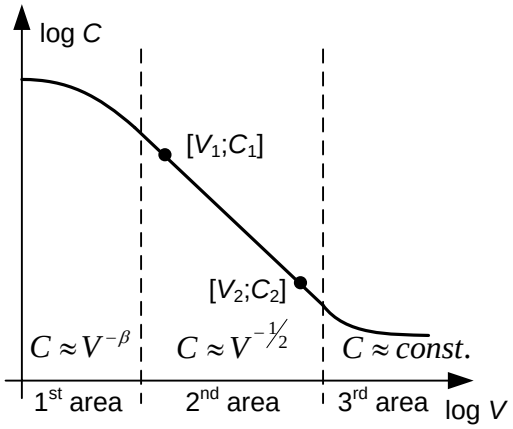

Figure 2: Typical voltage dependence of pn junction capacity in logarithmic scale.

In the 1st area (low polarization voltage in the order units of volts) are capacities of basis P and N comparable. The capacity is approximately equal to the power function $C \approx V^{-1/3}$. It can be drawn on a logarithmic scale as a decreasing line with the derivation −1/3. If the applied voltage increases, the capacity behaves as the curve in the 2nd area. The voltage dependence of the capacity is equal to the power function $C \approx V^{-1/2}$. Pn junction behaves as an ideal capacitor. The width of SCR, resistivity of initial Si bulk and other parameters can be computed according [3]. On the logarithmic scale, it can be drawn as a declining line with derivation −1/2. Such a dependence is typical for abrupt pn junction with polarization up to kV units.

When the applied voltage in the 3rd area continuously increases, the SCR suddenly stopped its expansion. The decrease of capacity slows down. The electric field propagates over the entire width of Si wafer and has no space for further expansion. The capacity of pn junction stops decreasing and is almost constant.

In the real situation, capacity behaves as a power function $C \approx V^{-\alpha}$, but with a very small exponent approaching zero. This effect is characteristic of 3rd area and is called the „compressed field“. Such a dependence is typical for power rectifier diodes with narrow bases. They are optimized for rectifying huge currents and have a very low forward voltage drop. Avalanche diodes and high voltage diodes for voltage levels 5÷7 kV are characterized only by 2nd area. They behave exactly according theoretical model derived for pn junction.

Resistivity calculation

In the 2nd area, SCR behaves as an ideal linear plate capacitor with thickness w and relative permittivity $\varepsilon_r = 11.7$. Under these conditions, calculations introduced in [3] can be performed. The width of the SCR expansion can be obtained from the formula

$$w = \frac{\varepsilon_0 \varepsilon_r S}{C}, \tag{5}$$

where w is the width of SCR (typical value about tens of μm); S is the active area of pn junction; C is the electrical capacity given by the procedure described in previous chapter. For an abrupt pn junction with P^+N or N^+P structure and by Poisson equation, the following expression can be derived

$$\frac{1}{C^2} = \frac{2}{S^2 e \varepsilon_0 \varepsilon_r N_D}(V_D + V), \tag{6}$$

where V_D is the diffusion voltage; V is the external polarization voltage (bias) and e is the elementary charge. The linear trend of the dependence $1/C^2 = f(V)$ follows from the expression (6). Let's note that equations (5) and (6) are correct only for the reverse polarization of the investigated pn junction. Diffusion capacity should be taken into account when forward polarization is assumed. Furthermore, all the expressions dealing with capacity are correct only for a planar pn junction. By combining equations (5) and (6) we can determine the concentration of donors N_D donors in the SCR as follows

$$N_D = \frac{2 \varepsilon_0 \varepsilon_r V_r}{e w^2}. \tag{7}$$

A typical resulting value will be in the range of 10^{12} cm^3 to 10^{14} cm^{-3}. The last step of this procedure is the conversion from the N_D concentration to the volume resistivity ρ (Ωcm). For commonly used material (Si, Ge, etc.) some empirical formulas or nomograms from old references [4] can be used. There are some online calculators on the websites, e.g. [5]. The simplest empirical formula for converting concentration to volume resistivity follows

$$\rho = \frac{4 \cdot 10^{15}}{N_D}. \tag{8}$$

A circular chip or wafer characterized by its diameter D is the simplest sample of bipolar power device. If we take into account the calculation only in the 2nd area of

the *C-V* curve, we can use the expressions (5-8) and assuming a derived dependence $C \approx V^{-1/2}$, the resistivity depends only on the dimensions of the sample and its capacity at the given applied voltage.

$$\rho = const \cdot \frac{D^4}{C^2 V} = const' \cdot D^4 \cdot \tag{9}$$

Thus, the calculation of resistivity is affected only by the dimensions of sample (e.g. diameter) and the measured capacity. The result does not depend on the applied voltage; from a physical point of view it cannot depend. Expression (9) is very important for estimating the uncertainty of a method and accuracy.

Electric field compression

Resonant method resp. the measured dependence $C = f(V)$ can be used for an approximate calculation of compression of the electric filed in the SCR. The possibility to describe all areas of the *C-V* dependence shown in Fig. 2 by a general power function, where β is mostly a negative number, is the basic principle of the method.

The onset of compression is defined as the voltage at which the capacity drop slows. Let's say it is an idealized border between 2nd and 3rd area. This border is actually the intersection of the two curves of the power function. This means that we must solve the following set of equations (10) and (11):

$$C = A_2 \cdot V^{\beta_2}, \tag{10}$$

$$C = A_3 \cdot V^{\beta_3} \cdot \tag{11}$$

The coefficients A_2 and β_2 correspond to the measured dependence in the 2nd area. The coefficients A_3 and β_3 correspond to the measured dependence in the 3rd area. Using simple algebra, it can be derived that the applied voltage *V* at the equality of both relations is given by

$$V = \left(\frac{A_2}{A_3} \right)^{\frac{1}{\beta_3 - \beta_2}} \cdot \tag{12}$$

The analytical result of (12) has no physical significance. The compression process begins gradually with the expansion of SCR. The border between the 2nd and 3rd areas is not as sharp as shown in the actual measurement in Fig. 3. The compression start value was determined to be 1173 V according to (12) (marked by gray dashed line).

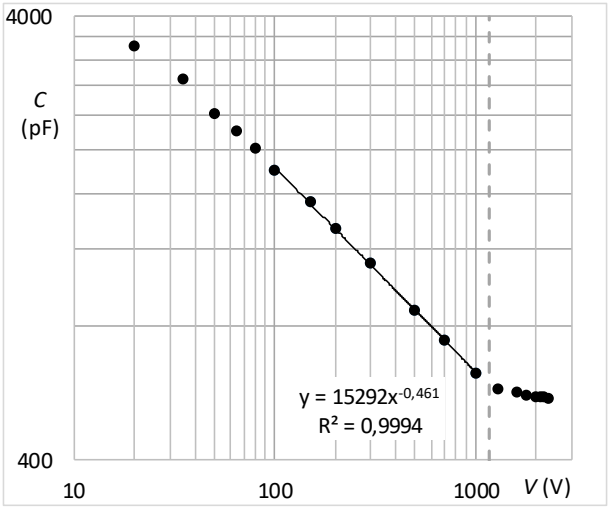

Figure 3: Real measurement of 2,2 kV rectifier diode.

It should be noted that before providing the calculation according to (12), it is necessary to obtain an analytical description of the individual areas of the *C-V* curve. The process is illustrated in Fig. 2. There are two measured points in the 2nd area marked with coordinates [V_1; C_1] and [V_2; C_2]. Substitution of these coordinates into power function $y = A x^{\beta}$ creates a new set of two equations. The analytical solution of this set is trivial:

$$\beta = \frac{\log(C_1) - \log(C_2)}{\log(V_1) - \log(V_2)}, \tag{13}$$

$$A = \frac{C_1 + C_2}{V_1^{\beta} + V_2^{\beta}} \cdot \tag{14}$$

The coefficients *A* and β can be than used to calculate the electric field compression according to (12).

PRACTICAL MEASUREMENT AND RESULTS

A prototype of the equipment described in the previous chapters was built in the year 2018 at the Department of Electrotechnology of the CTU in Prague. The basic parts and layout of the equipment are clearly visible in the Fig. 4. The polarization voltage source is manually controlled in the range 0÷7 kV and is equipped with a 4.5-digit display for indication. The operation of the oscillator can be checked by a built-in counter. The oscillator is further connected to the BNC output. The excitation of the vacuum tube circuit can be observed using a built-in micro ammeter. The round table for contacting the measured sample is placed outside the equipment and is fixed with N connector. This solution shows negligible parasitic capacity and does not affect the measurement. The measuring chamber together with the central table is accessible through a transparent plexiglass cover.

Figure 4: Prototype of a capacity measuring equipment.

The vacuum capacitor shown in the Fig. 5 was used to calibrate and determine all circuit parameters according to the circuit diagram in Fig. 1. A high-voltage vacuum capacitor 100 pF/15 kV was made in the Soviet Union for radio broadcasting transmitters. Both capacitor terminals were secured with non-ferromagnetic screw terminals. The capacity of this calibration etalon was measured with an accurate RLC meter HP 4284A with an accuracy of 0.5 %.

After that the calibration capacitor was inserted into the measuring chamber and its capacity was measured in the whole range of possible polarization voltage. There are two general advantages to using vacuum capacitor. First, it shows immeasurable power losses over the entire voltage range, i.e. it seems to be an ideal capacitor. Second, the capacity is voltage independent. Such an etalon does not attenuate the resonant circuit and does not affect the measurement itself. The only disadvantage is the relatively small capacity (10^2 pF). Fortunately, this value is comparable to most of the measured samples.

Figure 5: Vacuum capacitor used as an etalon.

Several typical samples of power bipolar devices were measured using the device described in Fig. 4. The first example is introduced at once in Fig. 3. There is a *C-V* curve typical for rectifier diodes with strong compression of electric filed. A sample 36 mm in diameter shows a power function in the range of 100 V to 1000 V with an exponent close to −0.5. In the range above 1000 V, a gradual compression of the electric filed occurs. Using formula (12), the limit was calculated as a value of 1170 V. The resistivity of the bulk material was computed based on the measured capacity and its value is 94 Ωcm. The resistivity band required by the Si-wafer supplier is 85÷115 Ωcm. In the low-voltage region (tens of volts), the bend of *C-V* curve corresponding to the 1st area is clearly visible.

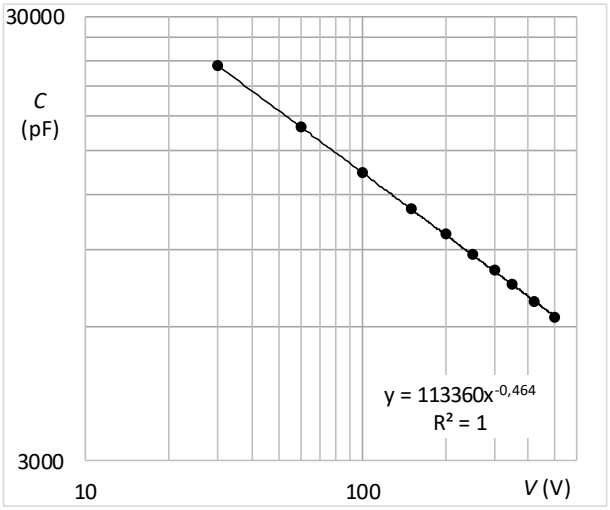

Figure 6: Measured *C-V* curve of 2.5' welding diode.

Fig. 6 is an example of *C-V* curve for welding diode with 2.5' diameter. The sample was measured only in a reduced voltage range up to 500 V. The power dependence has an exponent very close to −0.5. Large samples (cca 31 cm^2) are responsible for a large total capacity of 10^4 pF. The calculated resistivity of the bulk material is 15 Ωcm. This is in a good agreement with the band given by the supplier 10÷20 Ωcm. The purpose of welding diodes is to rectify huge current and their reverse blocking voltage usually does not exceed 400÷500 V. The *C-V* curves lie only in the 2nd area and do not show any field compression.

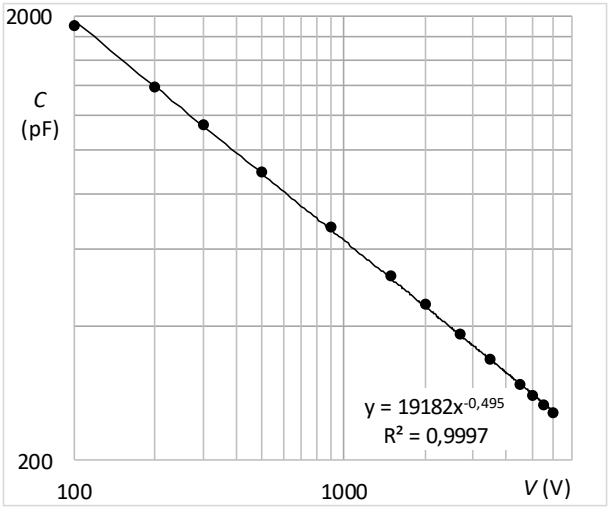

Figure 7: Measured *C-V* curve of 2' rectifier diode for 6 kV.

Fig. 7 is an example of *C-V* curve for 6kV diode with 2' diameter. The sample was measured in the whole range up to 7 kV. The power function has an exponent exactly equal to −0.5. The total capacity in the order of 10^3 pF corresponds to 18 cm^2 of active area of the examined sample. The calculated volume resistivity is 270 Ωcm. It is in accordance with the band 245÷275 Ωcm specified by the supplier. Such 6kV diodes have almost the same profile and *C-V* character as avalanche diodes. A very thick Si-wafer was used; the initial thickness was more than 800 μm. Therefore, the whole *C-V* curve is located only in the 2nd area. There is no field compression.

COMPARISON WITH 4POINT METHOD

Standard 4point method is based on a direct measurement of the Ohm's resistance of wafer and uses a simplified theoretical model, which is inaccurate in principle. Furthermore, this method needs direct contact with the measured surface, so there is a risk of damages and cracks on the wafers. Simplicity and hardware availability are the biggest advantages. There is a lot of measuring apparatus dedicated directly to this purpose. All manufacturers of Si wafer use this method and their data are comparable. The main disadvantage is that the measurement cannot be performed on the final device. The measurement is only possible on a local volume of cca mm^3 before the start of diffusion processes.
The proposed resonant method allows to measure the whole volume of devices and enables measurements on a diffused wafer with a final pn junction. It must be mentioned that the described method cannot be used on a bulk Si-wafer. Triangular electric filed in measured pn junction is needed. Therefore, it can be applied to a diode structure which contains a pn junction allowing an electric field. Statistic control of the diffusion process or reverse engineering on competition devices is possible using this method. This is the main advantage of the newly described method.

The estimation of the inaccuracy of the proposed method has two main parts. The first part deals with the analysis of the resonant circuit and the determination of all parasitic parameters by equations (1-4). The resonant frequency can generally be measured very precisely. Using the described calibration capacitor, we can measure the capacity of the common pn junction (cca 10^3 pF) with the accuracy of pF units. The relative error of capacity measurement is thus 0.5 % or rather 0.1 %.
The second part deals with estimating the inaccuracy of the calculation procedure described by the equations (5-9). An interesting result from (9) is that the largest error concerns the uncertain dimensions of measured sample. The explanation is in Fig. 8. It can be shown that the resistivity is proportional to the 4th power of the diameter *D* and this parameter has the biggest influence on total inaccuracy of the calculation. The capacity C_X can be measured with an accuracy of 0.5 % or better, see paragraph above.

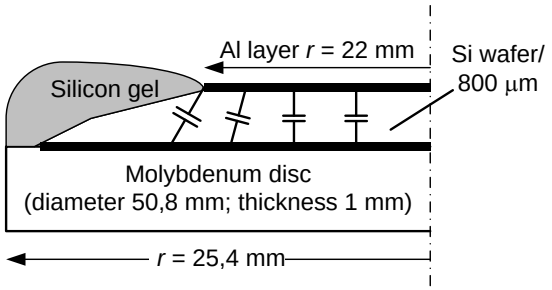

Figure 8: Uncertain diameter of measured capacitor.

The applied polarization voltage *V* can be measured with an accuracy of 0.1 %. The biggest issue is the determination of samples dimensions resp. capacitors dimensions. Remember that only the active area of the sample is important. The chip bevel and facet cover with a silicon coating are not covered by metallization, so they do not participate in the total capacity. According to (9), the total error of the resistivity calculation is in the worst case given by following formula

$$|\delta_\rho| = 4|\delta_D| + 2|\delta_C| + |\delta_v|, \tag{15}$$

where δ_i are relative errors for all variables used. We can conclude that the greatest influence on the uncertainty of resistivity determination has the inaccuracy of determining the sample dimensions.

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Structure-Aware Compact Thermal Models of Power LEDs

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Abstract

This paper based on the example of white power LEDs illustrates the methodology for the generation of device compact thermal models, whose element values can be assigned physical meaning. The diode thermal behaviour was studied both with the forced water cooling and with the natural convection air cooling. Moreover, owing to the fact that the investigated devices had an electrically isolated thermal pad, the measurements were carried out with the thermal pad properly soldered and with the pad left unconnected, what facilitated the identification of particular sections in the heat flow path. All the measurements of device heating or cooling curves were taken according to the JEDEC standards. The determination of the optical power allowed the computation of the real heating power, which was used then as the input quantity for thermal computations and analyses presented in this paper. Based on the measurement results, thermal structure functions and time constant spectra were computed using the Network Identification by Deconvolution method. The compact thermal models of the investigated LEDs were derived based on the time constant spectra. Owing to the proposed methodology, it was possible to attribute physical meaning to model element values. The accuracy of generated compact models was validated by comparing the simulated heating curves with the measured ones. Although the compact models for the investigated cases consisted only of four RC stages, they provided excellent simulation accuracy with errors below 4% of the maximum temperature rise value.

Keywords: power LEDs, electrical, real heating power, Network Identification by Deconvolution, compact thermal models.

INTRODUCTION

Light Emitting Diodes (LEDs) become more and more important in our everyday lives. Compared to traditional light bulbs, LEDs are much more energy efficient, they last longer and, above all, they cost less [1]. However, their efficiency is still limited, so they produce not only the desired optical energy, but they dissipate significant amount of heat as well [2]. Therefore, Compact Thermal Models (CTMs) of LEDs and their cooling environment are always an indispensable part of larger multidomain system models [3].

Discrete thermal models are usually generated using the well-known electro-thermal analogy and typically they consist of a limited number of n thermal resistors R_{thi} and capacitors C_{thi}, whose product is called the thermal time constant τ_i. Different topologies of such thermal models were already proposed in the series of JEDEC JESD51 standards, including the canonical Foster RC networks. Then, device thermal responses in time $T(t)$ caused by the dissipated thermal heating power P_{th} can be found in such networks according to the following formula:

$$T(t) = P_{th} * \sum_{i=1}^{n} R_{thi} * \left[1 - e^{-\frac{t}{\tau_i}}\right] \qquad (1)$$

Foster RC networks can be derived using the Network Identification by Deconvolution (NID) analysis method, which is currently the base for the thermal measurement and modelling standards adopted for different electronic devices, not LEDs alone [4]. For real electronic systems the number of RC stages used in a model is theoretically infinite, but as it will be shown later on such models can be reduced to a compact form, preserving at the same time acceptable simulation accuracy.

According to the NID method, dynamic measurements of temperature responses have to be taken at instants equally spaced on the logarithmic time scale. Only then, all thermal time constants present in a response could be properly identified. Introducing a new time variable $z = \ln(t)$ and performing then numerical deconvolution, the continuous thermal time constant spectrum R_τ could be computed [5].

The concept of thermal resistance spectra extends the Foster RC ladder model, which can be related to each other as shown in Fig. 1. Namely, the Foster model can be obtained directly from the thermal resistance spectral density by dividing it into narrow segments having the width Δz. Then, each segment corresponds to a parallel RC connection, Thus, the RC equivalent Foster model results directly from the discretization of continuous time constant spectra.

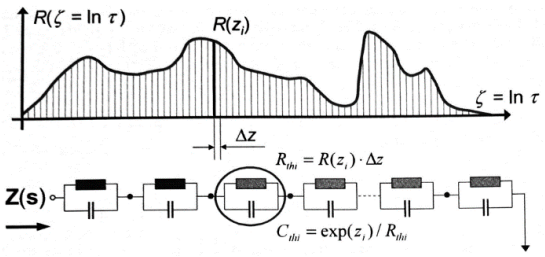

Fig. 1: The thermal time constant spectrum corresponding to the Foster RC network [4].

The thermal resistance spectra render possible also the construction of functions describing the entire heat flow path from the device junction to the ambient, which are known as cumulative thermal structure functions, shown in Fig. 2, relating the cumulative capacitance $C_{th\Sigma}$ and the cumulative resistance $R_{th\Sigma}$. These functions solve the main problem related to the Foster networks consisting in the fact that the node-to-node capacitances imply that thermal responses propagate instantaneously through the entire system and consequently thermal resistances and capacitances cannot be related to any physical part of a system.

Fortunately, the Foster RC networks can be transformed into mathematically equivalent Cauer networks, whose elements could be already assigned physical meaning. Such networks are formed by series thermal resistances and parallel capacitances, all connected to the thermal ground, however, the Cauer RC networks result from the discretization of the cumulative structure function performed in a similar way as described previously.

The main goal of this paper is to investigate the thermal properties of LEDs and to develop adequate methods for their thermal modelling. Based on measurement results, cumulative thermal structure functions of the diodes are calculated and their compact thermal models are derived from the time constant spectra using the NID method. The following section describes the experimental set-ups and presents obtained measurement results. Then, the results are analysed and the methodology to generate LED compact thermal models is introduced. Finally, the transient temperature simulation results obtained with these models are compared with the measurements.

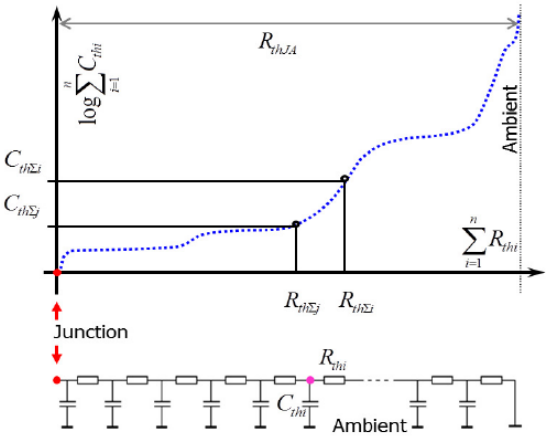

Fig. 2: The cumulative structure function corresponding to the Cauer RC network [6].

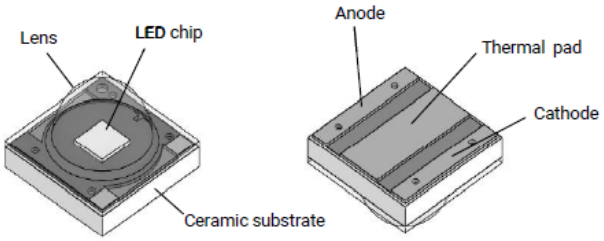

Fig. 3: Package of the investigated LED [7].

MEASUREMENT RESULTS

This section presents in detail the obtained measurement results. First, the investigated devices and their cooling conditions as well as the equipment used in experiments are described. Then, the diode temperature sensitivities are determined. Next, the device junction temperature transient measurement results for different mounting manners and cooling conditions are discussed. Finally, the optical measurements results are briefly covered.

Experimental Set-Ups

The particular device investigated here is the 3 A white power LED from the Cree XP-L family, whose package, shown in Fig. 3, has a thermal pad which is electrically isolated both from the cathode and the anode. This pad enhances the heat removal from the LED package to the board. For the experiments, the investigated diodes were mounted on metal core PCBs, whose dimensions were 2.50 cm x 2.50 cm x 0.16 cm. In order to investigate the influence of the thermal pad, two configurations were considered, once the thermal pad was properly soldered to the board and once it was left unconnected.

Additionally, two different types of cooling conditions, shown in Fig. 4, were applied. During the measurements with the free convection cooling the MCPCB with the Device Under Test (DUT) was suspended horizontally in thermally insulating clamps (see Fig. 4a), whereas with the forced water cooling the board was firmly pressed, again with the clamps, against a copper cold plate, as pictured in Fig. 4b. The thermal resistance between the board and the cold plate was reduced owing to the application of thermal grease. The cold plate temperature was maintained automatically at a desired value by a thermostat. During experiments both water and cold plate temperature values were measured.

a) free convection air cooling b) forced water cooling

Fig. 4: Cooling conditions applied during measurements.

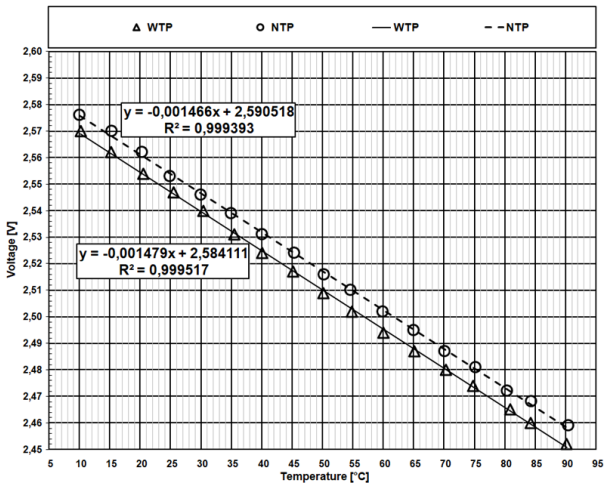

Fig. 5: Measured LED temperature sensitivity.

The measurements of diode heating or cooling curves were taken with the transient thermal tester T3Ster®, currently produced by Siemens. This equipment renders possible real time thermal impedance measurements compliant with the JEDEC standards by recording the device transient temperature responses to unitary power step excitations with the microsecond time resolution. The analysis of obtained experimetal results facilitates the evaluation software provided together with the tester and implementing the earlier described NID method.

Electrical Measurements

Before actual measurements the temperature sensitivity of the investigated LEDs had to be determined. For this purpose, the LEDs soldered to PCBs were placed on the cold plate. Then, the measurement current of 10 mA was forced through the devices and the diode voltage was recorded. The results of this calibration procedure are presented in Fig 5. As can be seen, both diodes show nearly perfectly linear characteristics of their junction voltage drop in function of temperature. The measured temperature sensitivity of the diode with the thermal pad connected (WTP) was equal to -1.479 mV/K whereas the sensitivity of the diode with the pad not connected (NTP) was -1.466 mV/K.

After the calibration, as mentioned previously, the diode cooling curves were recorded applying different kinds of cooling conditions. The measurements with the free convection cooling, denoted in the figures as FA, were performed for the diode currents of 350 mA, 700 mA and 1000 mA. In order to reach the thermal steady state the LEDs had to be heated for 1800 s and then cooled over the same period of time.

During the measurements with the forced water cooling, denoted further on as CP, the cold plate temperature was set to 20 ºC and the measurements were taken for the LED currents of 0.7 A, 1.0 A, 1.5 A and 2.0 A. Such high current values could not be attained with the free air convection cooling because of the excessive junction temperature. This time the diodes were heated only for 300 s until the thermal steady state was reached and then the cooling curve was recorded.

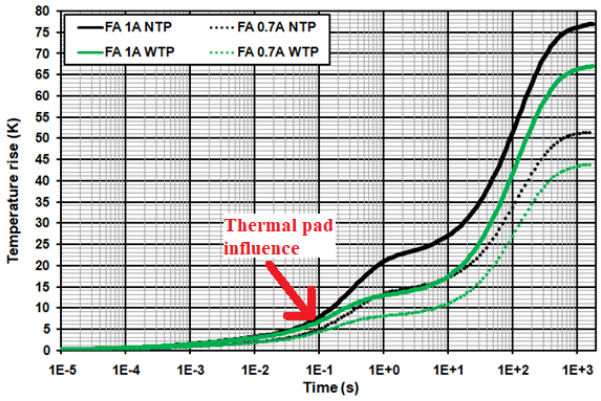

Fig. 6: Thermal pad influence in the case of the natural convection cooling.

The measurement results are shown in Figs.6-9. In order to facilitate the analyses, the figures represent the diode heating curves, which were obtained by subtracting the recorded cooling curves from the respective steady state temperature values. Analysing now the influence of the thermal pad, it can be seen that its presence affects the heating curves already after several tens of milliseconds. Independently of the applied cooling conditions, the pad noticeably enhances the dissipated heat removal. With the free convection cooling the device temperature rise is reduced owing to the use of the pad by one third and for the forced water cooling this reduction is even more significant.

Examining the influence of cooling conditions on the device heating curves, it can be observed that for the same current value the curves are initially identical and then they diverge drastically after a couple of seconds. When the thermal pad is not connected the junction temperature rise value is some two-third lower in the case of forced water cooling. This reduction is more important for the LEDs with the pad soldered, reaching even 80%.

Hence, it is evident that attaching the devices to a cold plate assures much better heat removal than in the case of free convection cooling. Furthermore, with the forced water cooling the thermal steady state is reached much faster, only after a few seconds, compared to the couple of minutes required in the case of natural convection cooling.

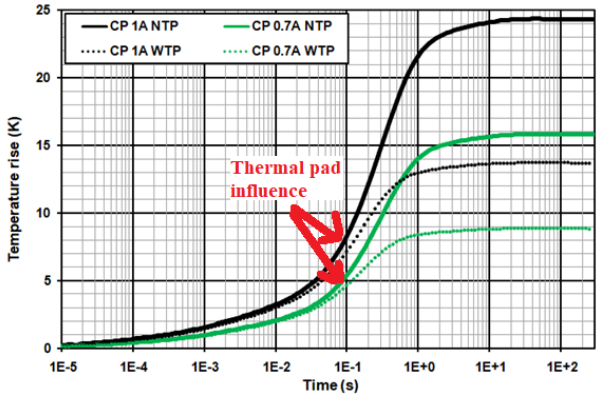

Fig. 7: Thermal pad influence in the case of the forced water cooling.

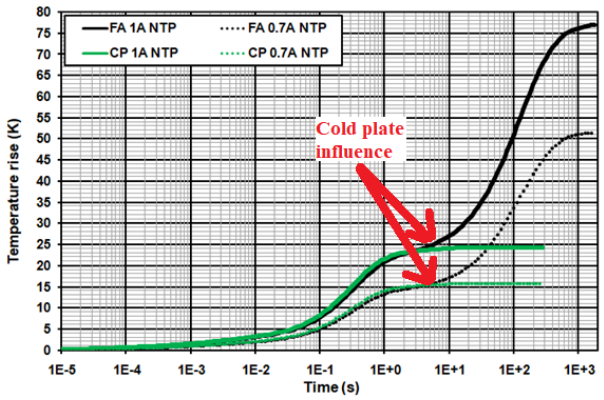

Fig. 8: Cooling condition influence for LED with the thermal pad not connected.

Optical Measurements

For most electronic systems the NID thermal analysis method could be applied directly using the electrical power value P_{el} as the input variable, since it is almost entirely dissipated in the form of heat. However, when a system contains devices in which the electrical energy is converted into some other form, e.g. the optical one P_{opt}, as it is in the case of LEDs, only the real heating power P_{th} has to be used for thermal analyses. This fact was stated in the JEDEC standard concerning LEDs [8]. The main function of LEDs is the generation of light. This occurs when the electric current flows through the junction of a diode. Unfortunately, these devices do not convert all delivered energy into light and a significant part of the input electrical power is dissipated as heat. Typically around a half of the energy is converted into heat, but the exact values depend on many factors, such the device current or operating temperature.
Here, the data concerning the optical power values were acquired from the earlier results published in [9]. There, the optical power was measured using the set-up shown in Fig. 10, where the diode was placed on a cold plate inside a light tight box. Then, the light intensity was measured directly over the diode and the total optical power was calculated based on the knowledge of the spatial distribution of the emitted light provided in the LED datasheet by device manufacturer.

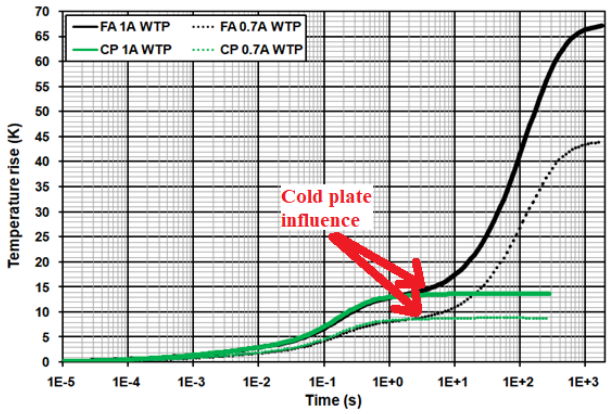

Fig. 9: Cooling condition influence for LED with the thermal pad soldered.

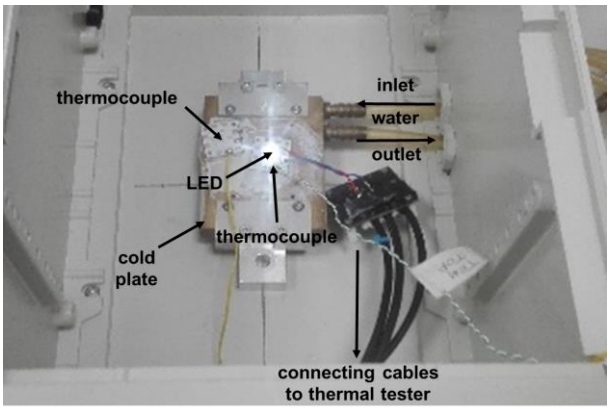

Fig. 10: Experimental set-up used for the measurements of optical power [9].

The results of these optical measurements, adapted from [9], are presented in Table 1. As can be seen, for the investigated diodes their optical efficiency η_{opt}, being the ration of the optical power to the electrical power, drops down when the device current increases. Then, correspondingly more supplied energy is transformed into heat. At the same time, the influence of temperature on the LED efficiency turned out not to be so important.

	I[A]	P_{el}[W]	P_{opt} [W]	η_{opt} [%]
Forced convection cooling 20°C with thermal pad	0.70	2.08	1.49	71.46
	1.00	3.06	2.07	67.46
	1.50	4.79	2.97	61.99
	2.00	6.60	3.78	57.24
Forced convection cooling 20°C with no thermal pad	0.70	2.06	1.44	69.88
	1.00	3.01	1.98	65.81
	1.50	4.64	2.79	60.08
	2.00	6.34	3.48	54.85
Natural convection cooling with thermal pad	0.35	0.98	0.68	69.53
	0.70	2.02	1.30	64.10
	1.00	2.95	1.74	58.98
Natural convection cooling with no thermal pad	0.35	0.98	0.71	72.69
	0.70	2.00	1.34	66.97
	1.00	2.90	1.79	61.65

Table 1: The optical measurement results.

THERMAL ANALYSES

This section provides detailed analyses of measurement results, which are obtained employing the NID analysis method. According to the discussion from the previous section, all the presented results are produced using the real heating power as the input quantity.

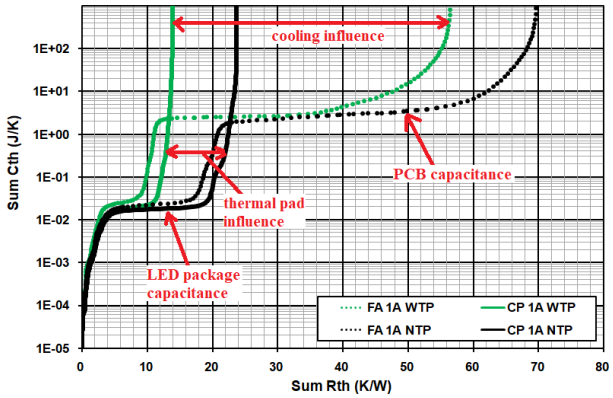

Fig. 11: Comparison of cumulative thermal structure functions for 1 A LED current.

First, the thermal structure functions are analysed and compared for different experimental set-ups. Then, the thermal time constant spectra for the considered cases are discussed. Next, the methodology used to generate CTMs is introduced together with the explanation of the physical meaning of particular model element values. Finally, the generated CTMs models are validated with measurement results.

Thermal Structure Functions

The cumulative thermal structure functions allow the identification of both thermal pad and cooling condition influence on thermal resistances. The analyses presented here begin with the examination of structure functions presented in Fig. 11. From the figure, it is clearly visible that the thermal pad reduces significantly the thermal resistance, what coincides with the earlier observations considering heating curves. The flat section around the thermal capacitance of 20 mJ/K can be attributed to the package capacitance and the one at around 2 J/K to the one of MCPCB.
The use of the cold plate visibly reduces the thermal resistance, around three times when the pad is soldered and almost four times when the pad is not connected. The thermal pad decreases the total thermal resistance by almost 10 K/W, but only in the section, where heat diffuses from the package to the board. On the other hand, the change of the cooling mechanism affects the entire structure function.

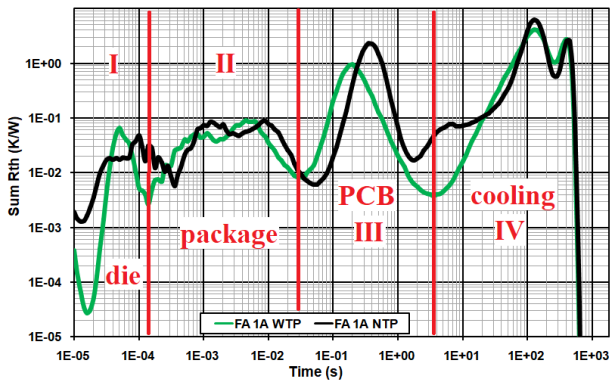

Fig. 12: Comparison of time constant spectra for the free convection cooling.

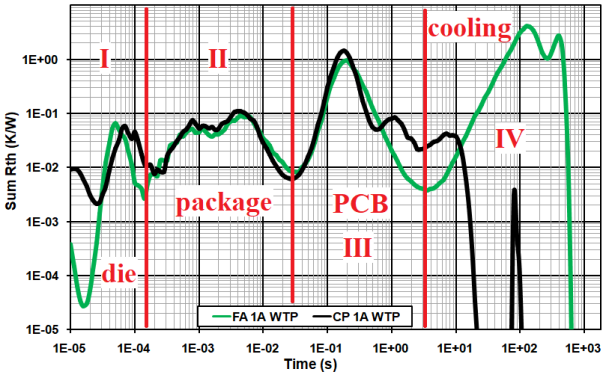

Fig. 13: Comparison of time constant spectra for the LED with the thermal pad soldered.

The natural convection cooling influences the thermal resistance already inside the package since heat spreads more laterally through its entire volume. Moreover, the structure function has an additional, long, flat section corresponding to the heat exchange with the air. The length of this part depends mainly on the value of the heat transfer coefficient. On the contrary, owing to the use of the cold plate, the thermal resistance is much lower and the structure function ends earlier. Then, the thermal capacitance of the MCPCB is no longer visible in the structure function because the heat spreads into the cold plat only through a very small part of substrate volume.

Time Constant Spectra

The time constant spectra demonstrating the influence of the thermal pad and applied cooling conditions are presented in Figs. 12-13 respectively. According to the NID method theory, the minima in the spectra indicate time instants when heat diffuses into another material. These spectra have three clear minima marked in the figures with thick vertical lines.
The first minimum between Sections I and II reflects the die attach thermal resistance. Furthermore, leaving the thermal pad unconnected shifts the peak in Section III to the right from 0.2 s to almost the double of this value and the spectral density of the resistance becomes much higher, what suggests that the shift is mainly due to the increase of the resistance. Finally, the change of cooling conditions affects only Section IV of the spectra.
Thus, Sections I and II reflect the heat flow inside the LED package from the semiconductor die to the solder point, whereas Sections III and IV the heat conduction into the PCB and the cooling. In this way the thermal time constant spectra can be divided into four sections corresponding to the physical parts of the structure.

Compact Thermal Models

Following the above presented discussion concerning the time constant spectra, the CTMs for the investigated circuits can be derived by dividing the spectra in the location of their minima. The main advantage of this solution is that it might preserve the physical meaning of model element values [8].

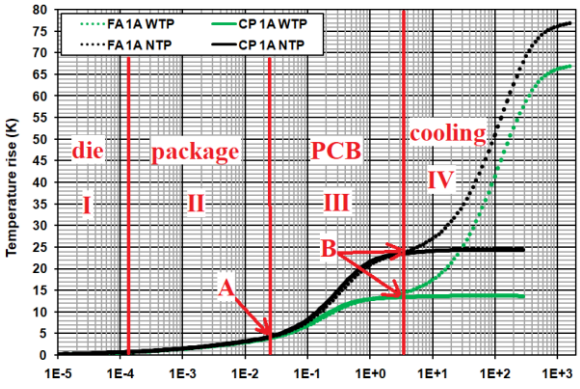

Fig. 14: Diode heating curves divided according to different heat flow path sections.

The four heat flow path sections identified in the spectra correspond to the respective locations in the heating curves indicated in Fig. 14. These curves diverge for the first time at Point A owing to the use of the thermal pad and then at Point B due to the change of cooling, what proves the correctness of the proposed approach.

For each of these sections, their thermal resistances can be computed by adding the components of the spectrum. The next step is to determine the thermal time constant values for each section. The best strategy is to assign initially for each time constant the value coinciding with the maxima in the spectra, what yields relatively small simulation errors, which could be further minimized. Then, the capacitance values could be computed simply by dividing the respective thermal time constant and resistance values. In this way a CTM in the form of RC Foster network is obtained.

Although it is easier to compute temperature responses using the Foster network, the physical meaning can have only the Cauer RC network element values. Therefore, the last step is the conversion from the Foster to Cauer network, such as the one shown in Fig. 15. The conversion can be performed employing the algorithm presented in [4]. The resulting values of the Cauer RC network element values for the curves shown in Fig. 14 are provided in Table 2.

The analysis of the values given in the table confirms the earlier observations. For the free convection cooling, the last component corresponding to the thermal time constant of some 140 s is the dominant one. Its thermal capacitance of 3 J/K is the capacitance of the MCPCB and its resistance of almost 50 K/W reflects the heat exchange with ambient. Knowing the surface area of the board, i.e. just over 13 cm^2, the value of the heat transfer coefficient h can be estimated around 17 ,$W/(m^2 K)$, what corresponds well to values predicted theoretically for the natural convection.

With the forced convection cooling the last component is very small and then the third component becomes dominant. This RC stage describes the package to board interface, so the impact of the thermal pad is reflected in its element values. As already mentioned, the time constant of this stage increases noticeably when the pad is not connected. This is due to the change of thermal resistance, which for the natural convection cooling increases from 8.4 K/W to 17.2 K/W.

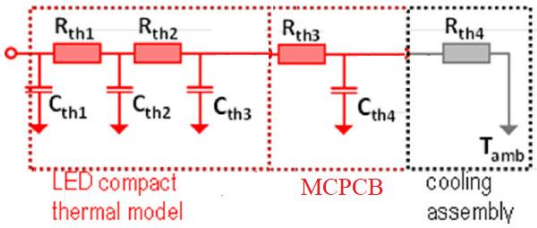

Fig. 15: The Cauer RC model for investigated structures [10].

The first and the second stage of the models correspond to the junction to solder point thermal resistance of the diode and its typical value provided in the datasheets is 2.2 K/W, whereas the measured ones fall in the range 2.5÷3.0 K/W. Therefore, these results are very realistic, taking into account that the exact boundary conditions applied during measurement were not specified by the manufacturer. Moreover, the CTMs in Sections I and II can be less accurate because, depending on the cooling conditions, they are relatively lower than the thermal resistances of Sections III or IV. Consequently, their estimates might bear more error because of relatively higher measurement noise.

Finally, the accuracy of generated RC ladder CTMs was verified by comparing the simulated heating curves with the measured ones. The results of this comparison are shown in Fig. 16, where the black lines denote the simulated curves. The dashed and double lines are used for the natural convection cooling with and without the thermal pad respectively. As can be seen, for all of the cases the simulated values closely follow the measured ones. In particular, for the free convection cooling with the thermal pad the maximum error is equal to 2.4 K, without the thermal pad it equals 2.2 K and finally for the forced convection with the thermal to only 0.4 K. Thus, this relatively simple 4 stage RC model provided excellent simulation accuracy with errors remaining always well below 4% of the maximum temperature rise value.

	sec	τ [s]	R [K/W]	C [J/K]
Natural convection cooling 1A with no thermal pad	I	3.83×10^{-5}	6.51×10^{-1}	5.89×10^{-5}
	II	3.40×10^{-3}	2.34×10^{0}	1.45×10^{-3}
	III	3.33×10^{-1}	1.72×10^{1}	1.94×10^{-2}
	IV	8.33×10^{1}	4.96×10^{1}	1.68×10^{0}
Natural convection cooling 1A with thermal pad	I	1.91×10^{-5}	4.59×10^{-1}	4.15×10^{-5}
	II	2.51×10^{-3}	1.99×10^{0}	1.26×10^{-3}
	III	1.96×10^{-1}	8.40×10^{0}	2.33×10^{-2}
	IV	1.44×10^{2}	4.57×10^{1}	3.15×10^{0}
Forced convection cooling 1A with thermal pad	I	3.71×10^{-5}	6.35×10^{-1}	5.84×10^{-5}
	II	2.40×10^{-3}	2.22×10^{0}	1.08×10^{-3}
	III	1.90×10^{-1}	1.06×10^{1}	1.79×10^{-2}
	IV	1.06×10^{1}	4.13×10^{-1}	2.55×10^{1}

Table 2: Cauer RC CTM values for different set-ups.

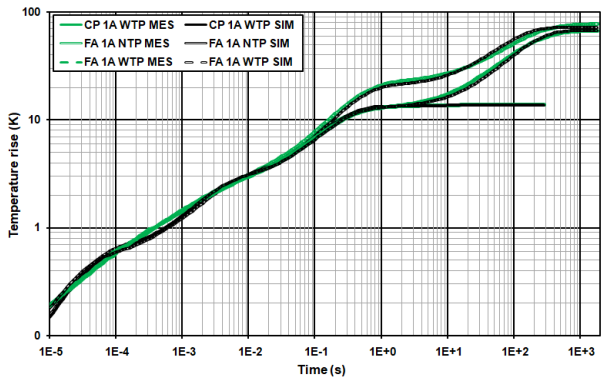

Fig. 16: Comparison of measured and simulated LED heating curves in different experimental set-ups.

CONCLUSIONS

This paper proposed a methodology to develop compact thermal models of power LEDs, which were generated in such a way that it was possible to relate particular model elements to selected regions of the structures, hence allowing physical interpretation of their values. As a result, the change of device mounting manner and cooling conditions affected only certain values of these CTMs.

Moreover, the paper demonstrated experimentally the influence of thermal pad and device cooling conditions on the value of junction to ambient thermal resistance. Specifically, it was shown that the use of thermal pad enhances significantly the heat conduction from the package to the board by lowering the thermal resistance. At the same time, the forced water cooling considerably improves the heat exchange between the board and the ambient.

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AUTHOR INDEX

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